

# Low Power CMOS Electronic Central Pattern Generator Design for a Biomimetic Underwater Robot

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**Abstract**— This paper, presents a feasibility study of a central pattern generator-based analog controller for an autonomous robot. The operation of a neuronal circuit formed of electronic neurons based on Hindmarsh-Rose neuron dynamics and first order chemical synapses is modeled. The controller is based on a standard CMOS process with 2V supply voltage. In order to achieve low power consumption, CMOS subthreshold circuit techniques are used. The controller generates an excellent replica of the walking motor program and allows switching between walking in different directions in response to different command inputs.

The simulated power consumption is 4.8mW and die size including I/O pads is 2.2mm by 2.2mm. Simulation results demonstrate that the proposed design can generate adaptive walking motor programs to control the legs of autonomous robots.

**Index Terms**—subthreshold operation, Central Pattern Generator, electronic neuron circuit, electronic synapse circuit, neuronal oscillator circuit

## I. INTRODUCTION

ROBOTS are fundamental in a broad spectrum of repetitive or dangerous work efforts ranging from industrial to field applications. Most contemporary robots, however, can operate only in simple structured environments. There is a strong demand for consumer, industrial, and scientific applications for autonomous robots that can operate adaptively in unpredictable environments. Existing robots are commonly controlled by algorithm based systems such as finite state machines[1]. However, algorithm-based robots controlled by digital processors adapt poorly to unstructured environments due to an inability to anticipate all contingencies. Animal models provide proven solutions to the problem of adaptation to field environments and the underlying neuronal mechanisms are understood adequately to allow construction of neuronal circuit-based controllers[2]. As a result, some investigators have focused on emulation of biological nervous systems through biomimetics[3].

The innate behavior of animals is controlled by central pattern generators (CPGs) resident in central ganglia or the spinal cord[4]. It is our contention that if CPG-based controllers are imitated, many problems due to deterministic control program can be solved and it will be feasible to develop

an adaptive autonomous robots that operate with flexibility in natural environment. CPGs can be constructed from electronic neurons based on non-linear dynamical models of biological neurons[5]. However, these circuits are built from discrete components and are not a realistic solution due to their size and power.

The basic concept of the CPG and its architecture are reviewed in Section II, and its sub-blocks are discussed in Section III. Section IV demonstrates the electronic CPG circuit followed by the HSPICE simulation results in Section V. Finally, Section VI concludes the paper.

## II. CENTRAL PATTERN GENERATOR

Central pattern generators are normally turned and modulated by descending motor commands and coordinated among themselves by coordinating neurons that provide a governed oscillator with information about the activity status of a governing oscillator to maintain gait [6]. During locomotion the motor programs generated by central pattern generators are modulated by sensory feedback. Depending on the locus of action of the sensory feedback within the CPG it can either modulate the amplitude of the output or reset its timing to adapt to environmental contingencies. We have been developing robots based on this central pattern generator model[3]. Our lobster-based platform is intended for remote sensing applications in the littoral zone. This robot features a physical plant based on the lobster body, artificial muscle fabricated from shape memory alloys, neuromorphic sensors and a controller based on known lobster circuitry[7].

Figure 1 represents the core of the central pattern generator (CPG) for control of the walking movements of one leg. The four interneurons form the neuronal oscillator for the four-phase rhythm and two of these interneurons (*elev* and *dep*) directly activate motor synergies that control the elevation/depression movements of the coxo-basal (CB) joint. The other two interneurons (*swing* and *stance*), activate both antagonistic motor synergies that control the thoraco-coxal (ThC) and mero-carpopodite (MC) joints of the leg. The interneuron timing circuit enclosed by the dashed square is activated by a parametric command that corresponds to the bias current (i)



To implement an electronic neuron circuit (EN), the Hindmarsh-Rose(HR) neuron model [8], [5] is used. Compared to other neuron models such as Fitzhugh-Nagumo or Hodgkin-Huxley, the HR model has several advantages. The mathematical equations are simpler than the Hodgkin-Huxley model that is based on global behavior rather than electrophysiological processes. Therefore, it requires less hardware resources and less design complexity. Also this model provides an accurate output frequency-input current relationship, which is not described by the Fitzhugh-Nagumo formulation. The mathematical expression of HR model is given by

$$\frac{dx}{dt} = y - ax^3 + bx^2 - z + I \quad (1)$$

$$\frac{dy}{dt} = c - dx^2 - y \quad (2)$$

$$\frac{dz}{dt} = r(s(x - x_1) - z) \quad (3)$$

where,

$x$ : membrane potential of neuron,

$y$ : recovery current of neuron,

$z$ : adaptation current of neuron,

$I$ : applied current,

$x_1$ : the leftmost equilibrium point of the neuron model without adaptation.

Coefficients of the Equation (1),(2), and (3) are:  $a = 1$ ,  $b = 3$ ,  $I = 3.024$ ,  $c = 1.01$ ,  $d = 5.0128$ ,  $r = 0.0021$ ,  $s = 3.966$ , and  $x_1 = 1.605$ .

The equations with given coefficients are used to describe the behavior of the biological neuron's action potential. Figure 2 (a) shows the solution to the Hindmarsh-Rose neuron model in the phase plane. The inner traces correspond to higher frequency oscillations than the outer traces, and the tail corresponds to the period between the bursts. This high-level behavioral simulations of HR model using Matlab provides references for the electronic neuron circuit design. The output waveforms of  $x(t)$ ,  $y(t)$ , and  $z(t)$  obtained from Matlab simulations are shown in Figures 2 (b), (c), and (d), respectively.

### B. Circuit Design of the Electronic Neurons

Figure 2 shows the phase relationship between "x" and "y" (a), "x" variable response(b), "y" variable response(c), and "z" variable response(d) in time domain. As shown in the Figure, the output bursts of the neuron are larger than the power supply voltage (2V). Also the output frequency is slower than the real neuron's bursting. For the electronic neuron to work at low power supply voltages, the magnitude and the frequency of the neuron outputs need to be scaled[9][10][11].

The magnitude-scaled and time-scaled variables are defined as

$$x_{new} = \frac{x}{x_{ms}} \quad (4)$$

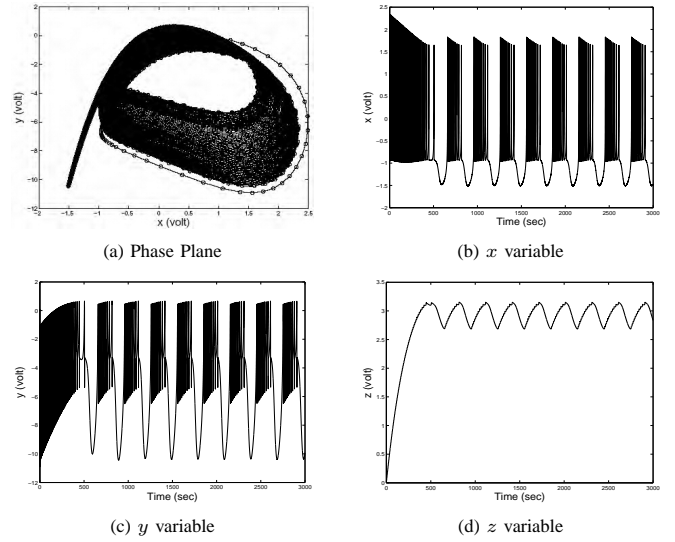


Fig. 2. Solutions of Hindmarsh-Rose Neuron Model

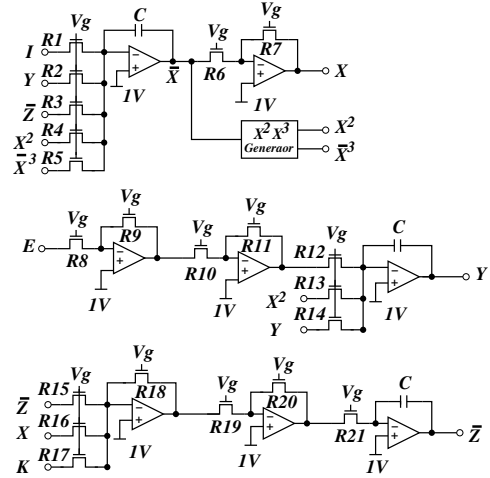


Fig. 3. Hindmarsh-Rose Neuron Circuit

$$y_{new} = \frac{y}{y_{ms}} \quad (5)$$

$$z_{new} = \frac{z}{z_{ms}} \quad (6)$$

$$t_{new} = T_s \times t \quad (7)$$

After these variables are applied to Equation (1), (2), and (3), the following new equations are obtained.

$$\frac{dx}{dt} = \frac{1}{T_s} \left( \frac{y_{ms}}{x_{ms}} y - x_{ms}^2 a x^3 + x_{ms} b x^2 + \frac{1}{x_{ms}} I - \frac{z_{ms}}{x_{ms}} z \right) \quad (8)$$

$$\frac{dy}{dt} = \frac{1}{T_s} \left( \frac{1}{y_{ms}} c - \frac{x_{ms}^2}{y_{ms}} d x^2 - y \right) \quad (9)$$

$$\frac{dz}{dt} = \frac{1}{T_s} \left( r \left( s \left( \frac{x_{ms}}{z_{ms}} x - \frac{x_1}{z_{ms}} \right) - z \right) \right) \quad (10)$$

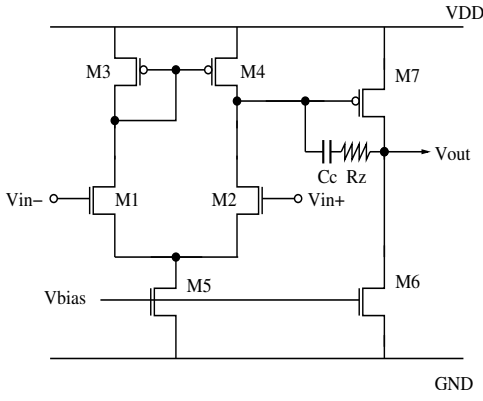


Fig. 4. Two Stage Subthreshold Operational Amplifier

Figure 3 shows the electronic neuron circuit's diagram to implement the Equation (8),(9), and (10) based on the discrete circuit diagram necessary to implement Hindmarsh-Rose model in [5]. These three circuits are connected together through feedback loops where outputs are connected to inputs indicated by the same symbols.  $E$  is the bias voltage to tune the circuit to satisfy the coefficients of the HR model. To integrate the circuits into VLSI on silicon, operational amplifiers, current sources, and multipliers are needed. In addition, MOS Resistive Circuits are required to minimize the silicon area.

Major issues in designing the neuron circuit are area and power consumption due to requirements of a battery-based power supply and the inherent restrictions on mission length. Since the electronic neuron circuit consists of several integrators, low power operational amplifiers are an essential building block.

The two stage operational amplifier architecture shown in Figure 4 is used in this research, where the current source is biased in the subthreshold region to allow subthreshold operation of the op amp [12],[13]. The gain of the two stage operational amplifier is represented by the transconductance of the driver times the load resistance of each stage. The transconductance is given by  $g_m = \frac{I_D}{nV_T}$ , where  $I_D$  is related to the reference current derived in Equation (13) from the current source. Then the gain of the subthreshold op amp can be modified as follows:

$$A_{dc} = \left( \frac{\ln S}{nR_1} \right) (r_{o2} || r_{o4}) \left( \frac{\ln S}{nR_1} \right) (r_{o6} || r_{o7}) \quad (11)$$

where,

$A_{dc}$  is the total gain of 2 stage amplifier,

$r_o$  is output resistance of transistor,

$n$  is slope factor,

$S$  is a current source area ratio  $\left( = \frac{S_3 S_2}{S_1 S_4} \right)$ .

Since the temperature term in  $g_m$  is canceled with  $V_T$  in the Equation (13), the gain is affected only by the temperature slope of the Early Voltage or channel length modulation ( $r_o$ ). Therefore, the gain is relatively constant and independent of temperature and process variations.

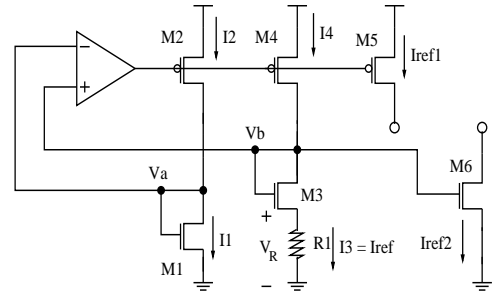


Fig. 5. Current Source Circuit

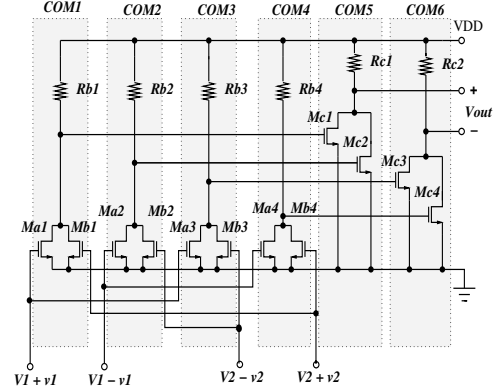


Fig. 6. The Multiplier Core Circuit

The conventional PTAT current source for subthreshold bias shows poor performance due to process variation. A new current source circuit shown in Figure 5 [12],[13] is used to overcome this problem. The process sensitivity of the current source is significantly reduced due to sufficiently large loop gain introduced by the op amp.

The equilibrium voltage  $V_R$  and  $I_{ref}$  is given by

$$V_R = V_T \ln \left( \frac{S_3 S_2}{S_1 S_4} \right) \quad (12)$$

where,  $V_T = \frac{kT}{q}$

$$I_{ref} = \frac{V_R}{R_1} = \frac{V_T}{R_1} \ln \left( \frac{S_3 S_2}{S_1 S_4} \right) \quad (13)$$

From Equation (12) and (13), the temperature coefficient (TC) of  $I_{ref}$  is given by

$$TC = \frac{1}{I_{ref}} \frac{\partial I_{ref}}{\partial T} = \frac{1}{T} - \frac{1}{R_1} \frac{\partial R_1}{\partial T} \quad (14)$$

A Monte-carlo simulation was performed for both conventional and process-insensitive current source circuits, where the reference current is  $500nA$  and  $V_{TH}$ (threshold voltage) is selected as a variable process parameter. The current variation of the circuit in Figure 5 is from  $499.03nA$  to  $501.77nA$ , while the conventional current circuit ranges from  $489.81nA$  to  $519.34nA$ .

The neuron circuit requires a multiplication function to produce square and cubic of variable  $x$ . The multiplier used for the adaptive analog controller is shown in Figure 6. This is an ideal multiplier for the proposed electronic neuron

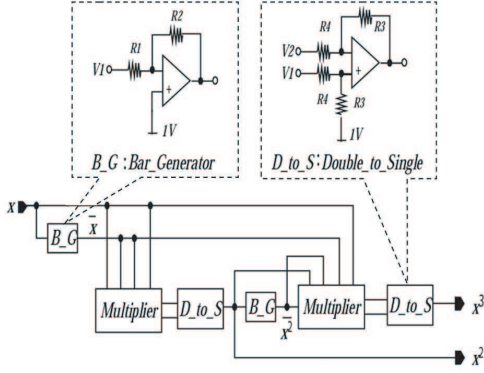


Fig. 7. Square and Cubic generation

implementation because it requires less area and low supply voltage and the output signal integrity is better than other multiplier circuits since it operates in the saturation region [14].

The output of the multiplier is given by,

$$v_{out} = [-32R_c K_c (R_b)^2 K_b K_a (V_1 - V_{TH})(V_2 - V_{TH})] v_1 v_2 \quad (15)$$

To generate  $x^2$  and  $x^3$  terms using this multiplier, additional circuitry shown in Figure 7 is required. The multiplier takes differential inputs and generates differential outputs. output to single-ended output are required. An inverting amplifier denoted as Bar.Generator is used to generate the complementary input signals. To convert the differential output to single-ended output, the difference amplifier with attenuation network denoted as Double.To.Single is used.

$V_{Bar\_Generator}$  and  $V_{Double\_To\_Single}$  are given by:

$$V_{Bar\_Generator} = \frac{R_2}{R_1} v_{in} \quad (16)$$

$$V_{Double\_To\_Single} = \frac{R_3}{R_4} (v_1 - v_2) \quad (17)$$

The resistor ratios  $\frac{R_2}{R_1}$  and  $\frac{R_3}{R_4}$  are set to be unity for both cases. Positive terminals of the operational amplifier are biased at 1 volt since a single rail power supply ( $V_{SS} = GND$  and  $V_{DD} = 2V$ ) is used. The connectivity among the multiplier core circuits including Bar.Generator and Double.To.Single is shown in the Figure 7 and the simulated  $x^2$  and  $x^3$  for a sine wave input  $x$  are shown in the Figure 8. Only  $82\mu\text{watt}$  is consumed to generate  $x^2$  and  $x^3$  due to subthreshold operation.

The size of the resistors and capacitors used in the integrators becomes an issue for VLSI implementation of the Equations (8),(9) and (10). To satisfy the coefficients of the neuron model, either the capacitor values or the resistor values should be larger. Because capacitance takes more area than resistance per square, capacitance values should be fixed as small as possible. Once the capacitance is fixed to a small implementable value, the resistor values are in the order of mega-ohm to satisfy time constants of the differential equations. A single MOS transistor operating in linear region is used to implement the resistor since the linearity is not

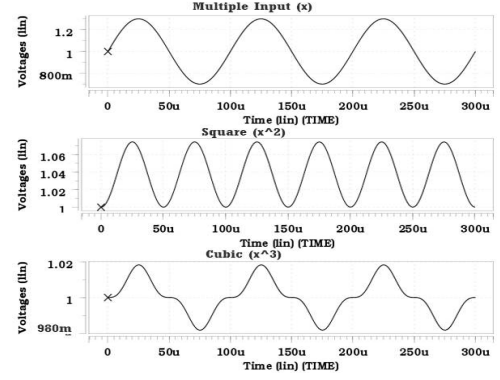
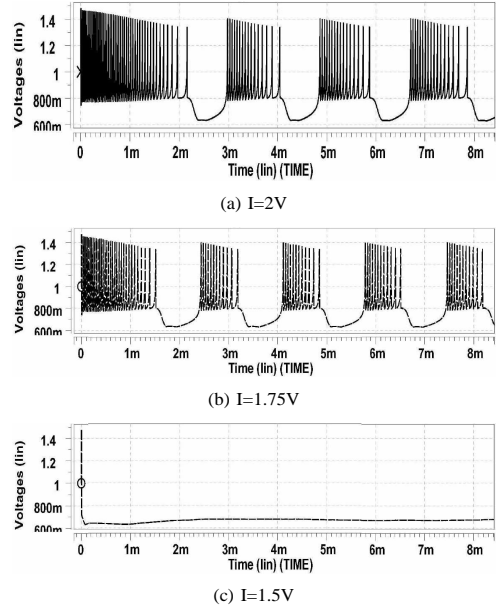
Fig. 8.  $x^2$  and  $x^3$  output waveform

Fig. 9. Neuron Outputs

a critical factor in this application. This single MOS resistor's advantages are: 1) Area is smaller compared to other MRC(MOS Resistive Circuit) [15] that requires at least four MOS transistors. 2) Since all resistors are composed of unit transistor, MOS resistor shows good matching performance. 3) A special process step is not required. The only disadvantage is that it requires high gate voltage ( $V_g$ ), which can be supplied from the external supply.

1) *Simulation Result:* The output waveform of the neuron circuit is shown in Figure 9. In the figure, X axis represents milli-seconds, and Y axis represents voltages. The waveforms of neuron circuit are close enough to the output of the neuronal behavioral(Matlab) simulation except the fact that it is scaled down for integrated circuit. The global behavior depends on the input  $I$ . If  $I$  is lower than the activation threshold (1.5V), the cell stays at rest as shown in Figure 9(c). The cell begins to fire at the higher value of  $I$  than the threshold. The frequency of spikes per burst increases as  $I$  increases as shown in Figure 9(a)  $I=2V$ , and Figure 9(b)  $I=1.75$ .

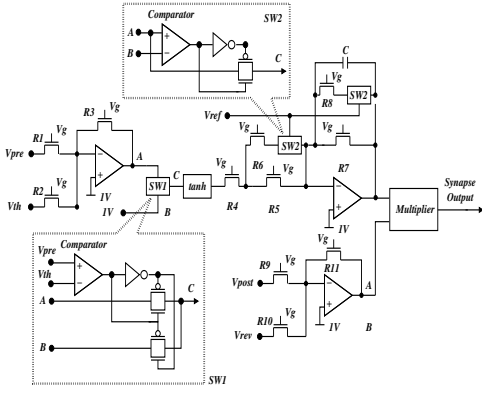


Fig. 10. Electronic Synapse Circuit

### C. Synapse Model

A biological chemical synapse is modeled as in [5]:

$$I = gS(t)(V_{rev} - V_{post}) \quad (18)$$

where,

$$\frac{dS(t)}{dt} = \frac{S_{\infty} - S(t)}{\tau_S(1 - S_{\infty})} \quad (19)$$

$$S_{\infty} = \tanh\left(\frac{V_{pre} - V_{thres}}{V_{slope}}\right) \text{ for } V_{pre} > V_{thres} \quad (20)$$

otherwise,  $S_{\infty} = 0$

- $g$  : maximal synaptic conductance
- $S(t)$  : instantaneous synaptic activation
- $S_{\infty}$  : steady-state synaptic activation
- $V_{rev}$  : synaptic reversal potential
- $V_{pre}$  and  $V_{post}$  : presynaptic and postsynaptic voltages
- $V_{thres}$  : synaptic threshold for transmitter release
- $V_{slope}$  : synaptic slope voltage
- $\tau_S$  : synaptic time constant

Both excitatory and inhibitory synapses are used in the CPG. The topology for these two types of synapse circuits are identical except the value of  $V_{rev}$ , which is selected such that the current injected into the postsynaptic EN is always positive relative to resting potential for excitatory synapses and negative relative to resting potential for inhibitory synapses.

### D. Design of Electronic Synapse Circuit

Based on the Equations (18),(19), and (20), the synapse circuit shown in Figure 10 has been designed. To construct this circuit diagram, operational amplifiers, multipliers, hyperbolic tangent function(tanh), and comparator elements are required. The same operational amplifier and multiplier used for electronic neuron circuit is used for the synapse circuit.

Figure 11 (a) and (b) show the "Tanh" and comparator circuits operating in subthreshold region. An exponential term is required to implement hyperbolic tangent function, and exponential behavior of a MOS transistor can be observed

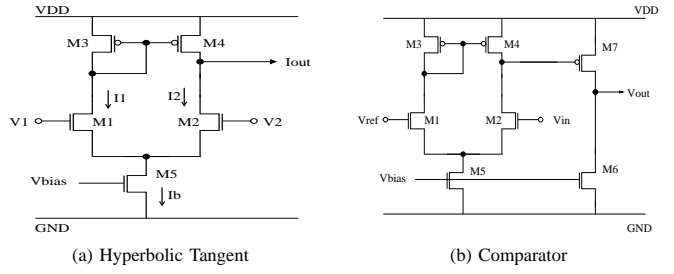


Fig. 11. Subcircuits for Synapse

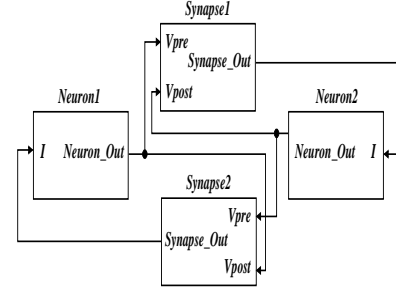


Fig. 12. Neuron Oscillator Block Diagram

in a subthreshold region[16]. Employing a transconductance amplifier operating in the subthreshold region, an output current characterized by tanh function can be obtained for the differential input voltage. This output current is then converted to voltage output using current-to-voltage converter circuit.

The current-voltage relationship of CMOS transistor in the subthreshold region is given by

$$I_{sat} = I_0 e^{kV_g - V_s} \quad (21)$$

where  $k$  is a constant for a given process technology.

The main difference between  $I_1$  and  $I_2$  in Figure 11 can be expressed as:

$$I_1 - I_2 = I_b \frac{e^{kV_1} - e^{kV_2}}{e^{kV_1} + e^{kV_2}} = I_b \tanh \frac{k(V_1 - V_2)}{2} \quad (22)$$

Another circuit required for electronic synapse is analog comparator shown in Figure 11(b) to compare  $V_{pre}$  with  $V_{thres}$  in Equation (20). The design of the comparator is almost identical to that of the proposed operational amplifier. Since the circuit does not have a feedback path and works with open-loop gain for high resolution, signals above  $V_{thres}$  saturate to high supply voltage and signals below  $V_{thres}$  saturate to low supply voltages. A transmission gate shown in Figure 10 is used to pass the original signal if it is higher than the threshold as described in Equation (20). Since the output loading of the comparator is only a parasitic capacitance, the final output driving capability is not an issue.

### E. Neuronal Oscillator Circuit

Figure 12 shows the block diagram of a neuronal oscillator, which is designed to verify the operation of the electronic synapse and EN (Electronic Neuron).

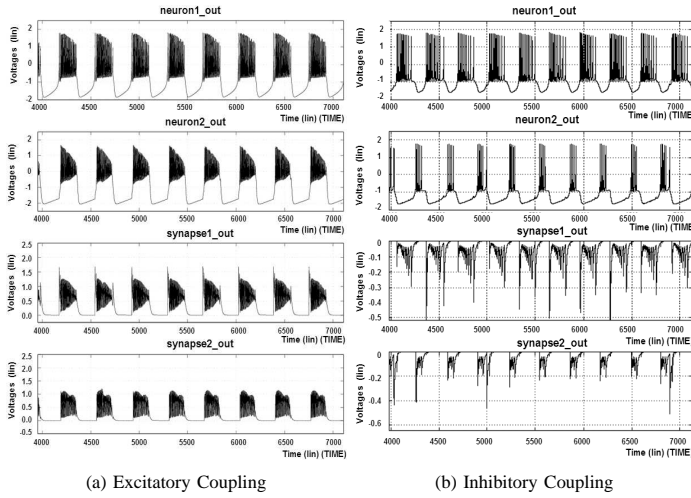


Fig. 13. The Behavioral Simulation Result of Neuronal Oscillator

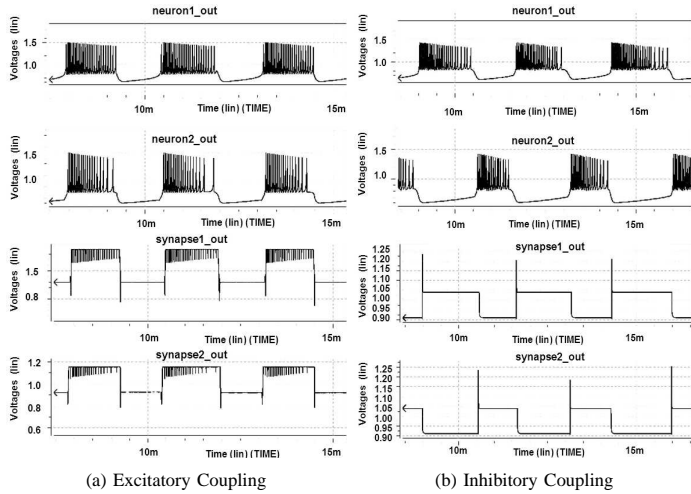


Fig. 14. The HSPICE Simulation Result of Neuronal Oscillator

The coupling of two ENs are connected via two identical synapses. The EN has one input ( $I$ ) and one output ( $Neuron.Out$ ), while the synapse circuits take two inputs: One input is  $V_{pre}$  that comes from the output of the presynaptic neuron and the other is  $V_{post}$  generated by the postsynaptic neuron ( $Synapse.Out$ ). Depending on the type of synapse, neural oscillators produce distinctive characteristics. Output bursts/spikes of two ENs are synchronized for excitatory synapse connections, and become out-of phase for inhibitory synapse connections. The behavioral simulation results of the two coupled neuron circuit, which is based on HR model equations using Matlab, are shown in Figure 13. The HSPICE circuit simulation results are shown in Figure 14 and are verified against the behavioral simulation result.

#### F. Pre-Synaptic Inhibition

Figure 15 shows a circuit diagram of pre-synaptic inhibitory circuit. While the role of synapse circuit is to directly modulate the postsynaptic neuron, the role of pre-synaptic inhibitor is to gate signal propagation from one neuron to another when the

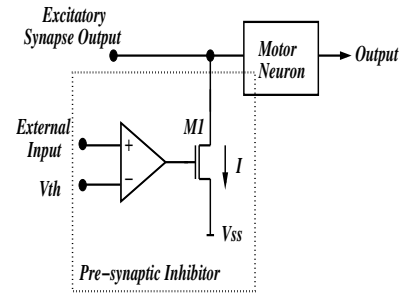


Fig. 15. Pre-synaptic Inhibitor Circuit

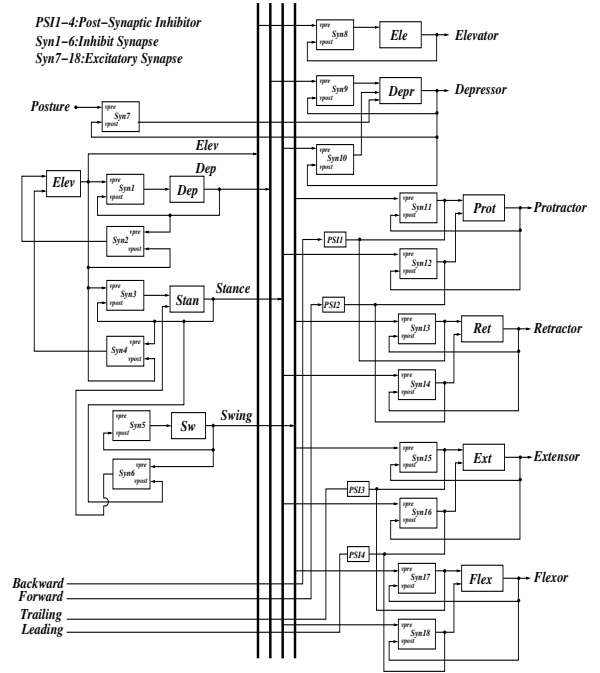


Fig. 16. The CPG Block Diagram

input of pre-synaptic inhibitor is activated. The pre-synaptic inhibitor is an output of the walking command neuron and selects the motor patterns for walking in different directions. Therefore, pre-synaptic inhibitor circuit is implemented using comparator and switch circuit. For example, in Figure 1, if *forward* signal is activated and it is higher than  $V_{th}$ , the output signal of pre-synaptic inhibitor turns on M1 in Figure 15, and the effect of *stance* signal is nullified by pre-synaptic circuit. Finally, output of protractor neuron is synchronized with *swing* signal. On the contrary, if *backward* signal is activated, the output of protractor neuron is synchronized with *stance* signal.

#### IV. ELECTRONIC CPG CIRCUIT AND ITS SIMULATION RESULT

Figure 16 shows the complete block diagram of CPG circuit. The simulation results of this circuit are shown in Figure 17 and 18. The waveforms shown in Figure 17 and 18 are *elev*, *dep*, *swing* and *stance* from the 4 state neuronal oscillator circuit, elevator, depressor, protractor, retractor, extensor, and flexor corresponding to the output signals

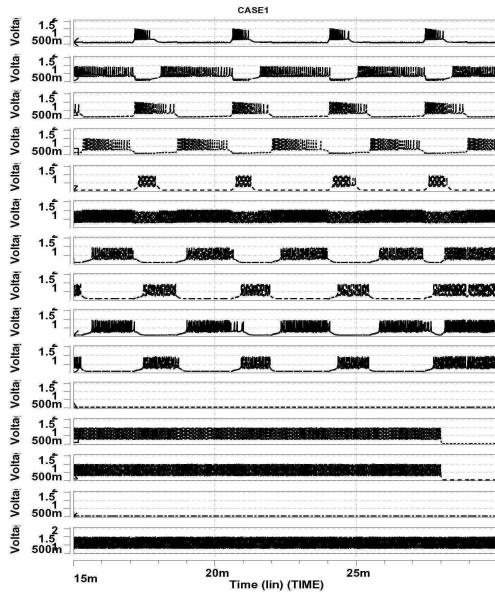


Fig. 17. Case I: *Forward* and *Leading* are off. *Backward*, *Trailing* and *Posture* are on.

of CPG, and *forward*, *backward*, *trailing*, *leading* commands as the input signals. For case1, protractor/retractor is synchronized with *stance/swing* by the *backward* command, and extensor/flexor is synchronized with *stance/swing* by the *trailing* command. In this case, *forward* and *leading* signals are off. This motor program corresponds to diagonal walking. The output of the depressor is due to the summation of the *dep*, *posture* and *stance* inputs. On the contrary, protractor/retractor is synchronized with *swing/stance* by the *forward* command, and extensor/flexor is synchronized with *swing/stance* by the *leading* command in case2. (the *backward* and *trailing* commands are off.)

## V. CONCLUSION

An electronic CPG circuit using 2V power supply is implemented using  $0.25\mu\text{m}$  CMOS technology. The electronic CPG is able to mimic the nervous system behavior of biological CPG. Each building block is designed and optimized for low power and minimum area. The total power consumption of  $4.8\text{mW}$  is obtained from HSPICE simulation and its layout dimension is  $2.2\text{mm}$  by  $2.2\text{mm}$  including I/O pads. Simulated results show that the CPG circuit with coordinate controller and command neuron is viable to build adaptive analog controller for autonomous biomimetic underwater robots.

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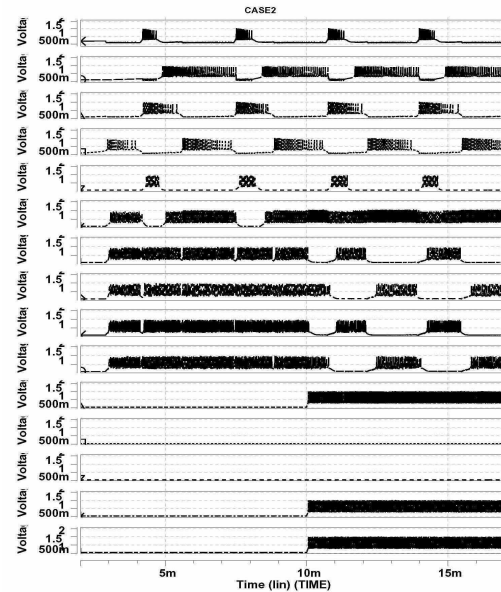
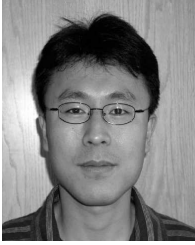


Fig. 18. Case II: *Backward* and *Trailing* are off. *Forward*, *Leading* and *Posture* are on.

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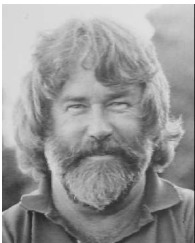
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