

Load Board Designs Using Compound Dot Technique and Phase Detector for Hierarchical ATE Calibrations

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Abstract

This paper presents two load board designs for hierarchical calibration of largely populated ATE. Compound dot technique and phase detector are used on both boards to provide automatic and low cost calibration of ATE with or without a single reference clock. Two different relay tree structures are implemented on the two boards with advanced board design techniques for group offset calibration. Various error sources have been identified and analyzed on both boards based on SPICE simulations and real measurements. TDR measurement compares the two approaches and shows that the two load boards give a maximum of 37ps group timing skew and can be calibrated out by the calibration software.

1. Introduction

Today's IC test systems have achieved 1024 tester pins per testhead in Gigahertz frequency, and more pins will be available in near future. This brings a challenging calibration problem of aligning all the pins to the same drive edge and the compare edge. It is impossible, however, to build a RF relay matrix for every pin to be able to align with a common reference, because it costs too much to implement in reality. One simple, yet accurate pin-to-pin calibration technique presented by Kikuchi [1] in 1995 is to use a compound dot that ties all its 384 tester pins together so that the compound pulse generated by all the tester pins, except the target pin, can be used as the common reference to calibrate the target pin.

The gate-array-based tester in [1] can work up to 666 MHz frequency and expendable to 1024 pins. However, for such a high pin population system, users may not populate all the pins on the testhead. Therefore, the compound dot that ties 1024 pins may be driven in reality by much fewer pins, and the system may not be accurate enough in such cases. On the other hand, for higher tester frequency, the compound pulse may not be sharp enough to satisfy the faster rise/fall time requirements for the reference. This is because the compound dot is relatively too big and capacitive as the timing requirement goes higher if there are still 384 or more pins tied on the dummy load board, which is called calibration load board in this paper. Therefore, for a test system that has large number of pins and works at Gigahertz frequency, pin group partitioning must be developed to conveniently configure the system and to use the compound dot technique for fast and low cost ATE calibration.

LTX has been using 16 64-pin groups for its 1024-pin single-platform test systems. It is believed that the average of 64 pins can give enough accuracy, while users can populate the system with an increment of 64 pins. Within each pin group, pin-to-pin calibration is based on Kikuchi's compound dot technique. Among the 16 pin groups, there are group offsets that are calibrated out by a relay chain structure. The 64th pin in a group aligns the compound pulse driven by the remaining 63 pins of the group with the timing of the next adjacent group.

Along the relay chain, all the pin groups can be aligned with respect to each other so that hierarchical calibration is achieved.

However, there are 16 different measurement pins and the measurement pin skews are accumulated along the relay chain. Even though the calibration can start from the middle of the chain with double directions to both ends, there are still 8 accumulations. To get rid of the accumulated error, a common time measurement unit with a capability to measure any individual group must be developed. A relay tree can be a good replacement for the relay chain. For time measurement, Feldman [2] has presented an analog phase detector that has shown good linearity and jitter rejection. In this paper, instead of designing a phase detector, an On-Semi ECL differential phase detector is used for time measurement of the group offsets. Two load boards with different relay tree structures are designed for group offset calibration.

This paper is organized as follows: Section 2 describes the pin group partitioning, relay structures for group offset calibration, time measurement using the phase detector, and board design issues. Section 3 presents measurement results of timing skews for both boards. Error sources such as the timing difference between relay contacts, through-hole via reflection, and dielectric variation are also analyzed in Section 3. The limitation of the proposed methods is discussed in Section 4 followed by conclusions in Section 5.

2. Load board design for hierarchical calibrations

2.1. Compound dot capacitance

Assuming there are n pins with ground shields tied together by a compound dot as shown in Fig. 1-1, all traces and dots should be in a stripline structure since there are not enough space for all of them on the top and bottom layers and they have to be in the same physical structure for the least timing skew.

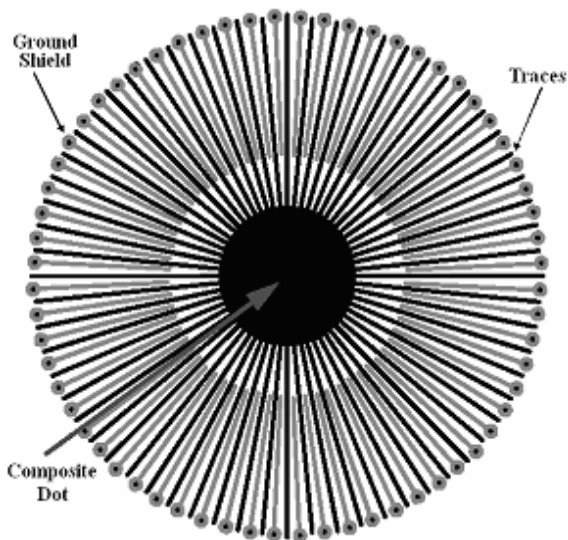


Figure 1-1. Compound dot



Figure 1-2. Zoomed dot edge

Figure 1-2 shows the zoomed dot edge. Let w and d denote the trace width and the space between traces at the edge, respectively. So the radius r and the area A of the dot are:

$$r = \frac{n(w+d)}{2\pi}, A = \pi r^2 = \frac{n^2(w+d)^2}{4\pi} \quad (1)$$

Assume board dielectric thickness between the dot layer and the ground plane is t . If w, d, t are all kept the same as n increases in order to keep signal integrity, the capacitance of the dot can be calculated by the parallel plate capacitance C_p plus the fringe capacitance C_f from the dot edge.

$$C_{dot} = C_p + C_f = 2 \frac{\epsilon_r \epsilon_0 A}{t} + 2 C_{fo} n d \quad (2)$$

$$\Rightarrow C_{dot} = \frac{\epsilon_r \epsilon_0 n^2 (w + d)^2}{2 \pi t} + 2 C_{fo} n d \quad (3)$$

where C_{fo} is the unit length fringe capacitance, which can be calculated based on the transmission line theory. Note that both the parallel plate and the fringe capacitances are doubled because of the stripline structure.

At high frequency, the transmission line capacitance per unit length is a function of its characteristic impedance and the velocity and given by $C_{TL} = 1/(Z_0 v_p)$, where $Z_0 = 50\Omega$, $v_p = c/\sqrt{\epsilon_r}$, and c is the number of the unit lengths that light transmits in vacuum. On the other hand, the total capacitance of a transmission line is equal to the parallel capacitance plus the fringe capacitance. Therefore, the fringe capacitance can be estimated by the difference between the transmission line capacitance and the parallel plate capacitance of the unit length transmission line with width w :

$$C_{fo} = \frac{1/(Z_0 v_p) - \epsilon_r \epsilon_0 w/t}{2w + 2} \quad (4)$$

Plug Eq. (4) into Eq. (3), we can get the compound dot capacitance:

$$C_{dot} = \frac{\epsilon_r \epsilon_0 n^2 (w + d)^2}{2 \pi t} + \frac{1/(Z_0 v_p) - \epsilon_r \epsilon_0 w/t}{w + 1} n d \quad (5)$$

2.2. Pin group partitioning versus compound pulse rise time

The first and the most important calibration step using the compound dot is to calibrate the compare edge of the target pin. In such case, there are $n - 1$ pins driving the dot. It is assumed that the compound pulse is identical to all target pins as long as n is large enough. Figure 2 shows the compare edge calibration diagram. The comparator of the target pin is able to identify the edge of the compound pulse which could have elongated rise and fall time in reality since every single pulse may not be aligned with each other before the calibration.

To properly partition the pin groups, assuming all the $n - 1$ pins drive at the same time, this will give the fastest compound pulse rising edge to the comparator. So the compound pulse rise time is:

$$t_r = 2.2 RC = 2.2 \frac{50}{n - 1} C_{dot} \quad (6)$$

For a 1024-pin tester, Table 1 calculates the capacitance of the compound dot using Eq. (5) and the rising time using Eq. (6) as a function of n , where $w = d = 5 \text{ mils}$, and $t = 10 \text{ mils}$.

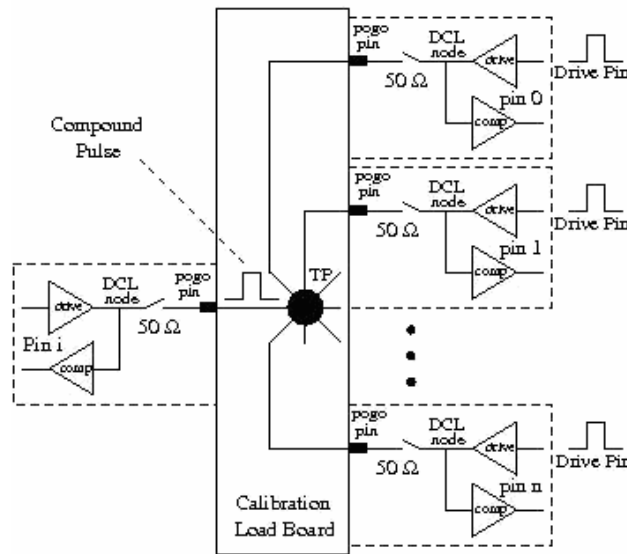


Figure 2. Compare edge calibration

Table 1. Compound dot capacitance and compound pulse rise time versus n

# of pins tied (n)	32	64	128	256	384
Compound Dot Capacitance (pF)	1.2	5.0	19.9	79.8	179.5
Compound Pulse Rise Time (2.2 RC) (ps)	4.4	8.7	17.3	34.4	51.5

2.3. Relay tree structures for group offset calibration

Figure 3 shows the binary relay tree structure designed for the 64-pin group calibration. There are two 3-layer sub binary trees with even and odd number groups associated with each tree. Even number groups can be aligned with odd number groups and vice versa. So there is only one accumulation for aligning all 16 groups. This group offset calibration scheme is called binary relay tree alignment without a common reference clock.

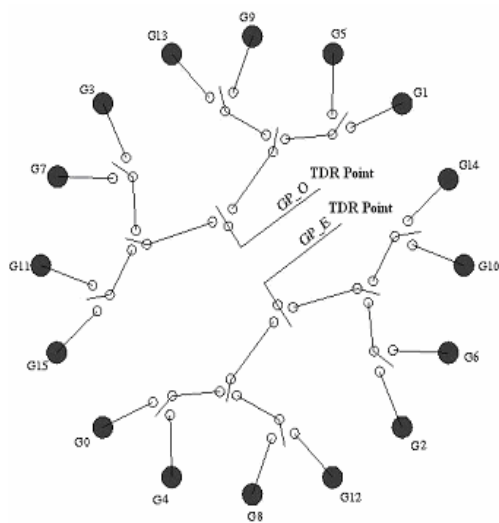


Figure 3. Binary relay tree

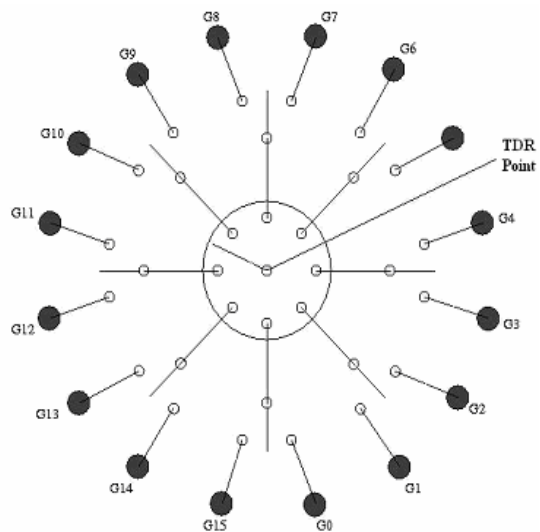


Figure 4. Central relay tree

The two sub-trees can be connected by another relay to make a 4-layer binary tree. Then each group can be compared with a common reference clock so that there is no accumulation if the timing for every relay and every contact of the relay is exactly the same. This scheme is called binary relay tree alignment with a common reference clock. 0402 size jumpers are designed on the board to switch between the two calibration schemes.

Figure 4 shows a central relay structure, where any group can be switched and compared with a common reference. For both structures, Teledyne DPDT SMT relay with ground shield, GRF103, is chosen as the 2-to-1 relay. A normally open 8-to-1 switch with SMA-female connectors from Dowkey Microwave, 571a, is used to build the central relay structure.

Both relay tree structures can be evaluated by the Voltage Standing Wave Ratio (VSWR). For frequencies less than 3.5GHz and the 4-layer binary relay tree, the minimum VSWR would be 1, and the maximum VSWR can be calculated by [3][5]:

$$VSWR_{\max}^{Binary\ Relay\ Tree} = VSWR_{GRF103}^4 = 1.11^4 = 1.518 \quad (7)$$

For the central relay tree, according to [3][6], the VSWR range is:

$$VSWR_{\min}^{Central\ Relay\ Tree} = \frac{VSWR_{571a}}{VSWR_{GRF103}} = \frac{1.2}{1.11} = 1.081 \quad (8)$$

$$VSWR_{\max}^{Central\ Relay\ Tree} = VSWR_{571a} \times VSWR_{GRF103} = 1.332 \quad (9)$$

Comparing with the binary tree relay structure, the central relay structure has better signal integrity due to less VSWR range since it has only two layers. However, the central relay costs more than the 2-to-1 relay and has shorter mechanical life.

2.4. Phase detector and calibration loop

On-Semi MC100EP40 phase detector is used to align groups. It compares the compound pulse from the target group with a common reference or another group. The output of the phase detector is then filtered and converted to a DC voltage and measured by the calibration software which tunes the pin cards in the target group to make the phase detector output to be zero. The diagram is shown in Figure 5.

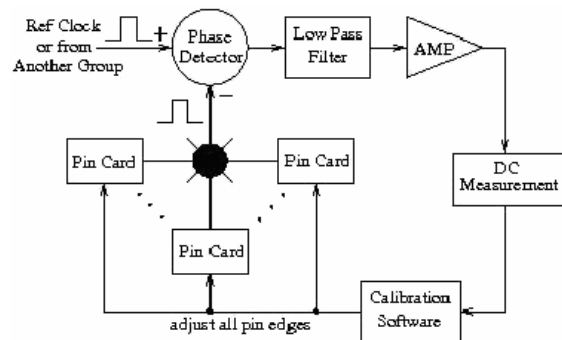


Figure 5. Group offset calibration using phase detector

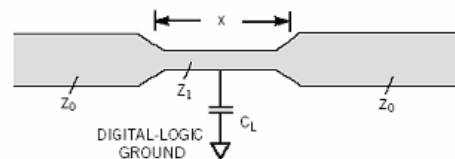


Figure 6. Skinny line with load capacitance

2.5. Board design techniques

2.5.1. Skinny line technique: Skinny Line has been used by high speed design engineers to compensate pad capacitance. A skinny line has a bigger inductance than a regular one so

that it can compensate load capacitance. The diagram of a skinny line is shown in Figure 6. By choosing the characteristic impedance Z_1 of the skinny line and the length x , the total effective characteristic impedance can be equal to Z_0 . Given Z_1 , x is calculated by [4]

$$x = \frac{Z_0 C_L}{\tau} \frac{k}{k^2 - 1} \quad (10)$$

where $Z_1 = Z_0 k$, and τ is the transmission line delay with an impedance of Z_0 .

2.5.2. Compound dot stack-up: Two calibration load boards, GOLB1 and GOLB2 are designed to implement the binary relay tree and the central relay tree structures, respectively. On each board, there are 16 pin groups, each of which ties 64 pins. For layout considerations, the compound dots are stacked up on each other on 4 layers as shown in Figure 7. There are ground planes between the signal layers. Traces that connect the pogo pins with their group are on the same layer as the group, and all other high speed signals run on the top layer.

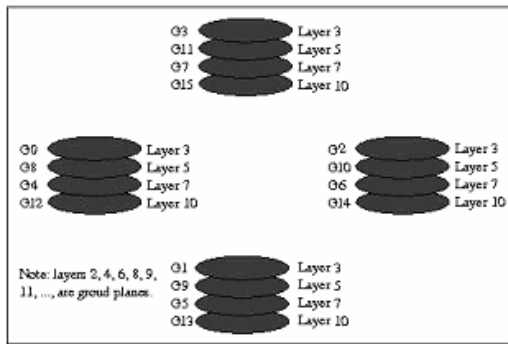


Figure 7. Compound dot stack-up

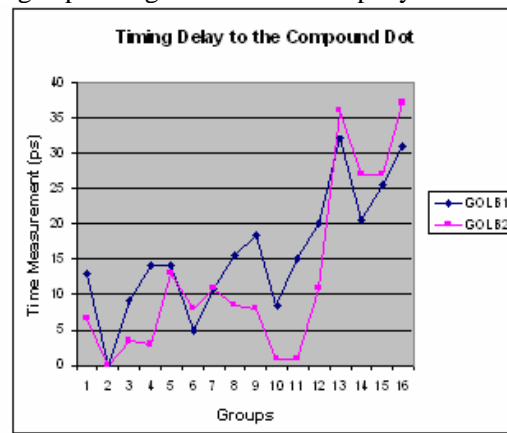


Figure 8. Group timing skew for GOLB1 and GOLB2

2.5.3. Back-drilled via: Each group use a via to connect itself inside the board to the top layer relay. In order to reduce the reflection due to the through-hole stub, it is back-drilled.

3. Measurement results

3.1. Timing skews on GOLB1 and GOLB2

Time Domain Reflection (TDR) measurement is used quite often to measure and evaluate the timing skew on PCB boards, and the measurement results can be applied to the calibration software to remove the skew. We have calibration software that enables automatic TDR measurements from the pogo pins to the compound dots, but not from the other side, i.e., from the compound dots to the phase detector.

Even though we have matched traces, there are still timing skews from the compound dots to the phase detector and they should be measured and evaluated for both GOLB1 and GOLB2 boards. This is done by TDR measurement using an external instrument from the points shown in Figure 3 and Figure 4 for both boards. The measurement results are plotted in Figure 8. Except for the last 4 groups G12-G15 that are on layer 10, GOLB2 shows a better performance than GOLB1. The error sources are analyzed in the following subsections.

3.2. Path length difference between normally closed and normally open relay contacts

Path length difference may exist in the Teledyne 2-to-1 GRF103 relay between Normally Closed (NC) and Normally Open (NO) contacts. Timing skew between NC and NO of GRF103 is observed in SPICE simulations based on the manufacturer-provided relay S-parameters. For SPICE simulation of the relay contacts, the relay S-parameter matrix is converted to a PSPICE model by EMTToSpice software [7]. However, the trace length skew on the manufacturer's test board was found and it is included in the S-parameters. Therefore, SPICE simulation itself does not provide information about how much length difference between NC and NO contacts is, but it did help design engineer focus on the problem.

Figure 9 shows the TDR setup on GOLB1 board for measuring the timing skew between NC and NO contacts. The traces on the board are 12-mil width and length matched. The timing skew between relay contacts is compared within the same pole of a relay. There are 8 TDR measurements from P1 to pads K6.1, K6.7, K5.7, K5.1, and from P2 to K1.1, K1.7, K2.1, K2.7. Four comparisons between NC and NO contacts are made and shown in Table 2.

The measurement results show that the NO contract, when energized to close, has a longer timing delay than the NC contact. This is probably because of the square structure of the relay. According to Table 2, the average timing skew between NC and NO contacts is 7.6ps.

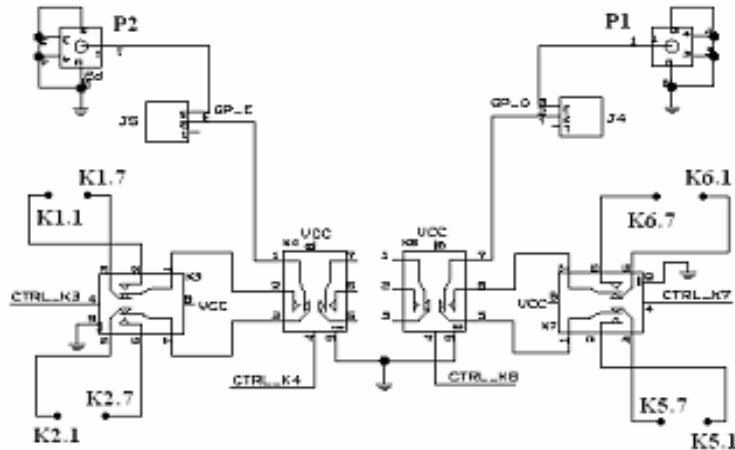


Figure 9. TDR setup for measuring timing skew between relay contacts

Table 2. GRF103 timing skew between NO and NC contacts

Contract Pair	(K1.1, K1.7)	(K2.7, K2.1)	(K5.1, K5.7)	(K6.7, K6.1)
Measured Timing Skew (ps)	8.75	6.25	7.5	8.0

For GOLB1 board, there could be 3 or 4 relays linked together depending on the usage of a common reference. So the maximum timing skew from P1/P2 to the groups due to the path length difference between relay NC and NO contacts is $3 \times 7.6ps = 22.8ps$ for odd and even group offset alignment and $4 \times 7.6ps = 30.4ps$ for alignment using a common reference. For GOLB2 board, there is only one binary relay layer, so the timing skew due to the path length difference between relay NC and NO contacts is 7.6ps.

Figure 10 shows the TDR measurements for all even number groups on GOLB1 board. The second last peak of a curve is when the TDR signal hits the via that connects the top layer trace to the group. So the total timing skew due to relays and traces on the top layer should be located right before the second last peaks. About 40ps TDR timing difference is observed in the figure among the 8 even number groups, so there is about 20ps timing difference among the paths and it is very close to the calculation of 22.8ps.

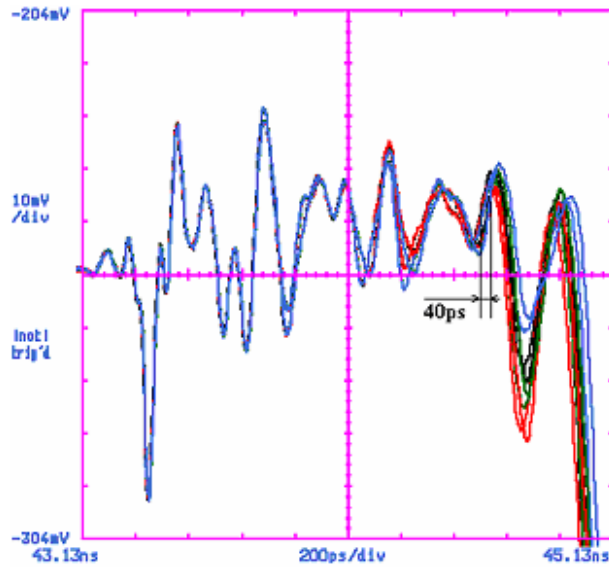


Figure 10. TDR measurements on even groups on GOLB1

3.3. Through-hole via reflection

For the vias that connect the groups inside the board to the top layer relays, GOLB1 used through-hole vias, while GOLB2 had these vias back-drilled to eliminate the reflection on the through-hole via stubs. Figures 11 and 12 show the TDR waveforms of G1, G9, G5, and G13 for GOLB1 and GOLB2, respectively. Note that the 4 compound dots for G1, G9, G5 and G13 are stacked up on each other on layers 3, 5, 7, and 10, respectively. Increasing capacitive effect is observed from G13 to G1 on GOLB1, indicated by label 1 in Figure 11 as the through-hole stub becomes longer. There is no such clear effect on GOLB2 in Figure 12.

3.4. Dielectric variation

There is longer timing delay for the compound dots on layer 10 than those on other layers for both boards. Figure 11 and Figure 12 show this longer delay for G13, one of the dots on layer 10. As indicated by label 2, it is observed that there is about 40ps longer TDR delay for G13 on both boards than G1, G9, G5 that are not on board layer 10. Our data show that all the dots from G12 to G115 on layer 10 suffer the same longer delay on both boards.

Since the delay is added to the TDR waveform after the last peak where the TDR waveform hits the dot, it is believed that the delay is brought by dielectric thickness or the dielectric constant variation since the compound dots are identical in design.

4. Limitations

One assumption from the compound dot technique is that when the target pin is switched, the compound pulse driven by the remaining $n - 1$ pins is identical. However, the timing difference due to switching the target pin would be brought to the compound pulse and shared by all the remaining $n - 1$ pins. So, it is necessary either to choose a bigger n , or to have the calibration iterate multiple times as suggested by [1].

All the error sources discussed above, except the manufacture process, could be reduced or avoided by choosing better parts and better designed board. For example, round shape

GRF303 could be a better replacement for GRF103. In some cases, however, the timing error due to board dielectric variation could be the largest. Therefore, timing skew needs to be measured for every board from the input of the phase detector to the compound dot edge. TDR measurement is still a good way, but either an external instrument is needed, or it is done automatically by the calibration software by a pin with some other relay switching logic.

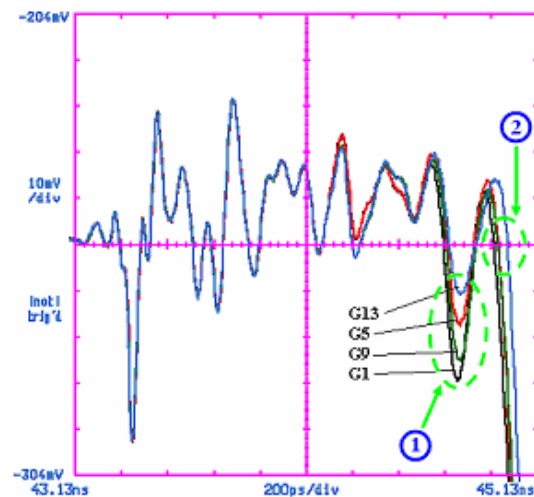


Figure 11: TDR measurements for G1, G9, G5, and G13 on GOLB1

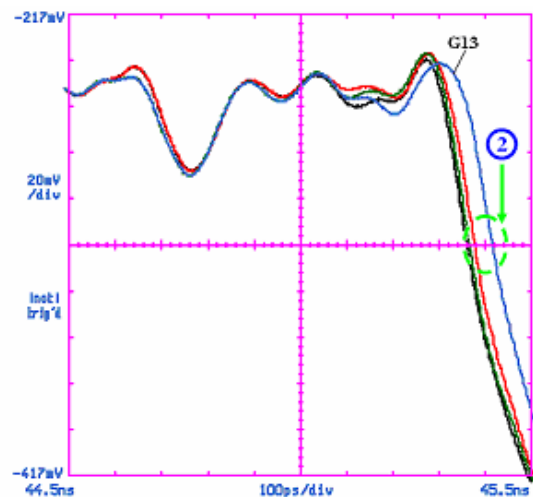


Figure 12: TDR measurement for G1, G9, G5, and G13 on GOLB2

5. Conclusions

In conclusion, we have been using the compound dot technology to align our 1024-pin testers with minimum relay matrix, minimum cost, and the requirement for the external robot or reference clocks. The phase detector works very well as long as each group is time shifted to cause the same phase detector output voltage. Experimental data show that GOLB1 does not have to use an external reference clock, while GOLB2 has to use one. But GOLB2 will provide a better solution if GOLB1 is configured to align with a common reference clock by connecting the two sub-trees with another 2-to-1 relay. Both boards together, based on the measurement given in Figure 8, provide a maximum of 37ps timing skew and it could be calibrated out if the measurement results in Figure 8 are used as the calibration factors.

6. Acknowledgements

Thanks to Mike Bruno, Wai-Kong Chen, Michael Davis and all other LTX fellow engineers for helpful discussions and suggestions to this project.

7. References

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