

A Fully Integrated Switched-Capacitor DC-DC Converter with Dual Output for Low Power Application

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ABSTRACT

This paper presents a fully integrated on-chip switched-capacitor (SC) DC-DC converter that supports two regulated power supply voltages of 2.2V and 3.2V from 5V input supply and delivers the maximum load currents up to 8mA at both of the outputs. The entire converter system uses two 2-to-1 converter blocks. The upper output voltage (3.2V) is generated from the 2-to-1_{up} converter by means of averaging the 5V input and the generated lower output voltage (2.2V), which is generated from 2-to-1_{dw} converter. Since 2-to-1_{up} converter is less sensitive to the bottom-plate parasitic capacitance loss, they are implemented with MOS capacitors, which show higher capacitance density ($2.7\text{fF}/\mu\text{m}^2$, $\alpha=6.5\%$) than MIM capacitors ($1\text{fF}/\mu\text{m}^2$, $\alpha=2.5\%$) while they have bigger bottom-plate parasitic capacitance ratio (α). The proposed implementation saves the area and quiescent currents for the control blocks since each block shares required analog and digital control blocks. The proposed converter is designed using high-voltage $0.35\mu\text{m}$ BCDMOS technology. Both output voltages are regulated by means of pulse frequency modulation (PFM) technique using 18-bit shift registers and digitally controlled oscillators (DCOs). Over the wide output power ranges from 5.4mW to 43.2mW, the converter achieves the average efficiency of 70.0% and the peak efficiency of 71.4%. 10-phase interleaving technique enables the output voltage ripples of the both outputs less than 1% ($<40\text{mV}$) of the output voltages when 400pF of output buffer capacitors are used for both outputs.

Categories and Subject Descriptors

B.7.0 [Integrated Circuits]: General

Keywords

Dual Output, Switched-Capacitor, DC-DC Converter

1. INTRODUCTION

The use of multiple supply voltages on a single chip has become very common due to the coexistence of low/high power digital circuits and analog/RF circuits in recent integrated systems. It is not desirable approach to add multiple high-efficiency off-chip DC-DC converters, which are mostly implemented with off-chip inductors, for generating multiple output voltages due to the increased cost/size, the degraded of supply impedance, and the

limited allowance for power pins. Since the integrated voltage regulators are cost and size effective and show fast load-transient response, integrating voltage conversion blocks on the silicon chip is a very attractive approach. Linear regulators have been widely used for on-chip DC-DC converters. However, the most significant drawback of linear regulators is their linear efficiency drop with increasing dropout voltage. Therefore, the alternatives are required to achieve high efficiency across a broad range of output voltages. Since the on-chip capacitors have significantly higher quality factor, higher energy density, and lower cost than on-chip inductors in standard CMOS process, SC based on-chip converter have been receiving increased attention from both academia and industry [1-5].

In this paper, a novel design technique, supporting two regulated output voltages (2.2V and 3.2V) out of 5V input at the maximum load currents up to 8mA, is proposed and designed using high-voltage $0.35\mu\text{m}$ BCDMOS technology. Two types of flying capacitors (MIM and MOS Capacitors) are used to maximize the power density and efficiency at the limited area. The proposed architecture uses closed-loop feedback control scheme by means of digitally controlled pulse frequency modulation (PFM) to regulate output voltage in the wide range of load current levels. Two sets of four dynamic comparators are used compare four reference voltage levels with the scaled output voltages to determine the mode of control. Top and bottom voltage levels are used for fast startup and fast transient response of the varying output load current while two intermediate levels are used for stably locking the output voltage. Section 2 presents the core design of proposed dual output converter in terms of operating principle and charge transfer and loss mechanisms. System architecture and simulation results are presented in Section 3 and Section 4, respectively. The paper is finally concluded in Section 5.

2. PROPOSED CORE DESIGN

2.1 Operating Principle

In general, a SC DC-DC converter consists of capacitors and switches driven by two non-overlapped clock signals. Each of signals is set as close as 50% duty cycle with a minimal dead-time (different phased ϕ_a and ϕ_b switches, as shown in Figure 2(c), are never closed at the same time) for the maximum efficiency and the maximum charge transfer to the load.

As shown in Figure 1, the proposed dual output topology is made in combinations of the two conventional 2-to-1 topologies. Conventional 2-to-1 topology in Figure 1 (a) can be symbolized as shown in Figure 1 (b), which has two input terminals and one output terminal. To present the loss due to bottom-plate parasitic capacitors, the bottom-plate parasitic capacitance C_{BP} is modeled as $C_{BP}=\alpha C$, where C is the actual capacitance and α is the process and layout dependent parameter. For an ideal operation, the output

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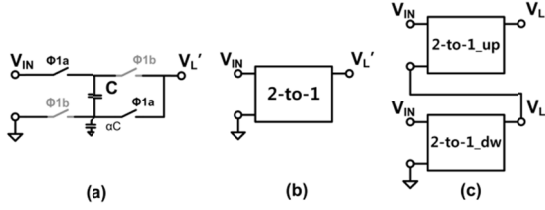


Figure 1 (a) Conventional 2-to-1 step-down topology (b) Simplified block diagram (c) Proposed 4-to-3 step-down topology

terminal produces the average voltage between the two input voltages. In the same way, new 4-to-3 topology is formed. That is, one input terminal of the 2-to-1_{up} is fed directly from the input (V_{IN}) and the other terminal is fed out of the output (V_L') of the 2-to-1_{dw} block. Therefore, the generated output voltage V_L ($= (V_{IN} + V_L')/2 - \Delta V_L$) is the average value of V_{IN} and V_L' ($= 1/2V_{IN} - \Delta V_L$). ΔV_L and $\Delta V_L'$ represent the voltage difference of the delivered output voltages when there is load and there is no load. ΔV_L and $\Delta V_L'$ arise from the fundamental conduction loss and they limit the maximum attainable efficiency to $\eta_{lin} = V_L' / (1/2V_{IN})$ for 2-to-1_{dw} and $\eta_{lin} = V_L / \{(V_{IN} + V_L')/2\}$ for 2-to-1_{up}. Figure 2 shows the transistor level implementations of the 2-to-1_{dw}(up) blocks and their gate driving signals. Since the breakdown voltage of MOS transistors is 5.5V, all switches can withstand any voltage levels between 0V and input (5V). All the gate driving signals in Figure 2 are generated from level shifter and non-overlap clock generator blocks in Figure 5 to minimize the switching loss and shoot-through current loss. Upper NMOS transistors are implemented by means of a triple-well device to isolate the voltage from the substrate.

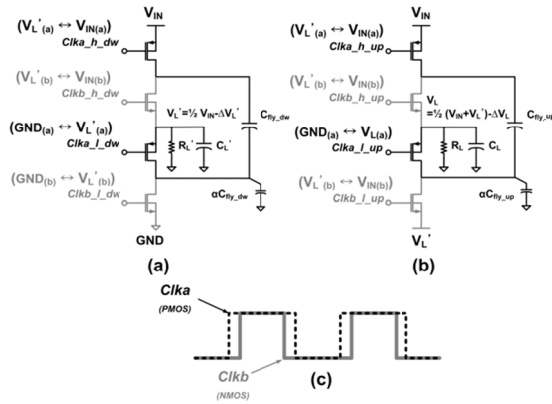


Figure 2 Transistor level implementation of the converter core; (a) 2-to-1_{dw} (b) 2-to-1_{up} (c) Non-overlap clock signals

2.2 Charge Transfer and Loss Mechanisms

Figure 3(a) shows 2-way interleaved structure, where ϕ_{1a} (ϕ_{1b}) and ϕ_{2a} (ϕ_{2b}) are 180° out of phase signals while ϕ_{1a} (ϕ_{2a}) and ϕ_{1b} (ϕ_{2b}) represent non-overlapping clock signals as shown in Figure 2(c). Figure 3(b) represents equivalent circuit during each half cycle of the clock. Assuming that those blocks deliver charges to the load capacitors at DC voltage V_L' and V_L , the charge extracted from the input voltage source (Q_{EXT}) during each half cycle of the clock (ϕ_{1a} and ϕ_{2b} are on) can be derived by

$$Q_{EXT} \approx \frac{C_{up}}{2} \{(V_{IN} - V_L) - (V_L - V_L')\} + \frac{C_{dw}}{2} \{(V_{IN} - V_L) - V_L'\}$$

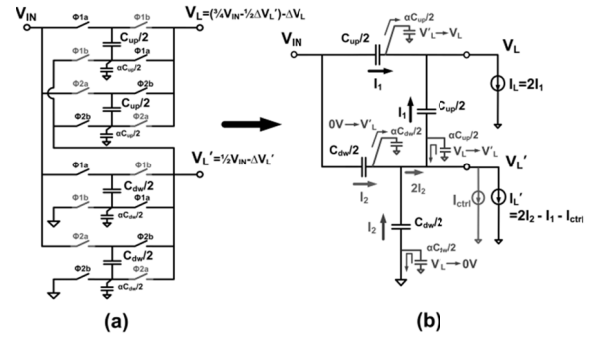


Figure 3 Proposed dual output topology with 2-way interleaved structure to provide voltages of V_L' ($\approx 2.2V$) and V_L ($\approx 3.2V$) out of V_{IN} ($= 5V$) input.

$$Q_{EXT} \approx Q_{EXT(up)} + Q_{EXT(dw)} = C_{up}(\Delta V_L) + C_{dw}(\Delta V_L') \quad (1)$$

where $V_L = (3/4V_{IN} - \Delta 1/2V_L') - \Delta V_L$ and $V_L' = 1/2V_{IN} - \Delta V_L'$.

Since the total charge delivered to the each load is the sum of the charge transferred from both top and bottom $C_{up}/2$ ($C_{dw}/2$) capacitors as shown in Figure 3(b), the total charge transferred to the load can be derived by

$$Q_L + Q_L' \approx 2Q_{EXT}(VIN) \approx 2C_{up} \left\{ (2.5V + \frac{V_L'}{2}) - V_L \right\} + 2C_{dw}(2.5V - V_L') \quad (2)$$

Since the efficiency for each output can be defined as $Q_L V_L / Q_{EXT(up)} V_{IN}$ and $Q_L' V_L' / Q_{EXT(dw)} V_{IN}$, this again sets the fundamental efficiency limitations of $V_L' / 2.5V$ for the 2-to-1_{dw} and $V_L / (2.5V + V_L' / 2)$ for the 2-to-1_{up}.

Besides of the conduction loss, the loss due to the bottom-plate parasitic capacitor is significant and has to be considered. In our design, MIM capacitors ($1fF/\mu m^2$) and MOS capacitors ($2.7fF/\mu m^2$) are used, and the bottom plate capacitance ratios (α) were assumed 2.5% for MIM capacitors and 6.5% of MOS capacitors. During every half cycle, each top bottom-plate capacitor $\alpha C_{up}/2$ ($\alpha C_{dw}/2$) is charged to V_L (V_L'), while each bottom bottom-plate capacitor $\alpha C_{up}/2$ ($\alpha C_{dw}/2$) is discharged to V_L' (GND). The charged electrons in the bottom-plate capacitors of the 2-to-1_{dw} block are discharged to ground; all stored charge is dumped into ground, but for the charged electrons in the bottom-plate capacitor of the 2-to-1_{up} block are discharged to the load V_L' . As a result, the energy lost every cycle due to those bottom plate capacitors can be given by

$$E_{BP} \approx \alpha C_{up}(V_L - V_L')^2 + \alpha C_{dw}V_L'^2 \quad (3)$$

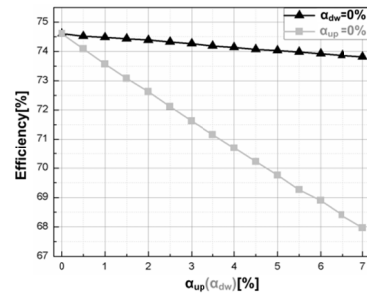


Figure 4 Efficiency drop dependencies with respect to increasing bottom-plate parasitic capacitance ratio ($\alpha=0\%$ to 7%); Black (Grey) represents the efficiency drop with increasing α_{up} (α_{dw}) while α_{dw} (α_{up}) is kept constant at 0%.

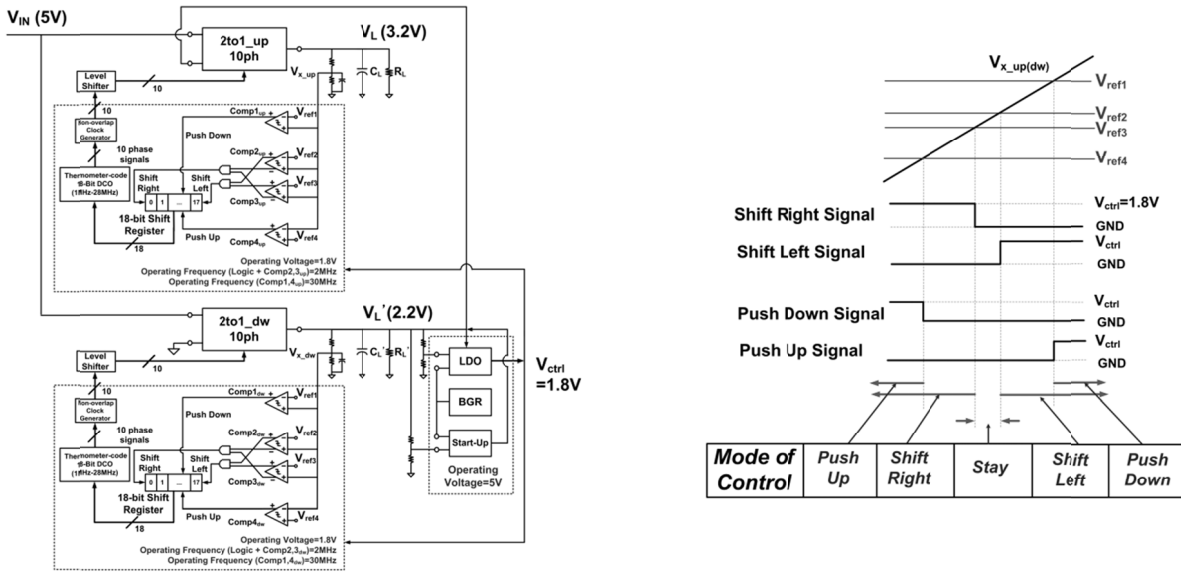


Figure 5 Architecture of dual output switched capacitor DC-DC converter system

Figure 4 shows the efficiency drop dependencies due to the increasing bottom-plate parasitic capacitance of flying capacitors used in 2-to-1_{up} and 2-to-1_{dw} while either α_{up} (when α_{dw} is swept) or α_{dw} (when α_{up} is swept) is set to 0%. Simulation results are obtained at its maximum load condition (delivering 8mA of load currents to both outputs) while the average output voltages are being maintained at $V_L' \approx 2.2V$ and $V_L \approx 3.2V$. With increasing α_{up} (0% to 7%), the total efficiency drops less than 1%, which is six times less than the efficiency drop with increasing α_{dw} (0% to 7%). 1% of efficiency drop arises from the loss during the charging phase (V_L' to V_L) of either of $\alpha_{up}C/2$ capacitor and from the increased V_L' due to the transferred charge from $\alpha_{up}C/2$ capacitors as shown in Figure 3(b) and Equation (3).

Since the overall efficiency is less sensitive to the increasing α_{up} and their larger capacitance density ($2.7fF/\mu m^2$) in $0.35\mu m$ BCDMOS Technology, MOS capacitors are used for implementing the flying capacitors of the 2-to-1_{up} while MIM capacitors are used for implementing 2-to-1_{dw} since they have less bottom-plate capacitance ratio (α_{dw}) than MOS capacitors. This trades off with bigger area since MIM capacitors have smaller capacitance density ($1fF/\mu m^2$).

The minimum required capacitances for each flying capacitor that satisfies the design requirements (the maximum load currents (I_L , I_L') of 8mA) are determined based on the load current handing capabilities of the proposed converter. From equations (1), (2) and Figure 3(b), the load current handing capabilities for both output loads at a fixed frequency and ΔV_L ($\Delta V_L'$) can be obtained by

$$I_L = 2I_1 \approx 2Q_L f_{sw} = 4C_{up} \Delta V_L f_{sw} \quad (4)$$

$$I_L' + I_{ctrl} + 0.5I_L = 2I_2 \approx 2Q_L' f_{sw} = 4C_{dw} \Delta V_L' f_{sw} \quad (5)$$

$$I_L' \approx 4C_{dw} \Delta V_L' f_{sw} - 4C_{up} \Delta V_L f_{sw} - I_{ctrl} \quad (6)$$

where ΔV_L and $\Delta V_L'$ represent the voltage difference of output voltages when there is load and there is no load as described earlier in this paper. Since our target voltages are 2.2V and 3.2V, from Figure 3(a), $\Delta V_L'$ and ΔV_L are determined to be 0.3V and 0.4V, respectively. Since the maximum control current (I_{ctrl}) required by the control block is 300 μA , the required control current is chosen to be 0.5mA with the margin of 200 μA . Therefore, the required

$2I_2$ in Eq. (5) is 12.5mA ($=8mA+0.5mA+4mA$) because both I_L and I_L' are maximum output load current in this case and they are predetermined as design goals. For the given specifications (ΔV_L is 0.4V, $\Delta V_L'$ is 0.3V, and the maximum switching frequency is 28MHz), the minimum required C_{up} and C_{dw} are estimated as 178.57pF and 372pF, respectively. In our design, C_{up} of 200pF and C_{dw} of 400pF are chosen.

As can be observed from equations (4) and (6), with the fixed values of ΔV_L ($\Delta V_L'$) and C_{up} (C_{dw}), I_L (I_L') can be controlled by changing switching frequency (f_{sw}). With changing load current, therefore, the output voltage can be regulated by mean of pulse frequency modulation (PFM). In this design, PFM control scheme is used with 18bit shift register and 18bit DCO which are designed to be operating in the range of 1MHz to 28MHz.

3. ARCHITECTURE

Figure 5 shows the overall architecture of the proposed dual output DC-DC converter. The complete system consists of two 10 phase 2-to-1 blocks, two 18-bit shift registers with push-up(down) function, two 18-bit thermometer code digitally controlled oscillators (DCOs), non-overlap clock generators, level-shifters, 8 dynamic comparators [7], a low-drop output (LDO) voltage regulator and a start-up circuit. The DCO is controlled by an 18-bit thermometer code produced by the shift register. As shown in Figure 5, the load voltages are scaled to $V_{x_up(dw)}$ with feedback resistors, and four reference voltages (V_{ref1-4}) are generated from 5V input with resistor ladders and capacitors. Four dynamic comparators (Comp1-4_{up(dw)}) compare $V_{x_up(dw)}$ to the four different reference voltages to determine the mode of control. For fast start-up and fast transient response with a large load current transition, Comp1_{up(dw)} and Comp4_{up(dw)} are operated with 30MHz of clock frequency while Comp2_{up(dw)} and Comp3_{up(dw)} are operated with 2MHz of clock frequency for stable voltage locking between V_{ref2} and V_{ref3} . If $V_{x_up(dw)}$ is less than V_{ref4} , Push-Up mode is enabled and thermometer code transits to its maximum value, which generates the maximum switching frequency. In the similar way, if $V_{x_up(dw)}$ is bigger than V_{ref1} , thermometer code drops to the pre-programmed value. If $V_{x_up(dw)}$ enters between V_{ref1} and V_{ref4} , the switching frequency increases or decreases

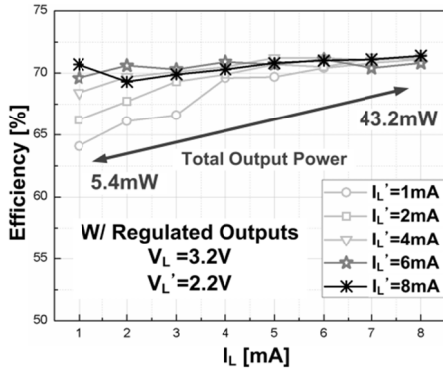


Figure 6 Efficiency versus I_L while I_L' is varying between 1mA and 8mA

linearly with the step period of $0.5\mu\text{s}$ ($(2\text{MHz})^{-1}$) until $V_{x_up(dw)}$ is locked between V_{ref2} and V_{ref3} .

4. SIMULATION RESULTS

The proposed SC power converter is designed using high-voltage $0.35\mu\text{m}$ BCDMOS technology and simulated with HSPICE. Two types of flying capacitors (MIM and MOS Capacitors) are used to maximize the power density and efficiency at the limited area. Each 2-to-1_{up} block uses 20pF of MOS capacitor (the total capacitance of 200pF for 10 phase) for its flying capacitor to maximize the power density, while each 2-to-1_{dw} block uses 42pF of MIM capacitor (the total flying capacitance of 420pF for 10 phase) to minimize the loss due to bottom-plate parasitic capacitance. MOS capacitors are used for the output buffer capacitors (400pF for each) to reduce the output ripple voltages and to maintain the moderate level of transient response for varying load currents. Figure 6 shows the simulated efficiency with different load current levels between 1mA and 8mA, while the output voltages are regulated at DC level of 2.2V (3.2V) for V_L' (V_L). The proposed converter achieves 70.0% of the average efficiency in the output power ranges between 5.4mW and 43.2mW and the maximum efficiency (71.4%) is achieved when it delivers the maximum power (43.2mW). The control logic blocks including BGR (Bandgap Reference) circuit and bias circuits consume the power between 0.46mW and 1mW over the operating power transfer ranges. Figure 7 shows simulated transient response with load current (I_L) transition from 1mA to 8mA, and vice versa. With Push-up and Push-down modes, the converter settles within 450ns ($1\mu\text{s}$) for 1mA (8mA) to 8mA

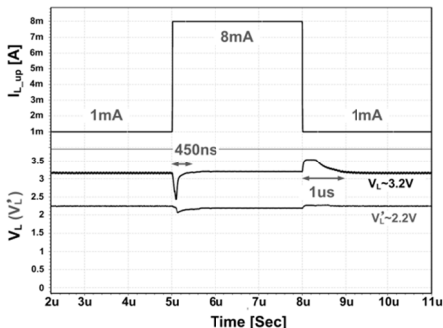


Figure 7 Transient response of V_L (V_L') with varying load current I_L (1mA to 8mA and vice versa) while $I_L'=8\text{mA}$

(1mA) transition while 2-to-1_{dw} delivers 8mA of the load current (I_L'). The interference between two outputs are inevitable, but this can be minimized with increasing clock frequency of $\text{Comp}_{1,4_up(dw)}$ or increasing the load capacitance. Comparison with recently published SC converters designed using $0.35\mu\text{m}$ CMOS technology is listed in Table 1. While other SC converters are able to support only one step-down output voltage at a time, proposed converter can support two different voltages at the same time. In addition, since the switching frequency of the proposed converter is regulated digitally over wide frequency ranges between 1 and 28MHz with different load conditions, it maintains higher peak and average efficiency even with less flying and output buffer capacitance, hence less area.

Table 1 Comparison with Recently Published SC Converters

	[4]	[5]	[6]	This work
Process (CMOS)	$0.35\mu\text{m}$	$0.35\mu\text{m}$	$0.35\mu\text{m}$	$0.35\mu\text{m}$ BCDMOS
V_{in}	2.5V	5V	3.4-5V	5V
V_{out} Regulated	0.9-1.5V	1V	3.3V	3.2V and 2.2V
C_{fly}	6.72nF (on-chip)	1.2nF (on-chip)	1uF (off-chip)	$C_{fly,up}=200\text{pF}$ MOS-cap $C_{fly,dw}=420\text{pF}$ MIM-cap
C_{out}	470nF (off-chip)	N/A	1uF (off-chip)	400pF (x2) MOS-cap
f_{sw}	0.2-1MHz	15MHz	100kHz	1-28MHz
η	$\leq 66.7\%$	31%	$\leq 65\%$	$\leq 71.4\%$ ($\eta_{avg}=70.0\%$)
P_{out}	0.4-7.5mW	10mW	3.3-24.7mW	5.4-43.2mW
I_L (I_L')	0.5-5mA	N/A	1-7.5mA	1-8mA

5. CONCLUSION

This paper presents a fully integrated on-chip SC DC-DC converter with dual outputs (2.2V and 3.2V). The proposed converter is designed using high-voltage $0.35\mu\text{m}$ BCDMOS technology. The converter achieves the average efficiency 70.0% and the peak efficiency 71.4%. Using 10-phase interleaving technique, the output voltage ripples of the both outputs are maintained less than 1% ($<4\text{mV}$) of the output voltages when 400pF of output buffer capacitors are used for both outputs.

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