

# Phase-Locked Loop with Leakage and Power/Ground Noise Compensation in 32nm Technology

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**Abstract**—This paper presents two novel compensation circuits for leakage current and power supply noise (PSN) in phase locked loop (PLL) using a nanometer CMOS technology. The leakage compensation circuit reduces the leakage current of the charge pump circuit and the PSN compensation circuit decreases the effect of power supply variation on the output frequency of VCO. The PLL design is based on a 32nm predictive CMOS technology and uses a 0.9 V power supply voltage. The simulation results show that the proposed PLL achieves 88% jitter reduction at 440 MHz output frequency compared to the PLL without leakage compensator and its output frequency drift is little to 20% power supply voltage variations. The PLL has an output frequency range of 40 M~725 MHz with a multiplication range of 1-1023, and the RMS and peak-to-peak jitter are 5psec and 42.7 psec, respectively.

**Index Terms**— Phase-Locked Loop (PLL), Power Supply Noise, Leakage Current

## I. INTRODUCTION

As the supply voltage scales down with the technology, any power supply noise on power and ground level affects the analog circuit performance more than before. This power supply noise has a direct effect on the voltage controller oscillator (VCO) output frequency of PLL. Therefore, this power supply noise is a critical issue to

be resolved for better jitter performance of PLL [1, 2].

The power supply noise (PSN) at the power/ground lines is another serious problem to be considered in the low power and high performance mixed mode systems since the on-chip power/ground voltage variation of the analog part increases due to the IR-drop and the  $Ldi/dt$  noise in digital part in spite of all the techniques to minimize them. This affects the functionality and performance of the analog circuit as well as the digital part, and may cause even circuit failure. Therefore, the power supply noise has a deep impact on the output frequency of PLL [3, 4].

In addition, leakage current in CMOS circuit design using nanoscale process has gradually become a significant issue [5, 6]. The leakage current increases with the transistor size of CMOS and the VCO output frequency is more sensitive to the leakage current and its control voltage ( $V_C$ ) in high frequency operation. Therefore, for a large multiplication factor in PLL, the leakage current has a considerable effect on the  $V_C$  variation of the VCO after the large feedback cycle detection. Consequently, the leakage current is an important issue to be addressed for the PLL jitter performance [7].

In this paper, a nanometer CMOS PLL design using a 32nm CMOS technology is described, where low jitter performance is achieved using compensation circuits to reduce power supply noise effect on VCO output frequency and the leakage current in the charge pump. An MOS capacitor and an MIM capacitor are used for a big capacitance to save the chip area and a small capacitor in the passive second-order loop filter, respectively. To compensate the leakage current from the MOS capacitor a voltage feedback buffer is used in the loop filter, and a ring oscillator based VCO is used for a relatively small area and robustness over process and temperature variations.

The remainder of this paper is organized as follows.

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Section II illustrates the circuit diagram of the PLL where the proposed compensation circuits for leakage and power supply noise (PSN) are presented. The results and comparison with other PLL are shown in Section III followed by conclusion in Section IV.

## II. PROPOSED PLL CIRCUIT

Fig. 1 shows the proposed PLL with the compensation circuit blocks for leakage current and PSN. In addition to the conventional PLL blocks such as phase-frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO), and a frequency divider, the PLL in this paper includes the leakage compensator, the PSN compensator, and the voltage buffer block in the loop filter. The leakage compensation consists of two charge pump replicas and current mirrors. Using the UP/DN signals from the PFD and two bias voltages of charge pump, the leakage compensator senses the leakage current of the charge pump circuit and generates the same amount of current as the leakage current of the charge pump.

However, the directions of the generated leakage current are opposite to those of the leakage current in the charge pump. That is how the leakage current of the charge pump is cancelled through the leakage compensator. The PSN compensation circuit consists of  $n$ -stage inverters and current differential amplifiers. The inverters are used to monitor the propagation delay which is variable depending on PSN. The number of stage of the inverter

chain is determined based on the power supply voltage noise range and the inverter delay. The current differential amplifiers convert the difference between the nominal propagation delay and the monitored actual propagation delay to current. The generated current is added to or subtracted from the current source in the VCO depending on the PSN polarity to adjust the VCO output frequency. The input signals of the PSN compensator are the control signal to enable the circuit and the reference clock, and the reference clock is propagated through the inverter chain.

### 1. Charge Pump Circuit and VCO Circuit

Fig. 2 shows the circuit schematic of the charge pump. The main charge pump is composed of MP6, MP7, MN6, and MN7. MP4,5(MP8,9). MN8,9(MN4,5) are the gain boosting stages to increase the output resistance of the charging and discharging current sources. In Fig. 2, the resistor,  $R_{bias}$ , MP1, and MN1 generate the bias current. When the UP (DN) signal is high, MP2 (MN2) turns on and MP6 (MN6) turns on. When the UP (DN) signal is low, MP3 (MN3) turns on and MP6 (MN6) will turn off. MP7 and MN7 are operated as current sources in the charge pump. UP1/UP\_bias signal and DN1/DN\_bias signal are used to replicate the leakage current of the charge pump in the leakage compensation circuit.

The VCO is designed to operate at low supply voltage. As shown in Fig. 3, the VCO consists of a cascode self-biasing current source and a current starved ring oscillator with 11-stage of inverters.

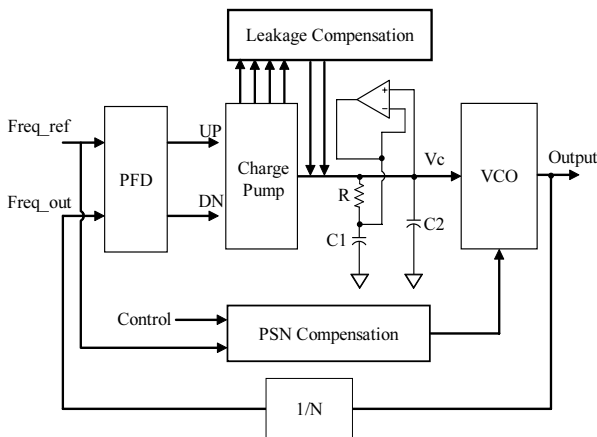


Fig. 1. Block diagram of the proposed PLL.

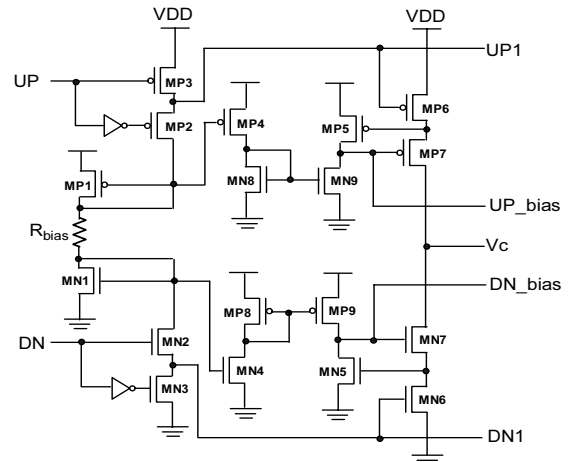


Fig. 2. Proposed charge pump circuit.

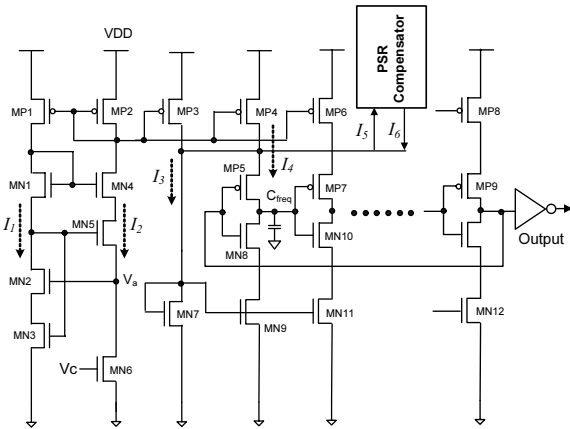


Fig. 3. Proposed VCO circuit.

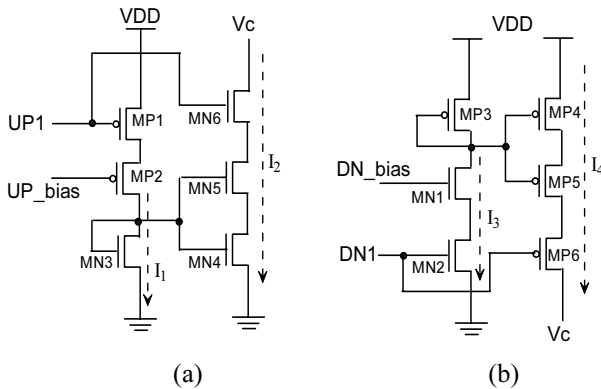


Fig. 4. Proposed leakage compensator with CP replica: (a) for PMOS, (b) for NMOS.

**2. Leakage Compensation Circuit**

The replica charge pump is composed of MP1, MP2, MN1, and MN2 as shown in Fig. 4. Figure 4(a) presents the leakage generator circuit for the PMOSFETs of charge pump, and Fig. 4(b) is the leakage generator circuit for the NMOSFETs of charge pump (CP). For the PMOS-FETs of the charge pump, the leakage current ( $I_1$ ) is generated by “HIGH” UP1 signal, and its mirrored current  $I_2$  flows through MN6 (ON state). The current  $I_2$  which is exactly the same as the leakage current is subtracted from the node Vc to offset the PMOSFETs’ leakage current of charge pump, resulting in the lower VCO control voltage Vc. The operation of Fig. 4(b) is the same as that of PMOSFETs.

The compensator uses the self-cascode current mirror for low voltage operation. The self-cascode structure (MN4 and MN5) provides high output impedance with larger voltage headroom than the conventional cascode

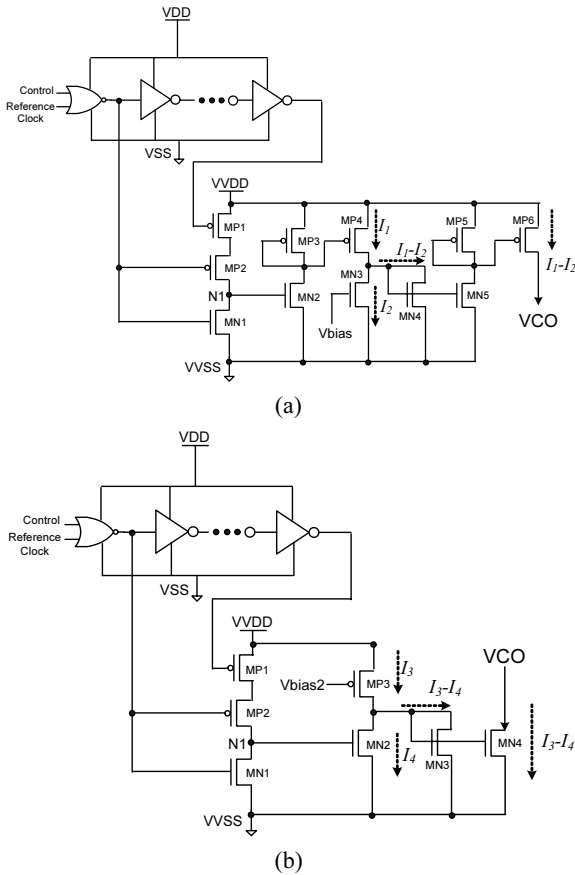
scheme. The MN4 and MN5 can be treated as a single composite transistor. The composite structure has much larger effective channel length, and the effective output conductance is much lower. The lower transistor MN4 is equivalent to a resistor whose value is dependent on the bias voltage. For optimal operation, the W/L ratio of MN5 is kept larger than that of MN4, that is,  $m > 1$  ( $m$  is the W/L ratio of the transistor MN5 to MN4). For the composite cascode structure, the effective transconductance ( $g_m(\text{effective})$ ) will be  $g_{m5}/m$ , which is equivalent to the transconductance of MN4 ( $g_{m4}$ ). Then, the drain current ( $I_D$ ) through MN4 and MN5 will be  $\beta_{\text{effective}} (V_{in} - V_T)^2 / 2$ , where  $\beta_{\text{effective}}$  equals  $\beta_4\beta_5 / (\beta_4 + \beta_5)$ , which can be approximated by  $\beta_4$  when  $m$  is large [8].

The voltage between source and drain of MN4 is small, and there is no appreciable difference between the  $V_{DSAT}$  of composite and simple transistors, and a self-cascode can be used in low voltage operation. For a self-cascode  $V_{DSAT} = V_{DSATM4} + V_{DSATM5}$ . The operating voltage of a regular cascode is much higher than that of a self-cascode. The self-cascode current mirror satisfies the requirements to compensate the small leakage current due to the advantages offered by the self-cascode structure offering high output impedance similar to that of the conventional cascode structure while the output voltage requirements are similar to those of a single transistor.

**3. PSN Compensation Circuit**

The main idea of the proposed PSN compensator is to monitor the power supply noise through its effect on the propagation delay of the inverter chain to compensate the charge pump output voltage error caused by the PSN. Fig. 5 shows the circuit schematic of the proposed PSN compensator for the positive and negative variations of power supply. The n-stage inverter chain works as a delay line, whose delay depends on its effective supply voltage (in this research seven stage is used). In PLL circuit, the PSN compensator is triggered by the control signal and reference clock is used as the input to the inverter chain delay line. The NOR gate works as a control gate to operate the compensator when desired.

Transistors MP1 and MP2 work as switches connected in series between voltage  $V_{VDD}$  and N1.  $V_{VDD}$  comes from a local capacitor which is large enough to keep the constant voltage. When the reference clock is at “0” and



**Fig. 5.** Proposed PSN compensation circuit: (a) Negative voltage variation, (b) Positive voltage variation.

the control signal is at “0”, switch MP2 is open and MP1 is closed. The rising edge of the clock line closes switch MP2, and a current begins to flow to N1 node. This current charges the gate capacitor of MN2 until the output signal of the inverter block changes, opening the switch MP1. Thus, the total charge supplied to N1 node is proportional to the propagation delay of the inverter block. As the propagation delay depends on the effective supply voltage seen by this block, the voltage of N1 at the end of the sampling period also depends on the supply voltage. As the power/ground bounce is produced just after the clock edge, the voltage of N1 will be dependent on the power/ground bounce: the higher the supply voltage drop is, the longer the propagation delay and the higher the voltage of N1 and  $I_1$  will be. If the effective supply voltage is higher due to the positive PSN noise, the voltage of N1 and  $I_1$  will be lower as the propagation delay becomes slower.

The compensator samples the PSN during a time interval that is much shorter than the duration of the PSN.

The sampling time of the compensator corresponds to the moment when a rising edge is produced in the reference clock. By introducing a programmable delay line from the control signal to the NOR input, the sampling moment can be changed and the samples of the voltage of N1 at different times are obtained to check the PSN in the whole clock cycle.

In addition, a current mirror and a current differential amplifier are added to convert the voltage of N1 to current. In Fig. 5(a),  $I_1$  is the current which is proportional to the voltage of N1, and  $I_2$  is the reference current generated when the inverters have a normal power supply without PSN. If the power supply is reduced by PSN, the propagation delay of the inverter chain will increase, and the output frequency of PLL will decrease. Therefore, if  $I_1-I_2$  in the current differential amplifier is added to the cascode self-biasing current source in the VCO block, and the VCO output frequency will increase in proportional to the current difference. The circuit to compensate positive PSN is shown in Fig. 5(b). In this case, the  $I_3-I_4$  has to be subtracted from the cascode self-biasing current source in the VCO to decrease the output frequency of VCO.

### III. EXPERIMENTAL RESULTS

The circuit is designed in a 32nm PTM BSIM4 technology. Correct operation and performance of the circuit design are verified through simulations. The proposed VCO operates from 40 MHz to 725 MHz at 0.9 V supply voltage.

When the temperature is changed from  $-25^\circ\text{C}$  to  $75^\circ\text{C}$ , the VCO frequency variation is within 8%. The linear relationship between the frequency and control voltage is shown in Fig. 6. As the control voltage increases from 0 V to 0.7 V, the current increases linearly. The VCO gain is 0.48 MHz/1 mV, and the center frequency is 450 MHz. 10 % supply voltage change causes only 9.3 % frequency variation ( $\pm 21$  MHz from the center frequency).

In Fig. 6, the frequency vs. control voltage is shown for different power supply voltages. If VDD is changed from 0.9 V to 0.7 V, the frequency decreases as expected. On the other hand, if the proposed PSN compensator is used in the same power supply voltage (0.7 V), the frequency is almost the same as the case with 0.9 V power supply voltage.

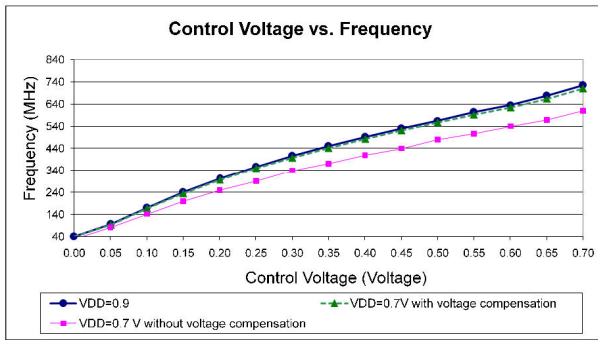


Fig. 6. Frequency vs. Control voltage of the proposed VCO.

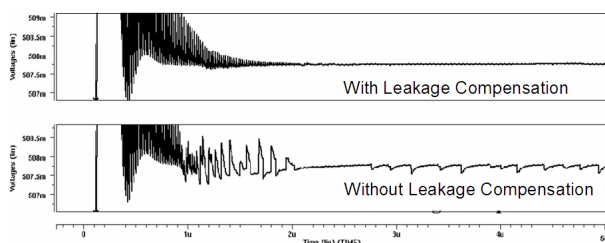


Fig. 7. VCO input control voltage of charge pump with and without leakage compensation.

Fig. 7 shows the control voltage of the PLL for both cases where the leakage compensation circuit is employed and the compensation circuit is not employed to compare the cases when the frequency of VCO is 725 MHz.

The proposed PLL performance is compared with a previously published PLL as shown in Table 1. It is demonstrated that the new PLL reduces timing jitter significantly while providing other comparable PLL performance. The variation of the control voltage in the conventional PLL is about 1 mV and the variation of the control voltage in the proposed PLL using leakage compensator is much less than 1mV.

#### IV. CONCLUSIONS

The proposed compensation is designed in 32nm PTM (Predictable Technology Model) BSIM4 model. A novel leakage compensation circuit technique is presented to reduce the jitter caused by the transistor leakage current. The leakage compensator effectively improves the jitter performance of the conventional PLL in nanometer technology. To compensate the power supply noise effect on VCO, the effect of the noise is detected using an inverter chain and the power supply noise effect is compensated by the PSN compensator. The PSN compensator and

leakage compensator provide the PLL with better performance and independence of power supply variation by reducing the jitter and increasing the output frequency range of the VCO. The proposed circuit techniques will be a good reference for the future mixed mode circuit design research in nanometer CMOS integrated circuit design.

Table. 1. Performance summary.

Performance Summary		
Reference	This Work	[7]
Process	32nm	0.13um
Supply Voltage	0.9V	1V
Reference Frequency Range	0.4M~10MHz	X
Output Frequency Range	40M~725MHz	10M~700MHz
RMS Jitter (peak-to-peak) at 440MHz	Charge Pump with Leakage Compensation	5ps (42.6ps)
	Charge Pump without Leakage Compensation	40.9ps (242ps)
		24.3ps(155ps) at 360MHz
		X

#### REFERENCES

- [1] Xiaolue Lai, and et al., “Fast, accurate prediction of PLL jitter induced by power grid noise”, *IEEE CICC 2004*, pp. 121-124, 2004.
- [2] Payam Heydari, and Massoud Pedram, “Jitter-Induced Power/Ground Noise in CMOS PLLs: A Design Perspective”, *Proceedings of the international Conference on Computer Design: VLSI in Computers & Processors (ICCD '01)*, pp. 209-213, 2001.
- [3] She Lin, and Norman Chang, “Challenges in Power-Ground Integrity”, *IEEE ICCAD 2001*, pp. 651-654, 2001.
- [4] Anantha Chandrakasan, William J. Bowhill, and Frank Fox, “Design of High-Performance Microprocessor Circuits”, *IEEE Press*, 2000.
- [5] Koichiro Ishibashi, Tetsuya Fujimoto, and et al., “Low-Voltage and Low-Power Logic, memory, and Analog Circuit Techniques for SoCs Using 90 nm Technology and Beyond”, *IEICE Trans. Electron.*, Vol. E89-C, No.3, Mar. 2006.
- [6] Anne-Johan Annema, Bram Nauta, et al., “Analog Circuits in Ultra-Deep-Submicron CMOS”, *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 1, Jan

2005.

- [7] Reuven Holzer, "A 1V CMOS PLL Designed in High-Leakage CMOS process Operating at 10-700MHz", *IEEE International Solid State Circuits Conference*, Vol. 2, pp. 220-482, Feb. 2002.
- [8] Shouli Yan, and Edgar Sanchez-Sinencio, "Low Voltage Analog Circuit Design Techniques: A Tutorial", *IEICE Trans. Analog Integrated Circuits and Systems*, vol. E00-A, No. 2, Feb. 2000.



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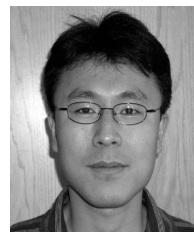
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