

DESIGN AND ANALYSIS OF A QUADDIFFERENTIAL AMPLIFIER WITH EFFECTIVE COMMON-MODE REJECTION FOR A SUB-CIRCUIT IN CAT5*

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This paper presents a design and analysis of a quadifferential amplifier for a CAT5 cable. A quadifferential amplifier consists of four inputs, four outputs, and a V_{ocm} pin which controls the output common-mode voltage. It is similar to the differential amplifier in that it amplifies differences and rejects overall input common-mode. The transfer function shows that quadifferential amplifier requires symmetry of feedback and gain resistors to approach its ideal behavior. Using a graphical approach the amplifier is compensated to drive a capacitive load of $50pF$. The output current drive is designed for minimum load resistance of 150Ω . Performing Monte Carlo simulations to evaluate offset voltage and common-mode rejection show the mean offset voltage of $265\mu V$ and a common-mode rejection of 126dB.

Keywords: A quadifferential amplifier; a Differential amplifier; a trifferentialamplifier; 4-channel RGBY video; Sub-circuit; CAT5.

1. Introduction

Traditional three color display devices provide limited brightness dynamic range. As a result of recent developments in display technology, display devices with four primary colors are becoming commercially available. The fourth color, yellow, is changing the signal processing from the traditional 3-channel RGB video to 4-channel RGBY. Design and analysis of the four channels provides an idea regarding the expanded version of the trifferential amplifier.[1]

The triffential amplifier is used in a sub-circuit in a CAT5 (Category 5) video cross-point switch matrix. A cross-point switch matrix is utilized in environments where multiple video inputs are routed to multiple locations. The presence of unwanted common-mode signals in CAT5 video applications corrupts the information. Slight differences in the common-mode DC between the outputs from the cross-point switches can further exacerbate overall image quality due to the brightness variations between outputs. The common-mode level needs to be controlled for two reasons. First, the overall common-mode must be kept constant to retain the dynamic range of the video signal. Second, the controlled common-mode level maximizes the amount of information sent over to the CAT5 cable. The most efficient method of controlling the common-mode signal is to remove it from all inputs. Adding clamping circuitry to the inputs can remove the common-mode. The triffential amplifier mitigates the need for multiple video clamping circuitries. It removes unwanted input common-mode and allows for the common-mode of the cross-point outputs to be controlled. The proposed quadfferential amplifier removes unwanted overall common-mode signals like triffential amplifier. The quadfferential amplifier not only removes the unwanted noise but also amplifies the differences of the four inputs.

2. Definition of a quadfferential amplifier

The function of the quadfferential amplifier is similar to a differential amplifier in that it responds to difference signals. The primary function of the quadfferential amplifier is to remove overall common-mode and amplify differences. By design, it will accept four input voltages and produces four output voltages; The voltage differences between any pair of output voltages is proportional to the differences between the corresponding pair of input voltages through the same proportionality constant.[1] The average value of the four output voltages is constant and unrelated to the input voltages.[1]

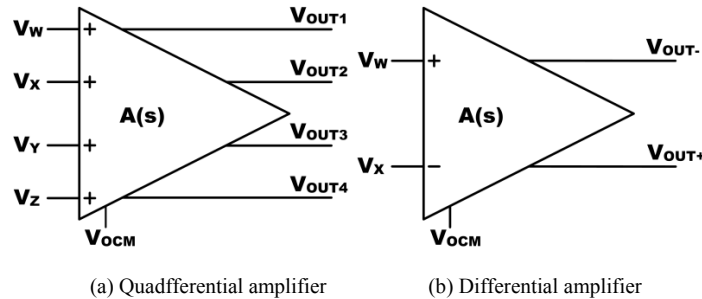


Fig 1. Symbol comparison of the quadfferential and the differential amplifier

A symbol of a quadfferential amplifier is shown in Fig 1. It has two supplies, four non-inverting inputs, four outputs, and output common-mode control, V_{ocm} . There are three visual differences between the two architectures as illustrated in Fig 1; (1) no inverting input terminals exist, (2) there are two additional inputs, and (3) there are two additional outputs.

A block diagram for the quadfferential amplifier is presented in Fig 2. Bus wire is used to indicate the parallel signal flows. The numbers of parallel signals are designated above each bus wire with a forward slash followed by a number. The input stage accepts four input voltages, and outputs eight currents.

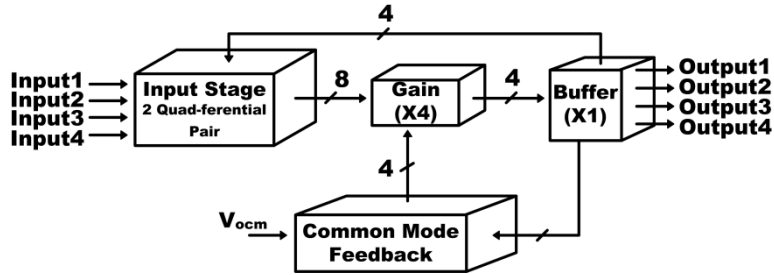


Fig 2. Block diagram of the quadfferential pair

The input stage is the core of the quadfferential amplifier. It accepts four voltages, outputs eight currents, and consists of two quadfferential pairs. The pairs amplify the differences between any two inputs while rejecting common-mode components. The quadfferential pair can be thought of as a g_m cell that accepts voltages and outputs currents like a differential pair.

The currents generated by the input stage proceed to the gain stage. From the gain node, the signals are buffered and continue to the output. The output is fed into two blocks, which are the input stage via R_F and R_C network to establish negative feedback and the common-mode circuit block for control of the overall output common-mode voltage. The common-mode circuit block samples the output voltages, compares the average value to V_{ocm} , and sends the appropriate common-mode bias level to the gain stage.

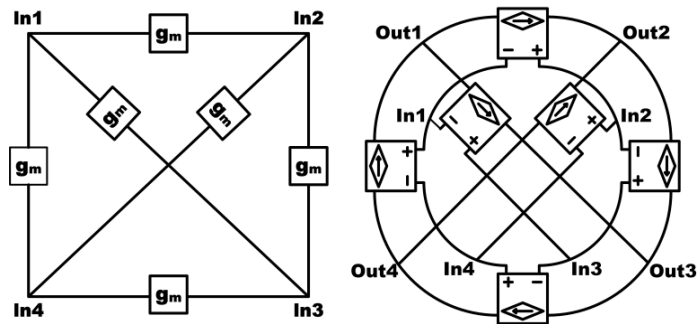


Fig 3. A configuration of the quadfferential pair

From an architectural standpoint, the quadfferential amplifier is an extension of the differential amplifier. The quadfferential amplifier processes its signals with three stages and two feedback loops: an input stage, a gain stage, an output stage, a quadfferential feedback loop to establish negative feedback and a common-mode loop to control the output common-mode voltage.

A simplified circuit of the quadfferential amplifier is presented in Fig 4. The input stage receives its bias from I_{TAIL1} . The cascode transistor Q_5 (Q_6) receives the bias current of $I_{TAIL2}/2$ from differential pair Q_9 and Q_{10} via the diode connection of Q_{11} (Q_{12}) and current source transistor Q_7 (Q_8).

The input stage accepts four input voltages and four output differential currents, i_{PX} and i_{NX} . Transistors Q_1 through Q_4 , Wilson current mirror, translates the transconductance of the input stage to the high impedance node. The high impedance node is formed by the output impedance of the Wilson current mirror[10] in parallel with the output impedance of the cascode current source.

From a feedback perspective, the common-mode level is sensed across the four resistors (R_1, R_2, R_3 and R_4) connected to the base of Q_{10} . The average of the output voltage is sampled and compared to the value on the V_{ocm} pin. The differential pair, Q_9 and Q_{10} , control the output common-mode level of the amplifier by setting the appropriate bias level (as determined by the input level on the V_{ocm} pin) at the output by modulating the currents in Q_{11} and Q_{12} . I_{TAIL2} provides the bias level for Q_9 and Q_{10} .

3. Quadfferential pair signal behavior

3.1. Large signal single-ended and differential behavior

Large signal behavior gives insight into the available DC linear operating range. It illustrates the limited range of input voltages, where the circuit behaves almost linearly.[6] The large signal behavior presented R_{EE} , the Norton equivalent impedance of the current source[7], is infinite because it does not strongly affect the low-frequency, large-signal behavior of the circuit.[8]

Single-ended output voltage behavior yields insight into how each output responds to the differences at its input. Single-ended output voltage behavior can be expressed as

$$V_{O1P,D} = \alpha I_{TAIL} R_C \left(\frac{1}{1+e^{\frac{V_{ID(1,2)}}{V_t}}} + \frac{1}{1+e^{\frac{-V_{ID(4,1)}}{V_t}}} + \frac{1}{1+e^{\frac{V_{ID(1,3)}}{V_t}}} \right) + V_{EE} \quad (1)$$

$$V_{O2P,D} = \alpha I_{TAIL} R_C \left(\frac{1}{1+e^{\frac{-V_{ID(1,2)}}{V_t}}} + \frac{1}{1+e^{\frac{V_{ID(2,3)}}{V_t}}} + \frac{1}{1+e^{\frac{-V_{ID(4,2)}}{V_t}}} \right) + V_{EE} \quad (2)$$

$$V_{O3P,D} = \alpha I_{TAIL} R_C \left(\frac{1}{1+e^{\frac{-V_{ID(2,3)}}{V_t}}} + \frac{1}{1+e^{\frac{V_{ID(3,4)}}{V_t}}} + \frac{1}{1+e^{\frac{-V_{ID(1,3)}}{V_t}}} \right) + V_{EE} \quad (3)$$

$$V_{O4P,D} = \alpha I_{TAIL} R_C \left(\frac{1}{1+e^{\frac{-V_{ID(3,4)}}{V_t}}} + \frac{1}{1+e^{\frac{V_{ID(4,1)}}{V_t}}} + \frac{1}{1+e^{\frac{V_{ID(4,2)}}{V_t}}} \right) + V_{EE} \quad (4)$$

Signal nomenclature will adhere to the IEEE standards as referenced by Hurst and Lewis.[2]

Three observations are prevalent from the large signal single-ended output voltage expressions responding to input differences in Equations (1) through (4). First, each channel influences three output difference voltages. Second, a single-ended output

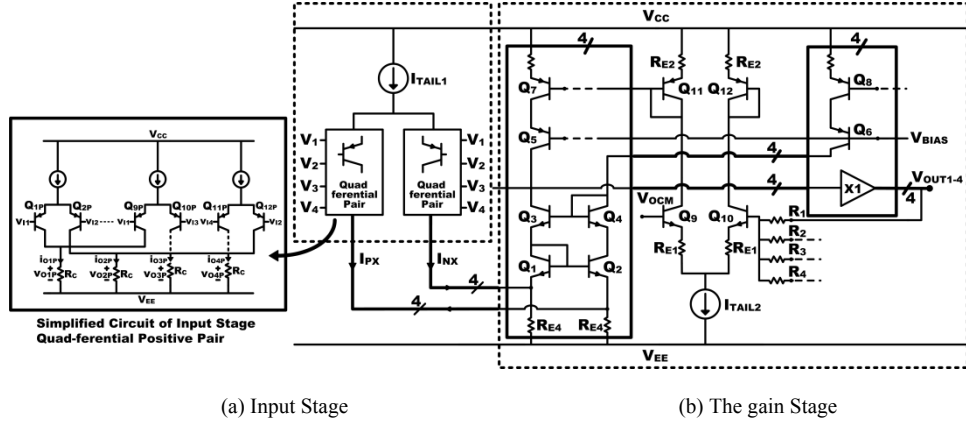


Fig 4. Simplified Circuits of the quadfferential amplifier

channel contains three terms and it is proportional to three difference inputs. Third, the arguments for the exponential terms, the input difference voltages, adhere to a pattern which reveals the three arguments sum. All arguments with the first number in the input difference voltage corresponding to the single-ended output channel have the same sign. The other arguments are the opposite in sign. This observation is important because it describes how the collector currents sum rather than oppose each other. Prior to detail quantitative graph illustration of how the quadfferential pair responds to large signal input differences, the variable for the independent axis (X axis) needs to be explained. An unconventional variable is required for the x-axis in the graph because one single-ended input voltage influences three difference voltages. To sweep the difference

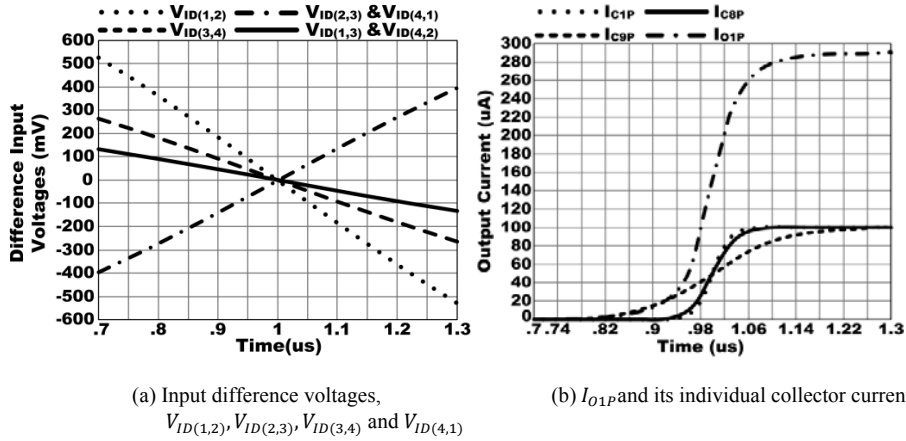


Fig 5. Simulation of I_{O1P} and its individual collector currents

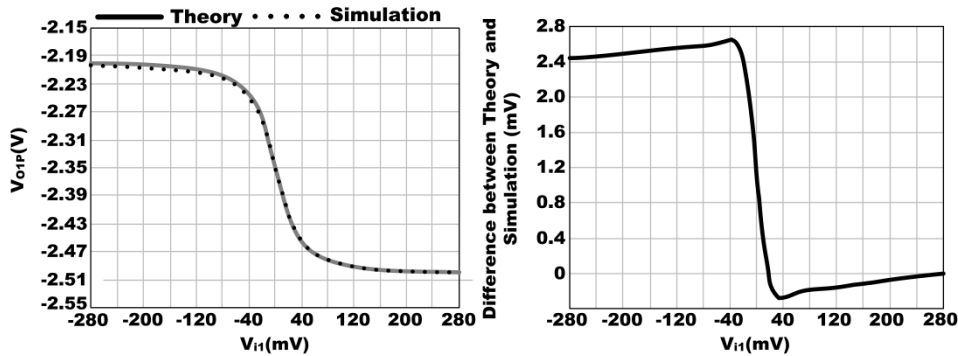
voltages independently, a transient approach is necessary. Time is therefore the independent variable to allow independent movement of the input difference voltages. The input difference voltages stimulating I_{O1P} , $V_{ID(1,2)}$, $V_{ID(4,1)}$ and $V_{ID(1,3)}$ are shown in Fig 5(a). The resulting output current, I_{O1P} with its individual elements, are shown in Fig

5(b). The plot shows the individual collector currents summing. With a tail current of $100\mu A$, each collector is capable of sourcing $100\mu A$ theoretically making the maximum current, $300\mu A$, through I_{O1P} . However, the simulation indicates I_{O1P} is not $300\mu A$. This discrepancy is due to I_{C9P} not reaching its final value of $100\mu A$.

An additional trait is evident from the single-ended large signal expressions responding to the input difference voltages in Equations (1) through (4). The same channel between the positive and the negative quadfferential pair are opposite in sign.

With the behavior of the individual voltages confirmed, it is important to prove the correlation between the theoretical analysis and simulation results. For simplicity, one output voltage, V_{O1P} in Equation (1), is used for comparison. Consequently, V_{I2} is the opposite in magnitude to V_{I1} , V_{I3} is proportional to 50% of V_{I1} , and V_{I4} is the opposite in magnitude and proportional to 50% of V_{I1} .

A plot of the theoretical expression, Equation (1), and simulation result for V_{O1P} is presented in Fig 6(a). The difference between the two is shown in Fig 6(b). As Fig 6(b) illustrates, the maximum difference (delta) between simulation and theoretical derivation is approximately $2.7mV$, which translates to a 10% difference. Therefore, the simulation and derivation correlate.



(a) Theoretical expression, Equation (1), and simulation result of V_{O1P}

(b) Correlation to within 10%

Fig 6. Comparison of the theoretical expression, Equation (1), and simulation result for V_{O1P}

When a circuit block consists of multiple inputs and multiple outputs and is capable of amplifying differences while rejecting common-mode, it is typically implemented in a differential signal chain. Thus, another trait of interest is how the four single-ended outputs of the quadfferential pair responds to two unique differential inputs. To implement two unique differential signals, the individual inputs are paired. V_{I1} is differential with respect to V_{I2} and V_{I3} is differential with respect to V_{I4} . Furthermore, being inherent in using two different input differential voltages, one differential voltage is larger in magnitude than the other. Thus, V_{I3} and V_{I4} are chosen to be fifty percent less in magnitude with respect to V_{I1} and V_{I2} .

With the input voltages established, Fig 7(b) is a simulation of the single-ended output voltages, V_{O1P} through V_{O4P} , responding to the two unique differential signals from Fig

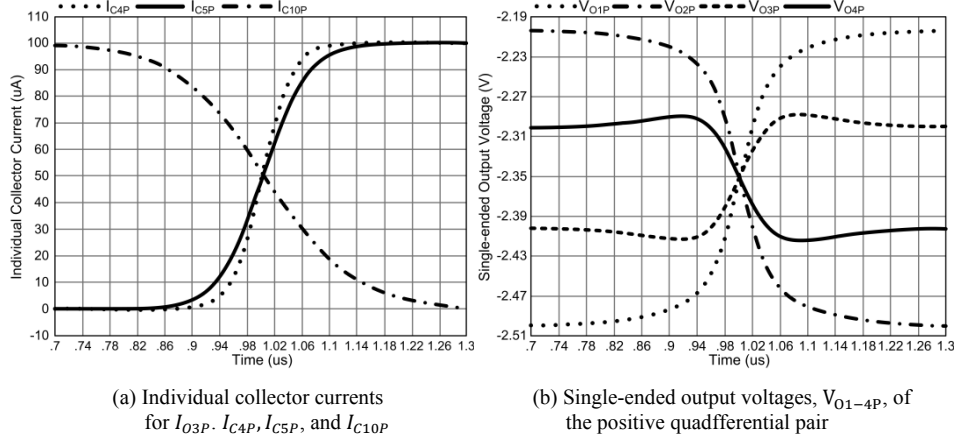


Fig 7. Single-ended output voltages of the positive quadfferential pair

5(a). There is mild peaking on V_{O3P} and V_{O4P} due to the presence of two unique differential input voltages. When two unique differential signals are applied, one of the collector currents is the opposite in magnitude compared to the other two. Instead of three collector currents summing together, a difference is seen during the transition, and the subtraction manifests itself through peaking. Using V_{O3P} as an example, its individual collector currents are I_{C4P} , I_{C5P} , and I_{C10P} , and are shown in Fig 7(a). The simulation in Fig 7(a) illustrates I_{C4P} and I_{C5P} summing while I_{C10P} subtracts from I_{O3P} .

To examine this behavior from a qualitative point of view, it is necessary to refer to the simplified schematic of the positive quadfferential pair in Fig 4(a). V_{I1} controls the base of Q_{9P} while V_{I3} controls the base of Q_{10P} . Because V_{I1} has a faster rate of change with respect to V_{I3} , I_{C10P} must decrease. A comparable argument can be made for V_{O4P} , however, the transistors and input voltages involved are Q_{11P} , Q_{12P} , V_{I4} and V_{I2} . Expanding upon that explanation, V_{O1P} and V_{O2P} do not have peaking because the $\frac{dV}{dt}$ of V_{I1} and V_{I2} are faster compared to V_{I3} and V_{I4} and thus, V_{O1P} and V_{O2P} , behave as expected. The large signal DC linear region is important because it is the region where small signal behavior can be modeled with linear approximations.

Differential behavior describes how a specific difference across two inputs is processed in the signal chain. Two observations are visible with respect to the linear DC operating range of the quadfferential pair. First, when the outputs are taken as differences, the linear region responds in a *tanh* manner with respect to its primary input differential voltage. Second, when two unique input differential voltages are applied, as shown in Fig 7(a), the input difference range where all transistors remain linear is determined by the input difference pairs which are non-differential and possess the same polarity.

3.2. Small signal single-ended and differential behavior

Small signal analysis defines the necessary parameters to describe a circuit's AC behavior. To make the small signal analysis realistic to within first order approximations and to be able to take advantage of linearization techniques, the following assumptions are necessary:

1. To maintain operation within the linear region, the DC input voltage difference is assumed to be zero.
2. Norton equivalent resistance of the tail currents is finite and is represented by the element, R_{EE} . This is important because R_{EE} has a considerable effect on small signal behavior. For example, if $R_{EE} = \infty$ then, the common-mode rejection would be infinite. Because infinite common-mode rejection is not realistic, R_{EE} is included in the small signal analysis.

Applying direct small signal analysis in conjunction with the superposition results in the following an equation

$$v_{ox,s} = A_{x1}v_{i1} + A_{x2}v_{i2} + A_{x3}v_{i3} + A_{x4}v_{i4} \quad (5)$$

The x in Equation (5) refers to each channel of output terms. The sixteen voltage gains, A_{11} through A_{44} , from (5) specify small signal operation of the circuit, where each gain is described as a response to the following loading conditions.

$$A_{xy} = \left. \frac{v_{ox}}{v_{iy}} \right|_{v_{ix}=v_{iw}=v_{iz}=0} \quad (6)$$

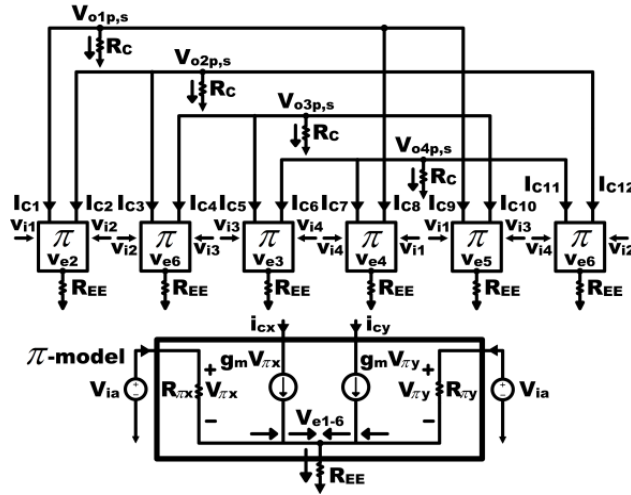


Fig 8. Small Signal π – model Analysis for the positive pair

The x represents the output term and y represents the input term. Given the fact, this circuit is a balanced and symmetrical architecture. Additionally, since there are two different configurations for the quadferential pair, a positive and negative (cross-coupled) option, there are four unique gain constant, A_{xyp} , A_{xyp} , A_{xxn} and A_{xyn} . The gain constants are defined as

$$\begin{aligned} A_{xyp} &= -\frac{g_m R_C}{2} \left(\frac{3 \left(1 + \frac{1}{B} \right)}{1 + \frac{1}{2B}} \right) & A_{xyp} &= \frac{g_m R_C}{2} \left(\frac{1}{1 + \frac{1}{2B}} \right) \\ A_{xxn} &= \frac{g_m R_C}{2} \left(\frac{3}{1 + \frac{1}{2B}} \right) & A_{xyn} &= -\frac{g_m R_C}{2} \left(\frac{1 + \frac{1}{B}}{1 + \frac{1}{2B}} \right) \end{aligned} \quad (7)$$

$$\text{where, } B = g_m R_{EE} \left(1 + \frac{1}{\beta_0} \right)$$

Inspection of Fig 8 reveals that this is a balanced system. The symmetry will be evident in the derivation for the small signal gain constants.

Typically, a differential circuit acts upon the differences at its inputs and ignores the part of the signal that is common to each.[6] A quadfferential pair is no different. To examine this behavior, the difference voltages that the quadfferential pair responds to in terms of generic gain constants are

$$\begin{aligned} v_{od(1,2)} &= \frac{A_{11} - A_{12}}{2} v_{id(1,2)} + \frac{A_{23} - A_{22}}{4} v_{id(2,3)} \\ &+ \frac{A_{14} - A_{11}}{4} v_{id(4,1)} + \frac{A_{11} - A_{13}}{4} v_{id(1,3)} + \frac{A_{22} - A_{24}}{4} v_{id(4,2)} \end{aligned} \quad (8)$$

$$\begin{aligned} v_{od(2,3)} &= \frac{A_{21} - A_{22}}{4} v_{id(1,2)} + \frac{A_{22} - A_{23}}{2} v_{id(2,3)} \\ &+ \frac{A_{34} - A_{33}}{4} v_{id(3,4)} + \frac{A_{33} - A_{31}}{4} v_{id(1,3)} + \frac{A_{24} - A_{22}}{4} v_{id(4,2)} \end{aligned} \quad (9)$$

$$\begin{aligned} v_{od(3,4)} &= \frac{A_{32} - A_{33}}{4} v_{id(2,3)} + \frac{A_{33} - A_{34}}{2} v_{id(3,4)} \\ &+ \frac{A_{41} - A_{44}}{4} v_{id(4,1)} + \frac{A_{31} - A_{33}}{4} v_{id(1,3)} + \frac{A_{42} - A_{44}}{4} v_{id(4,2)} \end{aligned} \quad (10)$$

$$\begin{aligned} v_{od(4,1)} &= \frac{A_{12} - A_{11}}{4} v_{id(1,2)} + \frac{A_{43} - A_{44}}{4} v_{id(3,4)} \\ &+ \frac{A_{44} - A_{41}}{2} v_{id(4,1)} + \frac{A_{13} - A_{11}}{4} v_{id(1,3)} + \frac{A_{44} - A_{42}}{4} v_{id(4,2)} \end{aligned} \quad (11)$$

$$\begin{aligned} v_{od(1,3)} &= \frac{A_{11} - A_{12}}{4} v_{id(1,2)} + \frac{A_{33} - A_{32}}{4} v_{id(2,3)} \\ &+ \frac{A_{34} - A_{33}}{4} v_{id(3,4)} + \frac{A_{14} - A_{11}}{4} v_{id(4,1)} + \frac{A_{11} - A_{13}}{2} v_{id(1,3)} \end{aligned} \quad (12)$$

$$\begin{aligned} v_{od(4,2)} &= \frac{A_{22} - A_{21}}{4} v_{id(1,2)} + \frac{A_{23} - A_{22}}{4} v_{id(2,3)} \\ &+ \frac{A_{43} - A_{44}}{4} v_{id(3,4)} + \frac{A_{44} - A_{41}}{4} v_{id(4,1)} + \frac{A_{44} - A_{42}}{2} v_{id(4,2)} \end{aligned} \quad (13)$$

Inspection of Equation (8) through (13) reveals that the common-mode component is canceled. From the small signal gain constants, Equation (7) reveals that the differential output voltages for a positive quadfferential pair are;

$$v_{od(1,2)p} = -2Dv_{id(1,2)} + Dv_{id(2,3)} + Dv_{id(4,1)} - Dv_{id(1,3)} - Dv_{id(4,2)} \quad (14)$$

$$v_{od(2,3)p} = -2Dv_{id(2,3)} + Dv_{id(1,2)} + Dv_{id(3,4)} - Dv_{id(1,3)} + Dv_{id(4,2)} \quad (15)$$

$$v_{od(3,4)p} = -2Dv_{id(3,4)} + Dv_{id(2,3)} + Dv_{id(4,1)} + Dv_{id(1,3)} + Dv_{id(4,2)} \quad (16)$$

$$v_{od(4,1)p} = -2Dv_{id(4,1)} + Dv_{id(1,2)} + Dv_{id(3,4)} + Dv_{id(1,3)} - Dv_{id(4,2)} \quad (17)$$

$$v_{od(1,3)p} = -2Dv_{id(1,3)} - Dv_{id(1,2)} - Dv_{id(2,3)} + Dv_{id(3,4)} + Dv_{id(4,1)} \quad (18)$$

$$v_{od(4,2)p} = -2Dv_{id(4,2)} - Dv_{id(1,2)} + Dv_{id(2,3)} + Dv_{id(3,4)} - Dv_{id(4,1)} \quad (19)$$

$$\text{where, } D = \frac{g_m R_C}{8} \left(\frac{4 + \frac{3}{g_m R_{EE} \left(1 + \frac{1}{\beta_0}\right)}}{1 + \frac{1}{2g_m R_{EE} \left(1 + \frac{1}{\beta_0}\right)}} \right) \quad E = \frac{-g_m R_C}{8} \left(\frac{4 + \frac{1}{g_m R_{EE} \left(1 + \frac{1}{\beta_0}\right)}}{1 + \frac{1}{2g_m R_{EE} \left(1 + \frac{1}{\beta_0}\right)}} \right)$$

In the case of the differential output voltages for the negative quadfferential pair is represented by ‘‘E’’ instead of ‘‘D’’. From the evaluation of the differential output voltages for the positive and negative quadfferential pair, three observations arise. First, the arguments inside the brackets for the constants ‘‘D’’ and ‘‘E’’ are a result of the finite impedance from I_{TAIL} , R_{EE} . As it can be seen from ‘‘D’’ and ‘‘E’’, if R_{EE} is large, its effect is minimal.

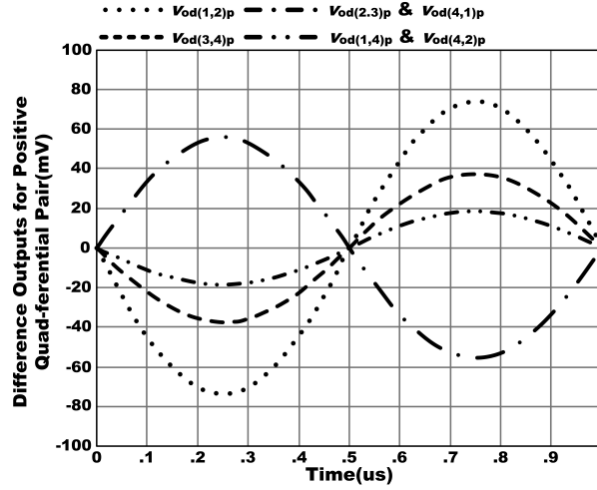


Fig 9. Transient simulation of output difference voltages for the positive quadfferential pair responding to two unique differential input voltages

However, if R_{EE} is small, it will reduce the gain. Second, the differential output voltages reveal that the corresponding input difference term of the desired output difference contributes twice as much when compared to the other input terms. Third, although there are six possible difference voltages as defined by the equations of the differential output voltages for the positive quadfferential pair, Equation (14) through (19) contain only five difference voltages. The ‘‘missing’’ difference voltage is absent because its channels do not impact the output difference voltage of interest. The simulation of the small signal behavior for the positive quadfferential pair responding to two unique input differential voltages is shown in Fig 9.

4. Design of a quadfferential amplifier

4.1. Input stage

A block diagram of the input stage for the quadfferential amplifier is presented in Fig 4(a). The quadfferential input stage is comprised of two quadfferential pairs. Therefore, the outputs of the positive and negative quadfferential pair are differential to each other

with respect to the same channel. The outputs of the quadfferential input stage are taken differentially. If a resistive load is present, then the input stage forms the following differential voltages

$$v_{ODX} = v_{OXP} - v_{OXN} \quad (20)$$

4.1.1. Large signal behavior

The output differential voltages that a quadfferential pair reacts to results in

$$V_{OD1} = \alpha I_{TAIL} R_C \left(\tanh \frac{-V_{ID(1,2)}}{2V_t} + \tanh \frac{V_{ID(4,1)}}{2V_t} + \tanh \frac{-V_{ID(1,3)}}{2V_t} \right) \quad (21)$$

$$V_{OD2} = \alpha I_{TAIL} R_C \left(\tanh \frac{V_{ID(1,2)}}{2V_t} + \tanh \frac{-V_{ID(2,3)}}{2V_t} + \tanh \frac{V_{ID(4,2)}}{2V_t} \right) \quad (22)$$

$$V_{OD3} = \alpha I_{TAIL} R_C \left(\tanh \frac{V_{ID(2,3)}}{2V_t} + \tanh \frac{-V_{ID(3,4)}}{2V_t} + \tanh \frac{V_{ID(1,3)}}{2V_t} \right) \quad (23)$$

$$V_{OD4} = \alpha I_{TAIL} R_C \left(\tanh \frac{V_{ID(3,4)}}{2V_t} + \tanh \frac{-V_{ID(4,1)}}{2V_t} + \tanh \frac{-V_{ID(4,2)}}{2V_t} \right) \quad (24)$$

As Equation (20) reveals, subtracting two individual voltages of the same channel (i.e. $V_{O1P,D}$ and $V_{O1N,D}$) results in the summation of three *tanh* functions.

When a circuit block consists of multiple inputs and outputs it is typically implemented in a differential signal chain. Thus, the operation of the quadfferential input stage with two unique differential inputs is of interest.

The individual inputs are paired to implement two unique differential signals. V_{I1} is differential with respect to V_{I2} , and V_{I3} is differential with respect to V_{I4} . Furthermore, being inherent in using two different input differential voltages, one differential voltage is larger in magnitude than the other as mentioned before. Thus, V_{I3} and V_{I4} are chosen as fifty percent less in magnitude with respect to V_{I1} and V_{I2} . The rate of change (dV/dt) between individual voltages is determined by setting the magnitude and rise/fall time of the input transients.

The resulting difference voltages are shown in Fig 5(a). Inspection of Fig 5(a) reveals that there are four unique difference voltages.

4.1.2. Small signal behavior

The small signal differential output voltages of the quadfferential pair is found by subtracting the same channel single-ended voltages from each other.

$$v_{od1} = \frac{-g_m R_C}{2} F_{v_{id(1,2)}} + \frac{g_m R_C}{2} F_{v_{id(4,1)}} - \frac{g_m R_C}{2} F_{v_{id(1,3)}} \quad (25)$$

$$v_{od2} = \frac{g_m R_C}{2} F_{v_{id(1,2)}} - \frac{g_m R_C}{2} F_{v_{id(2,3)}} + \frac{g_m R_C}{2} F_{v_{id(4,2)}} \quad (26)$$

$$v_{od3} = \frac{g_m R_C}{2} F_{v_{id(2,3)}} - \frac{g_m R_C}{2} F_{v_{id(3,4)}} + \frac{g_m R_C}{2} F_{v_{id(1,3)}} \quad (27)$$

$$v_{od4} = \frac{g_m R_C}{2} F_{v_{id(3,4)}} - \frac{g_m R_C}{2} F_{v_{id(4,1)}} - \frac{g_m R_C}{2} F_{v_{id(4,2)}} \quad (28)$$

$$\text{where, } F = \left(2 + \frac{1}{g_m R_{EE} \left(1 + \frac{1}{\beta_0} \right)} \right) / \left(1 + \frac{1}{2g_m R_{EE} \left(1 + \frac{1}{\beta_0} \right)} \right)$$

As seen in Equation (25) through (28), the common-mode terms are canceled when differential signaling is utilized, however the effect of the impedance from the tail current, R_{EE} , remains as shown in variable F . If R_{EE} is not sufficiently large enough for F to reduce to 2, then the full g_m can be ignored.

4.2. Gain stage

The gain stage for a single channel of the quadfferential amplifier is shown in Fig 4(b). The cascode current source transistors, Q_{P5} through Q_{P8} , receive their bias from I_{TAIL} via the differential pair Q_{N9} and Q_{N10} . The transistor Q_{N9} and Q_{N10} control the output common-mode level of the amplifier by setting the appropriate bias level (as determined by the input level on the V_{ocm} pin) at the output by modulating the currents in Q_{P11} and Q_{P12} .

The Wilson current mirror[10], transistors Q_1 through Q_4 , is biased by Q_8 such that $I_{C3} = I_{C5}$. It translates the transconductance of the input stage, G_{m1} , to the high impedance node in the second stage. Theoretically, the transconductance of the input stage is equal to the second stage, G_{m2} . However, due to base current losses in the second stage, $G_{m1} \neq G_{m2}$. Furthermore, due to the emitter degeneration of Q_{N1} , only 96% of G_{m1} is translated by the Wilson current mirror to the high impedance node. The single-ended gain at the high impedance node is given by

$$A_{V-SE} = A_{V1}A_{V2} \quad (29)$$

$$\text{where, } A_{V1} \approx G_{m1}R_{O1}, R_{O1} \approx \frac{1}{g_{m1}} // R_{EE}$$

$$A_{V1} \approx G_{m2}R_{O2}, R_{O2} \approx R_{O5} // R_{O3}$$

The high impedance node, R_{O2} , consists of the output impedance of the cascode current source, R_{O5} , in parallel with the output impedance of the Wilson current source, R_{O3} .

From a qualitative perspective, if channel 1 is modulating while channels 2, 3, and 4, are equal and constant, channel 1 will be 9.54dB larger in magnitude than the other channels as listed in Table 1. When the absolute value of 9.54dB from Table 1 is normalized to channel 1, a 33% difference is realized between channels 1 and channels, 2, 3, and 4.

Evaluation of channel 1, from a quantitative perspective, yields the approximate single-ended gain at the high impedance gain node $A_{V-SE,CHN1} \approx 87.4\text{dB}$. The difference between $A_{V-SE,CHN1}$ and $A_{V-SE,CHN2}$ is attributed to the transconductance from the input stage. Where a $G_{m1,CHN1} = 11.7\text{mS}$ results in 87.4dB, a $G_{m1,CHN1} = 3.8\text{mS}$ yields $A_{V-SE,CHN2} \approx 77.5\text{dB}$.

Table 1. Single-ended Δ change for the negative quadfferential Pair

Channel	Input	Output
1	+1 Δ	+1.5 Δ
2	0	-0.5 Δ
3	0	-0.5 Δ
4	0	-0.5 Δ

Furthermore, the difference behavior can be examined from a qualitative perspective. With 1 input modulating as analyzed in input stage, the output difference between the modulating and non-modulating channel is 2.5 dB larger when normalized to a modulating channel, channel 1, as listed in Table 2. From a ratio perspective, when 1 input is modulating, the output difference between a modulating and non-modulating channel is 1.33 times greater when compared with the single-ended output of the modulating channel.

Table 2. Output difference when a +1 Δ is applied to v_{i1} and the remaining inputs are held constant

Output Difference	Magnitude normalized to Channel 1
$i_{O1} - i_{O2}$	+2.49 dB
$i_{O2} - i_{O3}$	No change (0 Δ)
$i_{O3} - i_{O4}$	No change (0 Δ)
$i_{O4} - i_{O1}$	+2.49 dB
$i_{O1} - i_{O3}$	+2.49 dB
$i_{O4} - i_{O2}$	No change (0 Δ)

4.3. Output stage

The output stage of a quadfferential amplifier is comprised of four voltage buffers arranged in a parallel configuration. Each buffer is comprised of a diamond voltage buffer and is shown in Fig 10.

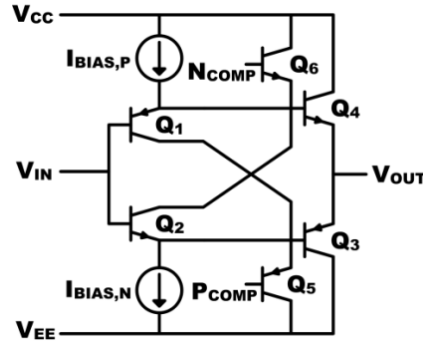


Fig 10. Voltage Diamond Buffer

One advantage in using the diamond buffer is the approximate equality between the input voltage, V_{IN} , and the output voltage, V_{OUT} . Thus, the gain from the input to output is approximately unity.

The input and output currents are dependent upon the ratio of Q_4 to Q_1 and Q_3 to Q_2 when $I_{BIAS,P}$ is same with $I_{BIAS,N}$. The maximum output current for the output stage is capable of sinking, and sourcing is limited by the base current of the PNP(Q_3) and NPN(Q_4) output devices such that

$$I_{BIAS,N} \geq \frac{\alpha I_{E3,MAX}}{\beta_{Q3}} \quad \text{and} \quad I_{BIAS,P} \geq \frac{\alpha I_{E4,MAX}}{\beta_{Q4}} \quad (30)$$

Since β_n for Q_4 is ≈ 111 and β_p for Q_3 is ≈ 85 , then Q_3 is the limiting factor to determine the DC output current drive. Thus, the requirement of driving $\mp 16.6mA$ in conjunction with $\beta_p \approx 85$ results in a minimum $I_{BIAS} \approx 200\mu A$.

The output impedance, R_O , is determined by the bias level of transistors Q_3 and Q_4 . With an Q_3 set to $200\mu A$ to satisfy output current drive and $V_t \approx 25.9mV$ at ambient results in $R_O \approx 86.5\Omega$. Additionally, Q_5 and Q_6 are added to the buffer to assist in base current compensation.

4.4. Bias cell

The core of a bias cell for the quadfferential amplifier is the Widlar bandgap circuit.[3] A magnified version of the bandgap is shown in Fig 11. This architecture is a common and proven bandgap circuit used in analog circuit design. The principle behind this bandgap is to produce two voltages with opposite temperature coefficients (TC'S) such that the reference is stable over temperature.

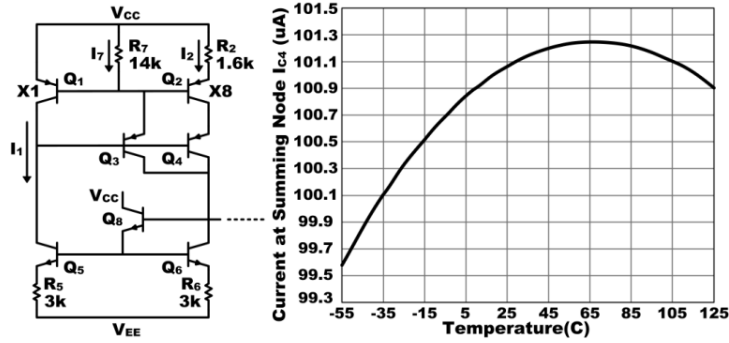


Fig .11 The bandgap circuit and simulation of Widlar bandgap over temperature

Typically, a stable current reference is created by summing a complementary to absolute temperature (CTAT) current with a proportional to absolute temperature (PTAT) current. From inspection of Fig 11, a unit current, I_{C5} , feeds I_1 . Neglecting losses due to base currents and assuming $\alpha = 1$, then $I_{C6} = I_{C5} = I_1$. I_7 is a CTAT current because it is determined by a V_{BE} which possesses a negative TC, approximately $-2mV/^\circ C$. Hence, I_7 decreases with temperature. The formation of a ΔV_{BE} between V_{BE1} and V_{BE2} creates the PTAT current. For equal area ratio, a ΔV_{BE} possesses a TC approximately equal to $+86\mu V/^\circ C$. I_2 is PTAT and I_7 is CTAT. I_2 and I_7 sum at the collectors of Q_3 and Q_4 establishing a stable current over temperature. Q_8 is a β helper and therefore reduces the non-ideal loss of I_B between I_{C6} and I_{C5} . Quantitatively, an expression for R_2 and R_7 are

$$R_2 = \frac{V_t \ln \left(\frac{I_1 A_2}{A_1 I_2} \right)}{I_2}, \quad R_7 = \frac{|V_{EB1}|}{I_7} \quad (31)$$

The unit current for this bandgap is $100\mu A$, therefore $I_1 = 100\mu A$. Splitting the current of $100\mu A$ equally in I_{C3} and I_{C4} results in $I_2 = I_7 = 50\mu A$. Accordingly, the initial area ratio between Q_1 and Q_2 is 1:2. With $V_{EB1} \approx 650mV$, $I_1 = 100\mu A$, and $I_2 = I_7 = 50\mu A$,

the initial values from Equation (21) and (22) for R_2 and R_7 are $R_2 = 1.44k\Omega$ and $R_7 = 13k\Omega$.

The simulations with a 1:2 area ratio (for $Q_1:Q_2$) results in a temperature curve exhibiting CTAT behavior. Increasing the ratio of the areas and introducing more PTAT current than CTAT current yields a better current reference over temperature due to the unit TC's associated between a V_{BE} and a ΔV_{BE} . A V_{BE} possesses a stronger unit TC than a ΔV_{BE} , thus, needing more PTAT current than CTAT current is valid. Simulation shows the best area ratio is 1:8. Varying resistor values to optimize overall temperature variation results in $R_2 = 1.6k\Omega$ from $1.44k\Omega$ and $R_7 = 14k\Omega$ from $13k\Omega$. The difference in resistor values between hand calculations and simulation results for an optimal curve over temperature is approximately 10%. As Fig 10 in simulation section shows, the change in current over a 180° range is $1.67\mu A$. At approximately $55^\circ C$, the TC is zero.

The Voltage reference, V_{CP} , biases the cascade transistors at the gain node such that there is zero V_{CB} at the current source transistor. If there is an emitter voltage mismatch, then temperature variances affect the bias circuit adversely. Emitter degeneration resistors are included with amount of degeneration set to $300mV$. This value allows the mismatch in current between different branches to be dependent upon resistor mismatch and not V_{BE} mismatch.

4.5. Stability and compensation

The closed loop transfer function of a quadfferential amplifier is of the canonical form

$$A_{CL}(s) = \frac{A(s)}{1+A(s)\beta} \quad (32)$$

$$\text{where, } A(s) = \frac{a(s)}{R_F+3R_G}, \beta = \frac{R_G}{R_F}, a(s) = \frac{1}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)}$$

The loop gain, $T(s)$, is

$$T(s) = A(s)\beta = \frac{R_G}{R_F+3R_G} \frac{1}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)} \quad (33)$$

Poles p_1 and p_2 are determined by the open loop transfer function of the amplifier, $a(s)$. Examination of the uncompensated loop gain Bode plot in Fig 12 reveals the cross-over frequency to be $1.5GHz$, with p_1 located at $1MHz$ and p_2 located at $358MHz$. The phase margin is -30° , therefore the system is unstable and requires compensation. In practical applications, the amplifier will drive loads of up to $50pF$. Inclusion of the load capacitance creates an additional pole, p_L . This pole is determined by C_{LOAD} in conjunction with the output impedance of the amplifier and results in a $T(s)$ of

$$T(s) = A(s)\beta = \frac{R_G}{R_F+3R_G} \frac{1}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)\left(1-\frac{s}{p_L}\right)} \quad (34)$$

To compensate the quadfferential amplifier a graphical linear approximation is utilized with Bode plots. A dominant pole is introduced such that the loop gain crosses $0dB$ at the location of p_L resulting in a minimum phase margin of 45° for $C_{LOAD} \leq 50pF$. To ensure the loop gain crosses $0dB$ with a phase margin of 45° , the calculation for the dominant

pole, p_1 , must consider characteristics from p_L . Designing for a cap load drive, $C_{LOAD} = 50pF$ and with an amplifier output impedance of 86Ω , p_L is

$$p_L = \frac{1}{2\pi R_0 C_{LOAD}} = 37\text{MHz} \quad (35)$$

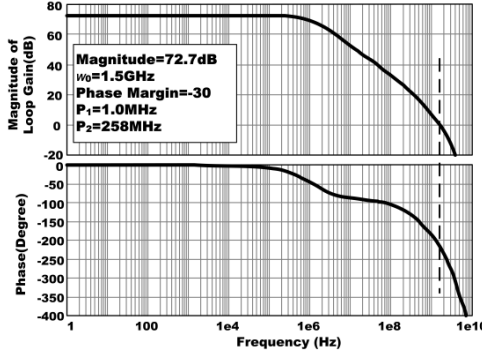


Fig 12. Uncompensated Bode plot of system loop gain, $|A(s)|$ and $Z_A(s)$

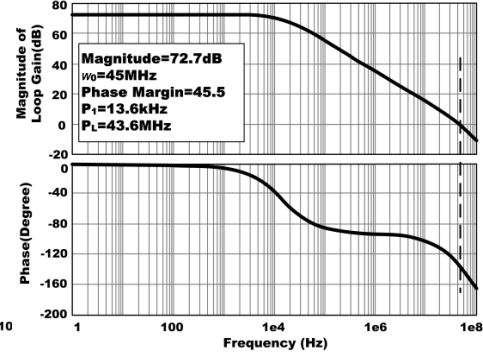


Fig 13. Compensated Bode plot for differential loop with $C_c = 7pF$

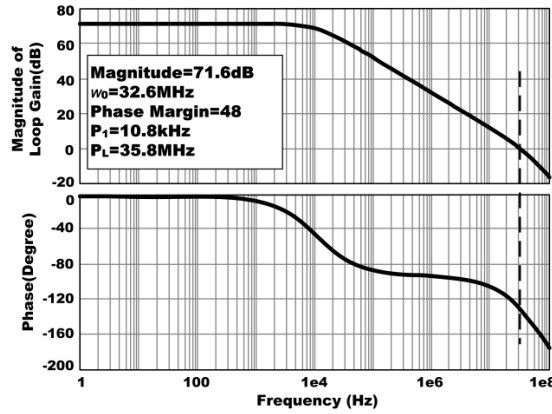


Fig 14. Compensated Bode plot for common-mode loop with $C_c = 7pF$

Using direct proportionality[8] and acknowledging poles p_L and p_2 are separated by approximately a decade, the following relationship between p_1 and p_L is obtained.

$$p_1 = \frac{p_L}{|T_0|} \quad (36)$$

where $|T_0|$ is the low frequency magnitude of the loop gain and p_1 is set by the high impedance gain node of the amplifier in conjunction with the compensation capacitor, C_c . The dominant pole, p_1 , is determined by calculating the compensation capacitor such that the location of the second pole, p_L , occurs where the loop gain crosses $0dB$. Iterating C_c empirically with the simulator yields 45° of phase margin with a $C_c = 7pF$. The iterative $C_c = 7pF$ is approximately 10% different from the graphical linear approximation technique used. The compensated loop gain is shown in Fig 13.

With the stability and compensation capacitor of the differential loop established, the common-mode loop requires investigation. A $C_c = 7pF$ results in the Bode plot in Fig 14. The phase margin of 48° for the common-mode loop is comparable to the differential loop. Therefore, the compensation capacitor of $C_c = 7pF$ satisfies the stability needs for both differential and common-mode loops.

4.6. Feedback

The quadfferential amplifier executes a feedback[4][9] via its input stage in combination with its feedback and gain resistors. To achieve negative feedback, from a qualitative perspective, the average of three outputs is fed back to the complementary summing junction. Table 3 in conjunction with Fig 15 provides an example of negative feedback for channel1. The outputs for channels 2, 3, and 4 sum together to form a net "negative" and are fed back to a net "positive" channel 1.

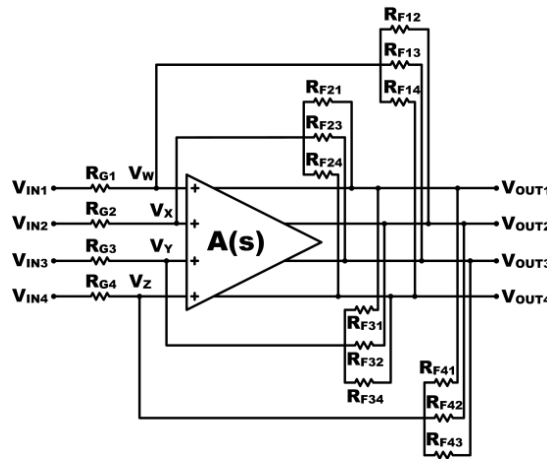


Fig 15. Typical configuration of the quadfferential amplifier

Table 3. Singel-ended Δ change for the negative quadfferential Pair

Channel	Input	Output
1	+1 Δ	+1.5 Δ
2	0	-0.5 Δ
3	0	-0.5 Δ
4	0	-0.5 Δ

5. Measurement result

Input stage is simulated in large signal and small signal. A simulation of the differential output voltages for the quadfferential input stage, with two unique input differential signals, is shown in Fig 17(a). The peaking in Fig 16 is a result of different rate of changes at the inputs, dV/dt , resulting from two unique differential voltages.

Additionally, *tanh* behavior is possible because the tail currents are identical. If the tail currents were different, the curves would exhibit more of an inverted log behavior resulting in a smaller linear region of operation.

A Simulation for a small signal model results in Fig 17 confirms the behavior derived in Equation (29) through (32). For example, with a $g_m = 3.8\text{ms}$, $R_L = 1\text{k}\Omega$, $\beta = 85$, $R_{EE} = 1\text{M}\Omega$, v_{od1} , in Equation (29), is 304mV . A simulation reveals v_{od1} as 290mV thus

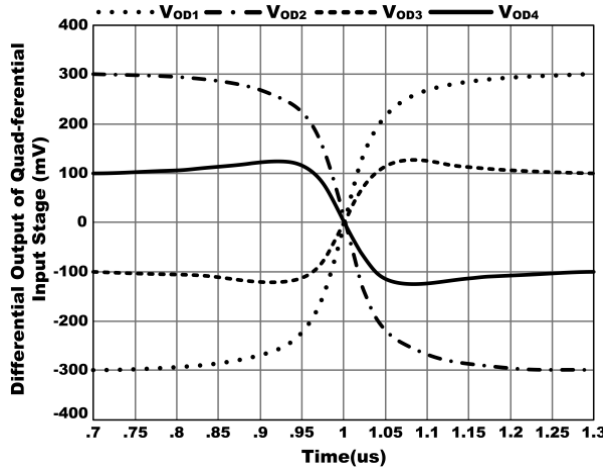
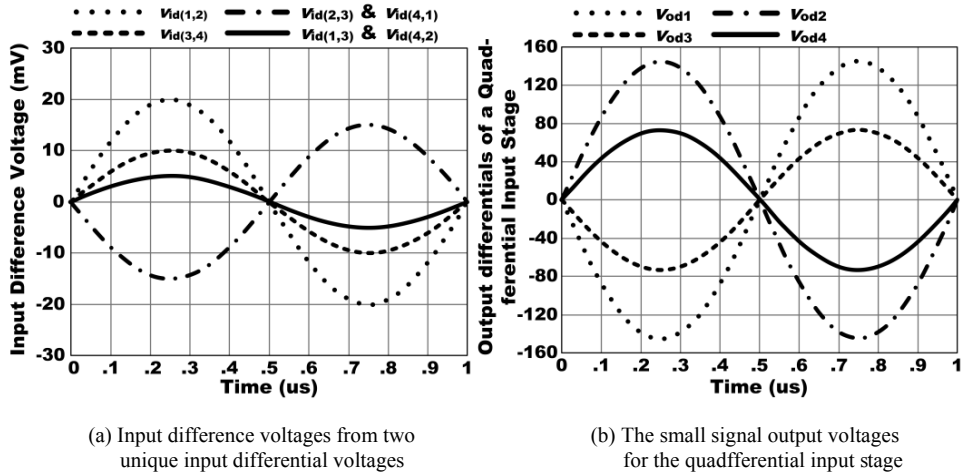


Fig 16. Simulation of differential output voltages by input difference voltages for the quadfferential input stage



(a) Input difference voltages from two unique input differential voltages

(b) The small signal output voltages for the quadfferential input stage

Fig 17. Simulation of the small signal output voltages for the input stage

simulation and Equation (29) correlate to within 5%. Relevant differential Bode plots are shown in Fig 18(a) and Fig 18(b). The inspection of Fig 18(a) reveals that v_{od2} , v_{od3} , and v_{od4} behave identically as represented by the dashed line. Furthermore, Fig 18(b) illustrates v_{od3} and v_{od4} responding identically when a differential signal is applied to channels 1 and 2.

The gain stage of a quadfferential amplifier is presented in Fig 4(b). The Simulation reveals a gain of 86.3dB, which deviates from theoretical analysis by 12%. Transient small signal output response of the quadfferential amplifier is presented in Fig 19 when conditions are the gain is 1, $R_F = R_G = 1k\Omega$, $R_L = 1k\Omega$, $C_L = 50pF$ and $C_C = 7pF$. R_F is a feedback resistor and R_G is gain resistor, which is not shown in this paper. The C_C is compensation capacitor that is derived as $7pF$. Fig 19 is the small signal output transient response for the quadfferential amplifier when conditions are the gain is 1, $R_F = R_G = 1k\Omega$, $R_L = 1k\Omega$, $C_L = 50pF$, $C_C = 7pF$.

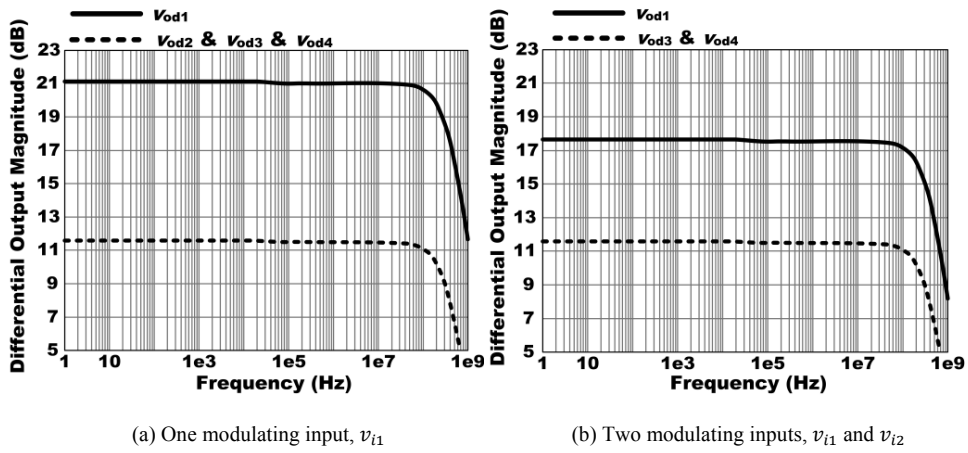


Fig 18. Differential Bode plot with the modulating inputs

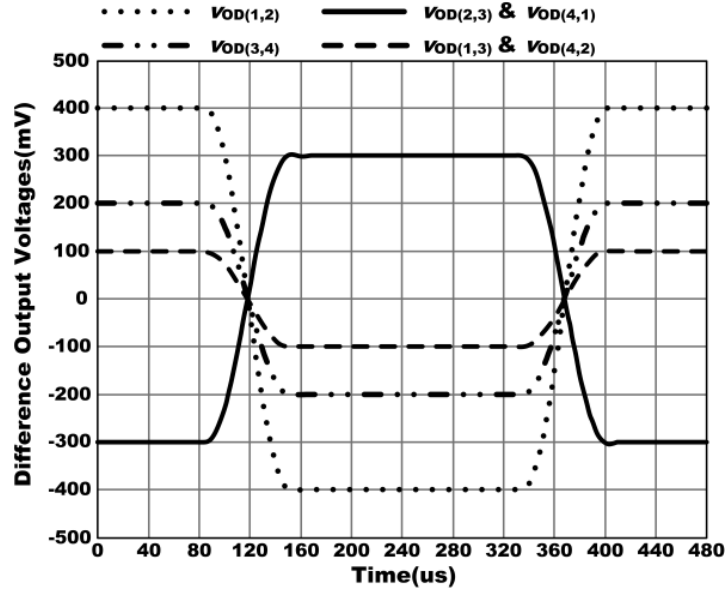


Fig 19. Small signal output transient response for $G=1$. $R_F = R_G = 1k\Omega$, $R_L = 1k\Omega$, $C_L = 50pF$, $C_C = 7pF$

Using statistical models for the transistors of the quadfferential input stage and running Monte Carlo simulations, Fig 20 shows the mean offset voltage of a quadfferential amplifier is $265\mu V$ with a standard deviation of $430\mu V$. Furthermore, the simulation of offset voltage, the mean common-mode rejection of a quadfferential amplifier is 126dB as shown in Fig 21.

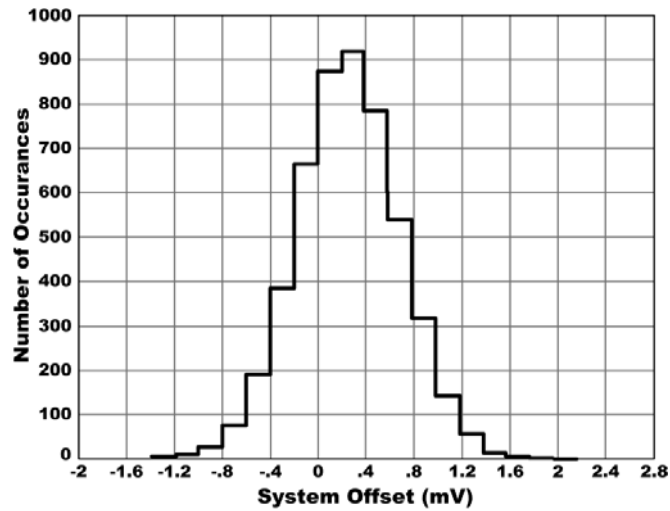


Fig 20. Simulation of offset voltage for the quadfferential amplifier

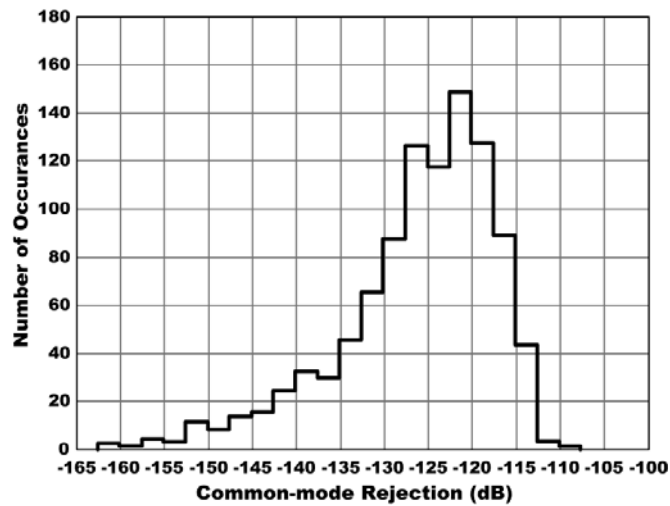


Fig 21. Simulation of common-mode rejection for the quadfferential amplifier

6. Conclusion

Transient simulations verified two fundamental aspects of the proposed quadfferential amplifier. First, it amplifies differences. Second, the output common-mode voltage is

controlled with the V_{ocm} input. Bode plots for one and two modulating inputs were included. The small signal differential bandwidth was 89MHz. Statistical models were utilized in performing Monte Carlo simulations to evaluate offset voltage and common-mode rejection. Offset voltage shows a mean of $265\mu V$ with a standard deviation of $430\mu V$. Common-mode rejection showed a mean of 126dB. The propose quadfferential amplifier is actually being used in real commercial products for CAT5 cable.

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