

The Novel Switched-Capacitor DC-DC Converter for Fast Response Time and Reduced Ripple

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Abstract—A novel voltage regulation scheme to control the number of multi-phase and frequency for Switched-Capacitor(SC) DC-DC converters is presented. The controller adjusts the number of interleaved phases with the size of switches. In addition, switching frequency of SC DC-DC converter is increased to reduce output ripple voltage when output load current is low. 16phase 2:1 SC DC-DC converter is designed in 45nm standard CMOS process using the proposed scheme. The converter with new control technique achieves fast response and low Vout ripple under fast varying currents. Maximum output voltage ripple(Vripple) is less than 15mV and maximum response time is less than 0.2us with 4mA. Normal Vripple is less than 2mV.

I. INTRODUCTION

As demand on SOCs increases, there have been researches to integrate the DC-DC converters used in portable consumer electronic products such as cell phones, personal digital assistants, and notebooks on the same chip as other cores. However, they still need off-chip inductance for high efficiency, which becomes an obstacle in achieving low cost and minimal size systems. In recent years, as VLSI technology and design techniques develop, SC DC-DC converters get more attention again[1,2] because they do not need external inductance any more making it possible for the converter to be integrated on chip.

On-die capacitors have higher Q(quality) factor and higher power density than on-die inductors. Therefore, it becomes possible to accomplish higher efficiency and higher power density Switched-Capacitor (SC) voltage regulators [3]. However, the output ripple of the SC converters often exceeds the tolerable limits of digital circuits [4]. Recently, SC regulators are investigated as a viable solution for on-die voltage conversion, where multi-phase interleaving is explored as a mitigation of the output ripple. On the other hand, the operating frequency of the on-chip converters is increased in order to achieve higher power densities [5]. This imposes difficulties in the regulation and stability of those converters with increased number of interleaved phases. In addition, the control loop of those converters should have faster response time and low power consumption in order to deliver high performance digital circuits.

SC converter with double-bound hysteretic control has been proposed in [7], where the lower-bound determines the SC converter switching frequency while the upper-bound sets the number of interleaved phases. By reconfiguring the number of interleaved phases with the switching frequency, the maximum operation frequency of the comparator is reduced. However, the SC converter scheme controls only the number of interleaved phases and switching frequency in the conventional converters.

This paper proposes and demonstrates a novel control scheme using additional switches and modified interleaving scheme in order to reduce maximum frequency and output voltage ripple. In addition, the proposed controlling scheme has the capability to deliver regular output voltage with variable output load current.

The steady-state analysis of 2:1 SC converter is discussed in section II, and Section III describes the proposed control scheme to reduce output ripple voltage and to improve the response time. The circuit implementation and simulation of the proposed 16-phase interleaved SC converter using 45nm standard CMOS technology are described in Section IV, followed by the conclusion in section IV.

II. ANALYSIS OF SC DC-DC CONVERTERS

A. Output ripple of SC DC-DC converter

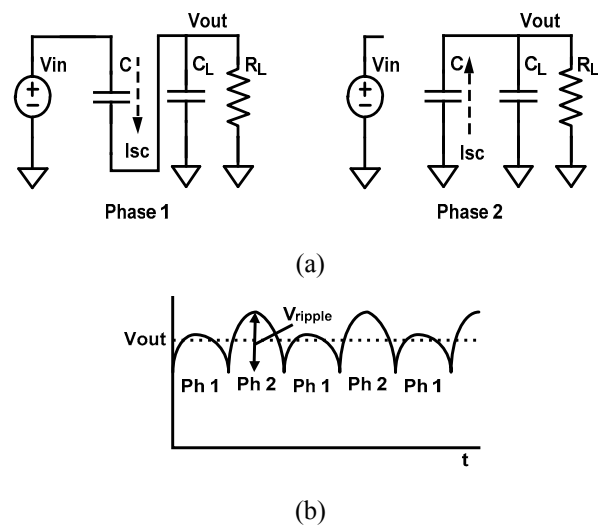


Figure 1. (a) Simplified 2:1 SC converters schematic. (b) SC output voltage

Figure 1 shows the principle of 2:1 SC DC-DC converter using only one transfer capacitor [6]. A load capacitor C_L is charged from V_{in} through a charge transfer capacitor C . In steady-state, assuming that C_L is held at the voltage V_{out} , C will be charged by V_{in} and C_L will be discharged in phase 1. Then, in phase 2, charge of C will be shared with C_L and it is discharged making V_{out} a half of V_{in} if C and C_L are same. The maximum V_{ripple} in phase 1 is less than the ripple in phase 2 since the discharge is done by only C_L , and the difference is decreased as switching frequency increases.

The SC converter current, I_{sc} , consists of charge pulses for 2:1 SC converter in the slow switching limit (SSL). The pulses are transferred to the output capacitor C_L and hence result in increasing of V_{out} . Then, the V_{out} is decreased by R_L with RC time constant. The difference between maximum V_{out} and minimum V_{out} is V_{ripple} . The relationship between V_{ripple} and C_L in the SSL is described as following equation.

$$V_{ripple} = \frac{I_{load}}{2f_{sw}C_L} \quad (1)$$

The SC converter switching frequency f_{sw} is proportional to the load current assuming a voltage regulation loop is applied in order to obtain the desired output voltage level. As a result, the peak-to-peak output V_{ripple} is almost constant with the I_{load} .

Optimization of the SC converter against different loss components results in the converter's operation in the region between the slow switching limit and the fast switching limit near the maximum load and switching frequency [7]. As the load current I_{load} increases and approaches its maximum value, the difference between the exponentially decaying SC current and the output load current I_{load} decreases. This current difference is integrated in the output capacitor C_L and forms the output voltage ripple. Therefore, the output voltage ripple decreases as the load current increases near the fast switching limit.

The SC converter's maximum output ripple is inversely proportional to the switching frequency as the load current approaches its maximum value. As a result, a lower number of interleaved phases are needed to satisfy the required peak-to-peak output ripple. Therefore, the number of interleaved phases can be reduced as the frequency increases. Therefore, a significantly lower comparator switching frequency is required.

B. Switching power loss

If it is assumed that all the switches are identical, the power loss of the switch can approximated as

$$P_{sw} = 4C_{ox}WL V_{DD}^2 f_{sw} \quad (2)$$

Where, C_{ox} is the oxide capacitance per unit area, L is channel length, and W is the width.

The factor 4 in the equation (2) represents that four switches are turned on and off every cycle. In practice, 4 switches consist of each of 2 PMOS and 2 NMOS for high efficiency. Because the switch loss is proportional to W as well as f_{sw} and I_{load} is not increased as same rate of rising of f_{sw} [1] W and f_{sw} should be optimized for high efficiency.

III. PROPOSED CONTROL SCHEME

A. Proposed Control technique to reduce ripple

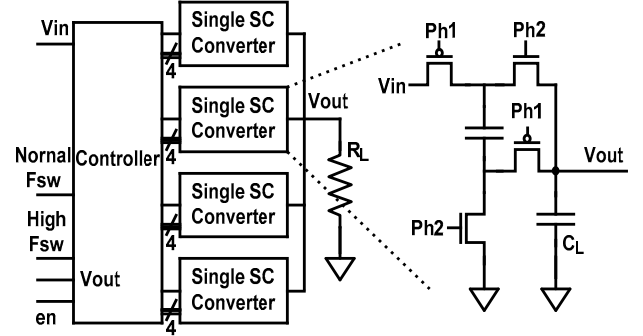


Fig. 2. The block diagram of the proposed 4 phase SC converter

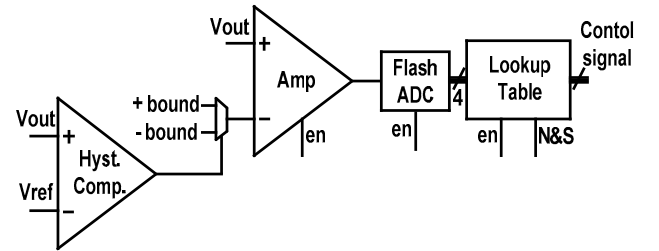


Fig. 3. The block diagram of proposed controller

Fig 2 shows the block diagram of the 4 phase SC converter. Each single SC converter consists of two PMOS and NMOS switches and transfer capacitor C and load capacitor C_L . The size of C and C_L of the single 2:1 SC converter are 150pF. For 1mA output current at 0.8V, 4 single converters are required. Ph1 and ph2 are non-overlap clocks with 180 degree difference. Fig 3 shows the block diagram of the proposed controller. The controller consists of hysteresis comparator, Flash ADC, Lookup table, and several digital logics. As the output load current needs to increase, the controller turns on the single SC converters until the output current becomes strong enough. Two voltage references are used, which are +bound and -bound as shown Fig 4. The two reference voltages are used to generate the control signals to turn on (when V_{out} is less than V_{ref}) or off (when V_{out} is larger than V_{ref}) the single SC converter units using the 4 bit lookup table outputs depending on the output voltage magnitude. The flash ADC keeps converting the amplifier output to feed the inputs to the lookup table. Once the V_{out} reaches the required voltage, the loop maintains the

regulated output voltage with acceptable ripple voltage. Because the comparator has hysteretic property, normal output voltage ripple can be ignored. In more specific, if V_{out} is larger than V_{ref} , the controller reduces the number of interleaved phases. If output load current is increased due to decreased R_L , then V_{out} is reduced. Then, the controller increases the number of interleaved phases and the amplifier the difference between V_{out} to $-$ bound to produce larger output to turn on more single SC converter units. The circuit works in the similar way for the opposite case.

Total output current is determined depending on the number of single SC converter. In order to control output current more specifically, the controller adjust the effective size of the switches. Figure 5 shows the structure of one of the two PMOS switches for phase 1. The structure of witches of NMOS is similar to PMOS. The single SC converter has four switches and the each switch is composed as four different sizes. After finishing decision of the number of interleaved phases, the controller decides the size of effective switches using the result of the 4-bit ADC by controlling the resistor of MOSFET. The lookup table has the pre-characterized data for regulated output voltage.

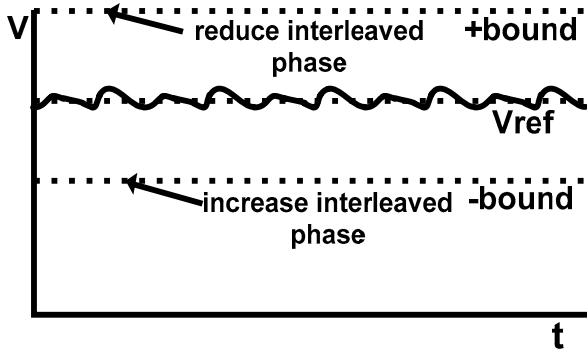


Fig. 4. Output voltage of single SC converter with bounds for control

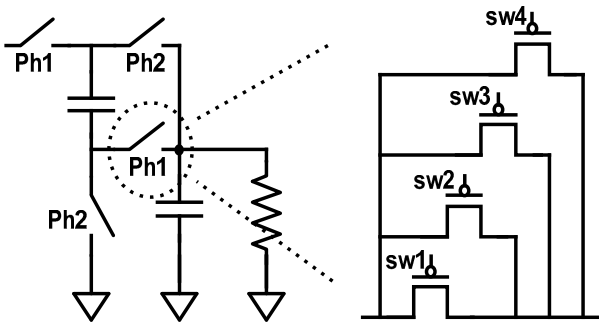


Fig. 5. The switch structure of single SC converter

B. Proposed control scheme for fast response time

As can be seen in equation (1), V_{out} ripple is increased if C_L is small. Therefore, if low output load current is required, the number of interleaved phases needs to be reduced. In this case, the switching frequency should be increased to have low ripple voltage as can be seen from equation (1) because the total value of C_L is decreased by having low number of interleaved phases. If less than three interleaved phase are required, high switching frequency mode is enabled making the switching frequency increase from 20MHz to 50MHz in this high switching frequency mode.

Even if there have been efforts to reduce the response time with varying output load, the result of response time still has not been satisfied. Therefore, high frequency mode is adopted during the first 0.2us whenever the number of interleaved phase changes to accomplish fast response time. 0.2us is enough time for the single SC converter units to settle down. The extra hardware to control this high frequency mode is minimal, which is less than 10% of the total hardware. Whenever the number of phase changes, the control unit activates the EN signal to enable the circuit to work in high frequency mode.

IV. SIMULATION RESULT

In the previous section, the algorithm of the SC DC-DC converter was explained using 4 interleaving phase structure for simplicity. In this paper, the number of interleaved phases is expanded from 4 to 16 phases, and the 16-phase 2:1 fully integrated SC converter is implemented using the proposed control scheme in 45nm standard CMOS process. Each SC converter consists of four switches and two capacitors, C and C_L of 150pF. Each capacitor is implemented using MIM (metal-Insulator-Metal) capacitor. In practice, the voltage of V_{out} is not a half of V_{in} exactly because of parasitics of the switch and the capacitor [1]. The converter generates only 0.8V normal output voltage V_{out} instead of exact half (0.9V) of 1.8V input voltage V_{in} . The phases of clock for switch are phase1 and phase 2, which are non-overlapped clock. PMOS switches are used in phases 1 and NMOS switches are used in phase 2. C and C_L are charged up to V_{in} (1.8V) in the mode of phase1, and PMOS switch is preferred to reduce the switch resistance between drain and source. On the other hand, NMOS switch is preferred in phase 2 because the voltage across the switch during the phase 2 is at most half V_{dd} (0.9V). The range of the hysteresis of the comparator is 3mV, and the SC converter regulates the output voltage against load current variations from 0.1mA to 4mA. The maximum peak-to-peak output ripple voltage is less than 15mV. Maximum SC single phase switching frequency is 50 MHz, normal frequency is 20 MHz, and the 16-phase SC converter's clock frequency is 700 MHz. In addition, normal output voltage ripple does not exceed 2mV, which is lower than [7] by 50%. With Full load current the efficiency of the SC converter is 85%.

Figure 7 shows the waveforms of the transient response of V_{out} and I_{load} when I_{load} is changed from 0.5mA to 1mA. While V_{out} is dropping, the controller adds two single SC

converters since each converter can produce maximum 0.25mA. At the same time, the controller adjusts the effective size of the switches to reduce the Ron resistance of the switch. The normal output ripple after load current change is 1.5mV. Figure 8 shows the comparison of the transient response between the response of the high frequency mode and with the response without high frequency mode. By adding the high frequency mode, the response time is faster than the previous work. The third waveform in Fig. 8 shows switching frequency of the high frequency mode. As shown in the figure, the switching frequency is changed during 0.2us.

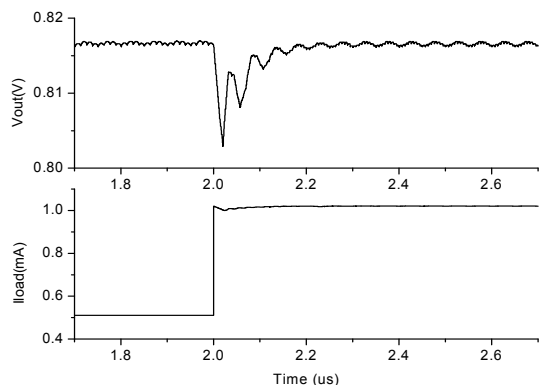


Fig. 6. SC converter transient response waveform with 50% load step

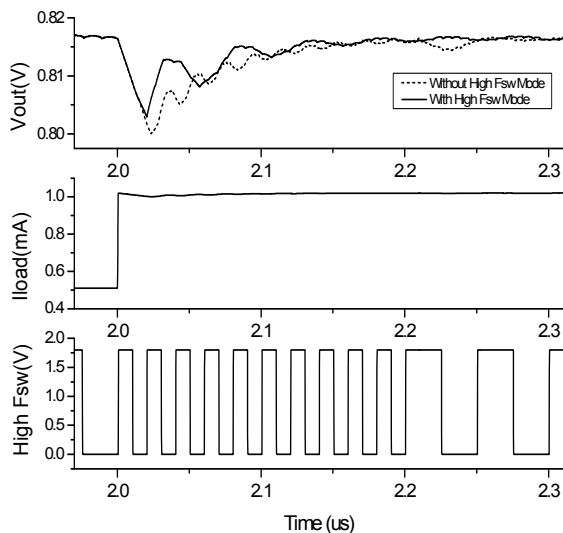


Fig. 8. The waveform with High switching frequency mode

Table 1. The comparison with previous work

Spec.	This work	[7]
Switching Frequency	20MHz	220MHz
Maximum output ripple	15mV	20mV
Normal output ripple	< 2mV	< 4mV
Load current variation	0.1mA ~4mA	2mA ~ 200mA

V. CONCLUSION

A novel control scheme of SC DC-DC converter is presented in this paper. As the output load changes, the number of interleaved phases and the size of switches are adjusted simultaneously. When I_{load} is changed, the frequency is jumped by 2.5 times to reduce the response time for few micro seconds. While low output load current is required, the switching frequency is also increased for low Vout ripple. Proposed SC DC-DC 2:1 (1.8V to 0.8V) converter using 16-phase was designed in 45nm standard CMOS process. Maximum Vout ripple was reduced to 15mV using 20 MHz switching frequency with variation of output load current between 0.1mA and 4mA while the ripple of the previous work is 20mV.

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