

# A Low Stand-by Power Start-up Circuit for SMPS PWM Controller

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## ABSTRACT

In this paper, a novel start-up circuit with a simple topology and low stand-by power during under voltage lockout (UVLO) mode is proposed for SMPS (switching mode power supplies) application. The proposed start-up circuit is designed using only a few MOSFETs, LDMOSs, and one JFET based on the analysis of the existing start-up circuits to address the power consumption and input voltage range issues of the conventional start-up. Simulated results using 0.35 $\mu$ m BCDMOS process demonstrate that the leakage current of the proposed circuit is less than 1 $\mu$ A after UVLO signal turns on. Setting time is less than 1ms when the load current changes from 10mA to 20mA and vice versa.

## Categories and Subject Descriptors

B.7.0 [Integrated Circuits]: General

## General Terms

Performance, Design, Economics,

## Keywords

Start-up circuit, SMPS, PWM, AC/DC

## 1. INTRODUCTION

The flyback topology is one of the popular choices as SMPS (switching mode power supplies) for low power applications such as adapter for mobile devices and auxiliary power supplies of the personal computer [1] and electrical home appliances [2]. Due to its insulating properties and simplicity, the flyback can be implemented using one switching component and one transformer. The switching component can be implemented using discrete or integrated power MOSFET, and control circuits are required to turn it on or off.

Most of the control integrated circuits for SMPS using the flyback topology require their starting current to charge a capacitance of the self-supply circuit in the integrated circuit to a certain level [3]. Such current comes from the starting circuit known as the bootstrap circuit (start-up), which is constituted in the simplest case by a resistance connected to the supply line [4].

When the voltage on the capacitance achieves a preset voltage

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value called start-up voltage, the self-supply circuit supplies the control circuit. The self-supply circuit is generally constituted by an additional winding performed on the main transformer of the switching power supply to which a suitable rectification and filtration circuit is connected.

Since there are ever increasing demand for the reduction of the supply consumption lately, the simple aforementioned resistance is replaced by the circuits that are active during the starting phase and inactive during the normal operation.

Lately there are also demands for monolithic devices for the SMPS that are comprised of both control circuit and the active starting circuit. However, the technologies used for these integrated circuits have limitation regarding the maximum sustainable voltage because the start-up circuits are hard to be integrated due to its high and wide input voltage range such as 80~275 VAC for universal operation. Therefore, there is a need for a bootstrap start-up circuit that has lower power consumption and accommodates a wide bias voltage range. To address these problems, 700V DMOS or BiCMOS process technology is often used for products.

This paper proposes a novel start-up circuit using only a few MOSFETs, LDMOSs, and one JFET based on the analysis of the existing start-up circuits to address the power consumption and input voltage range problems of the conventional start-up circuits.

The remainder of this paper is organized as follows. Section II introduces the basic concept of the start-up circuit by showing the conventional topologies as well as the state-of-the-art topologies. Section III describes the proposed start-up circuit, and the simulated results are discussed in Section IV to prove the proposed design, followed by the conclusion in Section V.

## 2. CONVENTIONAL START-UP CIRCUITS

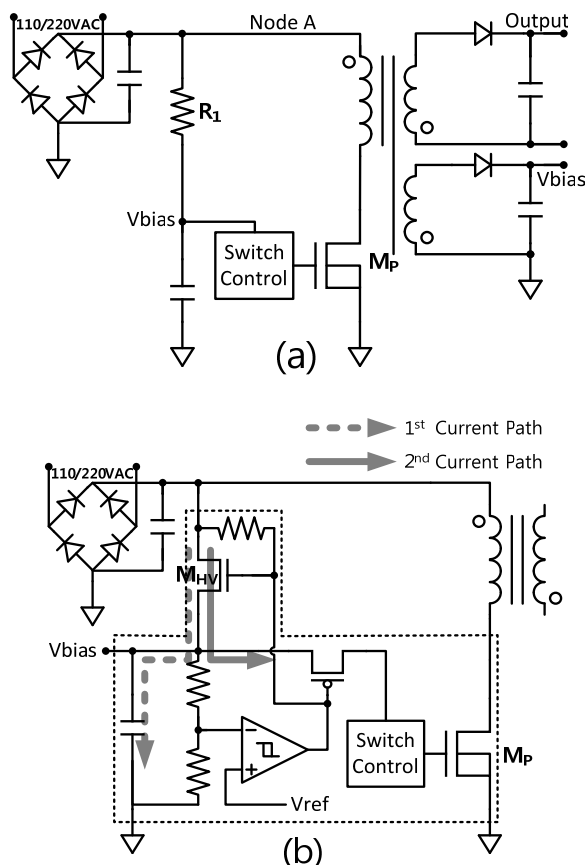
### 2.1 Prior Arts

Figure 1(a) shows a prior art SMPS using flyback topology that includes a full-wave bridge rectifier, a transformer, and control circuit using pulse width modulation (PWM) mode.

$M_P$  (Power MOSFET) controls the power switching of the primary winding of the transformer, and high input voltage is applied to the transistor during initial power-up.

The power to operate the control circuit is produced by the secondary winding side and is referred to as  $V_{bias}$  in Figure 1(a). However, at power start-up, controller will be without power because primary winding will be open and no voltage will be induced into the secondary winding because the controller is not switching during this time. To initiate such switching, node A with high DC voltage is tapped on bridge rectifier by the resistor,

and the current is filtered by the capacitor. This tap supplies just enough current through the resistor to start chip because significant amounts of power can be dissipated in the process of dropping the high voltage of the line to the low voltage required by chip. This waste of power is continuous, even after  $V_{bias}$  is available. This problem is severe particularly after  $V_{bias}$  is available, which makes the resistor dissipate all the more power at the highest expected voltage. Therefore, high wattage resistor type is inevitable and it requires extra space and air circulation.



**Figure 1 Conventional start-up circuits**

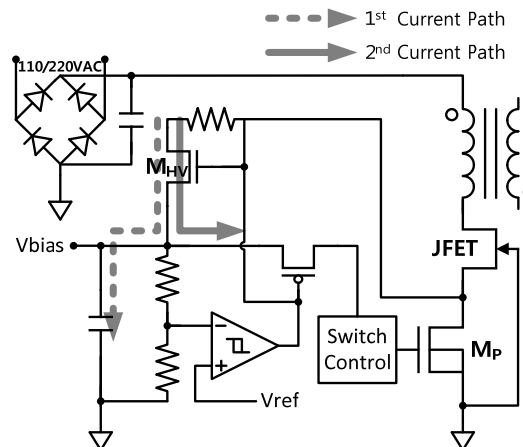
Figure 1(b) shows an evolved SMPS that is similar to the circuit shown in Figure 1(a), where the resistor  $R_1$  has been eliminated and several components have been included.

A voltage regulator inside the chip (dashed line in Figure 1(b)) allows the elimination of the high watts resistor and includes a high voltage pre-regulator transistor and supply power to PWM. A voltage is developed across the primary winding and induces a voltage in the secondary winding that supplies  $V_{bias}$ . With  $V_{bias}$  being supplied, the comparator operates to maintain the transistor off and no further high voltage power is required. Turning off high voltage pre-regulator saves power after start up, but such a function is more expensive to implement as it requires a high voltage transistor and extra pin with high voltage safety spacing. The high voltage transistor used in the pre-regulator of SMPS chips is usually relatively small device. The transistor's immunity to line transients is therefore limited. Thus, the pin associated with the transistor becomes a limiting factor for electrical static discharge (ESD) and safe operating area (SOA) rating of the switching regulator chip.

## 2.2 The-State-of-the-arts

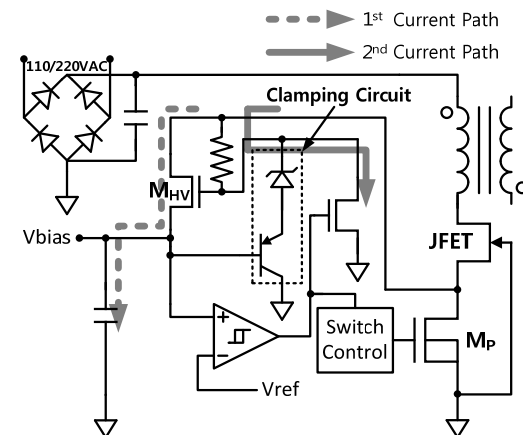
Figure 2 shows SMPS that includes a start-up circuit, which is very similar to Figure 1(b) but uses one JFET. The voltage of the drain node of the transistor  $M_P$  is lower than the voltage at the output of the primary winding (drain node of JFET) because the voltage at the output of the primary winding is dropped through the JFET, and the JFET supplies a regulator with power either temporarily or continuously to operate a PWM in the chip.

Advantages of the circuit are that the circuits not only save power but also reduce the number of pins of the chip while ESD and SOA concerns are reduced by using JFET [5].



**Figure 2 Schematic of the start-up circuits that uses JFET**

When a line voltage is applied to the drain of the JFET, the JFET's body is fully depleted with a typical source to substrate pinch-off voltage of 50V wherein the body of the JFET is often referred to as the drift region of the  $M_P$ . The JFET is operated in the saturation region. Since the source voltage of the JFET is limited to approximately 50V, most of the line voltage applied at a terminal of the transformer is dropped across the body of the JFET thereby providing a buffer from the line voltage. This protects  $M_V$  and the resistor connected to this node.



**Figure 3 Schematic of the start-up circuit using clamping diode**

Figure 3 is the schematic of another conventional start-up circuit. Clamping circuit limits the voltage appearing at the control electrode of  $M_V$  thereby limiting the current flowing between a

terminal of the transformer and an input terminal of the comparator. Clamping circuit includes an avalanche diode having a typical breakdown voltage of 10V, and a PNP transistor. The Clamping voltage is typically below 20V to prevent a long term degradation of the gate oxide of the  $M_{HV}$  (MOSFET for High Voltage). The 10V avalanche diode was selected for its low leakage, providing a sharp knee at low bias currents. The advantages of the circuit are that it provides a high ESD breakdown voltage and highly SOA. Furthermore, the start-up charging current can be adjusted from 5mA ~ 25mA by controlling the gate voltage of  $M_{HV}$ .

### 3. The PROPOSED START-UP CIRCUIT DESIGN

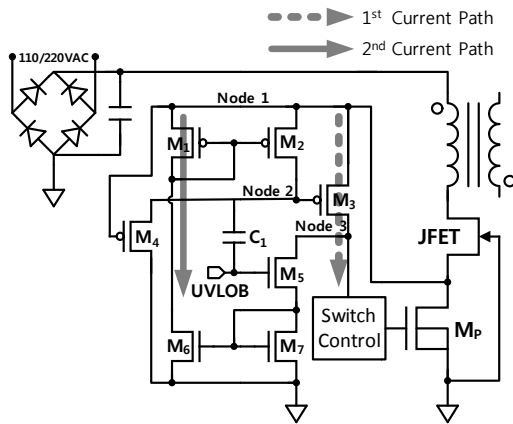


Figure 4 Schematic of the proposed start-up circuit.

Figure 4 shows the schematic of the proposed start-up circuit. The circuit consists of several MOSFETs, one capacitor, and one JFET. Because the role of capacitor C1 is to change the voltage of Node 2, C1 can be smaller size than 100fF. In the initial mode, the current through JFET goes to high voltage P-channel LDMOS transistors (M1 to M4). Initial voltage of Node 1 is zero and it makes M4 turn on initially, making M3 turn on in turn. As the voltage at Node 1 rises, M4 is turned off. Thus, the current flows through M3, M5, M6, and M7. This is the first phase of the start-up circuit operation, and this current path is indicated as 1<sup>st</sup> current path in the Figure 4. When UVLOB (complement of UVLO) is applied to the gate of M5 (when the voltage of UVLO goes to under 5V), the current flows through the 2<sup>nd</sup> current path shown in Figure 4. At this time, the voltage of Node 2 becomes high, making the current of M3 smaller. The total leakage current is expected to be very low because M4 and M3 are in linear region and there is no short circuit path. By switching the voltage of the gate of M5 and Node 2, start-up circuit is able to supply current to the controller. The Maximum voltage range of these nodes is equal to UVLO voltage so that the stress of M3 can be reduced.

As shown in Figure 5, the proposed circuit needs an internal signal called UVLO [6] to turn off the start-up circuit in order to save power and to protect the switch controller circuit when the input voltage or the voltage of the internal circuit of the controller is under specific voltage. In the proposed circuit, the signal of UVLO comes from the switch control block as shown in Figure 5, which shows the block diagram of the entire integrated circuit of controller including start-up, switch controller, and IO pin. The voltage of UVLO is controlled by the start-up circuit in the loop

for automatic operation of the circuit. UVLO voltage swings between 0V to 5V.

Not only UVLO voltage but also the reference voltage  $V_{ref}$  and bias current  $I_{BIAS}$  are generated by the voltage supplied from the proposed start-up circuit. Therefore, these signals should be independent of the supply voltage.

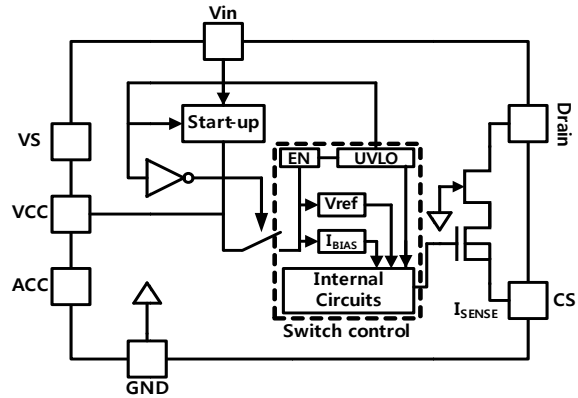


Figure 5 Block diagram of the integrated circuit including the proposed start-up circuit and controller.

The proposed start-up circuit is designed using only a few MOSFET, LDMOS, and one small capacitor for cost effective integration. However, in the case of PMOS such as M1, M2, M3 and M4, the drain voltages are very high with large voltage swing. Especially, M4 gate voltage can be up to 30V and it controls the gate voltage of M3 (Node2). Transistor M4 increases the circuit immunity against the change of Node 1 voltage to guarantee the start-up operation. Therefore, M4 transistor should have high breakdown voltage and its size should be carefully selected

### 4. SIMULATION RESULTS

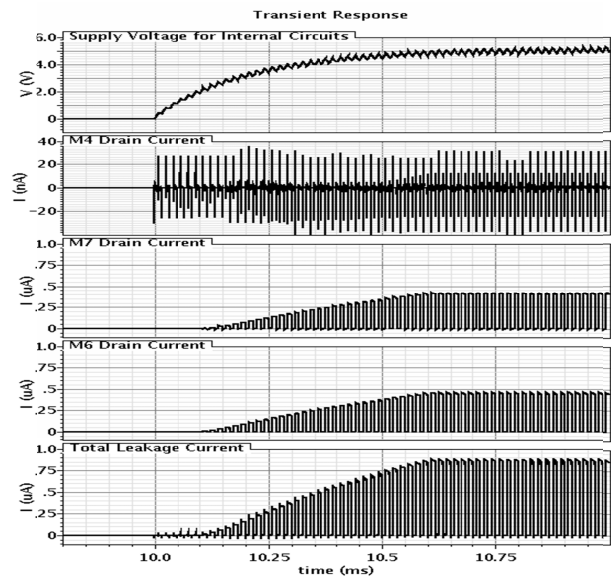


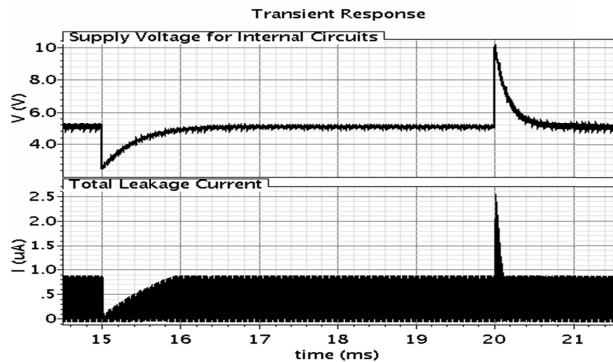
Figure 6 Simulation waveforms of the proposed circuit.

Figure 6 shows the waveforms of each nodes of the proposed start-up circuit. The fabrication process technology used for the proposed design is 0.35um 60V BCDMOS process and the

breakdown voltage of the discrete JFET transistor is 700V. The parameters of the BCDMOS process are shown in Table I. A variety of devices are available in the BCD process including normal MOSFET and LDMOS operating between 5V and 60V as well as high gain BJT, M5, M6 and M7 MOFETs in Figure 4 are designed using the transistor model with 8V supply voltage considering its operating voltage regions, and other P-channel MOS are designed using 36V Low V<sub>gs</sub> LDMOS transistor model. The output voltage of the start-up circuit goes to around 5V. Therefore, it is possible to integrate the JFET with controller using 700V BCDMOS process. The simulated average leakage current is 0.5uA and the possible operation current is up to 29mA, which satisfies the target specification. Figure 7 shows the transient responses when the load current changes from 10mA to 20mA (first dip) and 20mA to 10mA (second dip). Setting time is less than 1ms as shown in the Figure.

**Table I. Parameters of BCDMOS process**

Parameter	8V nMOS	36V LDpMOS
Electrical Tox [A]	300	130
V <sub>t_lin</sub> @ L=Min. [V]	0.6	0.8
Gate-source breakdown voltage [V]	12	5.0
Drian-source breakdown voltage [V]	8	36
Min. L [um]	2	1.8



**Figure 7** Transient response as changing required load current

**Table II. Comparison of the start-up circuits' characteristics**

	[7]	[8]	[9]	[10]	This work
JFET	O	O	O	X	O
Start-up On/off Logic	UVLO	UVLO	Time Delay Circuit	UVLO	UVLO
Leakage Current	Under 10uA	Under 10uA	Under 10uA	Under 15uA	Under 1uA
Cost	Mid	High	High	High	Low
2 <sup>nd</sup> or 3 <sup>rd</sup> winding feedback	Need	Need	Need	Need	None Need
Other Control Signal	None Need	None Need	None Need	Need	Need

Table II shows the comparison of the proposed start-up circuits with the ones that are commercially available. The proposed start-up circuit uses smaller area, which means low cost and low leakage current compared to other circuits because junction leakage is proportional to area as can be seen from the Table II.

## 5. CONCLUSIONS

This paper presents a novel start-up circuit for SMPS using flyback topology. The circuit is composed of only a few MOSFETs, LDMOSs, one capacitor, and one JFET to make it possible to integrate with lower cost and smaller area. In addition, ESD and SOA concern is reduced by using JFET and it can be integrated into a single integrated circuit using commercially available 700V BCDMOS foundry process. Therefore it is possible to reduce the number of pins of the controller chip by integrating start-up circuit, PWM, JFET, and Power MOSFET except transformer, which means the significant reduction of the cost of the controller. Simulation results show that the proposed circuit consumes a small current less than 1uA after UVLO signal turns on. The design demonstrates a novel and viable solution of the modern start-up circuit design.

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