Ultra-Low Voltage VCO Design Using Schmitt Trigger on SOI

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Abstract - *This paper presents a novel voltage-controlled-oscillator(VCO) on partially depleted 0.15μm Silicon-On-Insulator(PD-SOI) CMOS. The VCO shows phase noise from -79.98 dBc/Hz to -90.76 dBc/Hz at 600 KHz offset for various control voltages. The VCO consists of a novel Schmitt trigger and an ultra low voltage current source on PD-SOI with low temperature and supply voltage dependencies. The simulation results show that the proposed VCO on PD-SOI generates constant output amplitudes and good linearity between the control input voltage and the output frequency with less than 63μW power consumption at 0.7V power supply.*

Keywords: Silicon-On-Insulator (SOI), Voltage Controll-ed Oscillator (VCO), Schmitt Trigger Circuit

1 Introduction

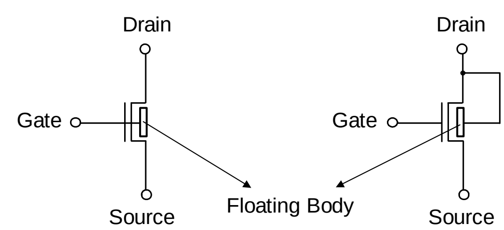
Voltage Controlled Oscillator (VCO) is a ubiquitous analog component in system-on-chip (SOC) system and falls into two main categories: the ring oscillator and the LC oscillator. Modern VCO circuit demands small size, low-power and high performance. Ring oscillator based VCO is widely used due to a relatively small area and robustness over process and temperature variations. However, the scaling of the circuit in dimensions and low supply voltage limit the signal amplitude, which in turn limits the signal-to-noise ratio and degrades system performance.

Especially, this is true for VCO in SOC systems of which high carrier power is necessary to lower the phase noise. Thus, new technologies and design techniques for analog and mixed-signal integrated circuits are critical to satisfy all the requirements. SOI CMOS is one of the new technologies and has been introduced as a low power solution and high performance with features, such as high current driving capability, low supply voltage, high current gain, and etc. Owing to small parasitic capacitance at the source/drain, SOI CMOS technology is suitable to integrate high frequency VCO [1]. Some works on LC oscillator based VCOs on SOI CMOS [2][3] and ring oscillator based VCOs on SOI CMOS [4][5] have been reported. However, VCO with ultra low voltage less than 0.7V has not been developed. This paper proposes a novel VCO circuits using Schmitt trigger on SOI to satisfy ultra low voltage features.

The paper is organized as follows. Section 2 reviews the basic concepts related to PD-SOI and DTMOS. In Section 3, a novel VCO consisting of voltage reference, current source, and the Schmitt trigger circuit is shown. Section 4 presents experiment results followed by conclusion in Section 5.

2 SOI Transistor

SOI transistor is known as a substitute for conventional silicon technology. The disadvantage of PD-SOI CMOS is the instability, such as hysteresis due to floating body, and self-heating effect. In order to reduce this disadvantage, several techniques for body-contact have been developed [1]. Among them, DTMOS results in a higher current drive than that of bulk CMOS. It gives a higher operating speed at very low voltage with little history effect [6]. The typical DTMOS is made by connecting the MOSFET gate to its floating body or the MOSFET drain to its floating body as shown in Figure 1 (a), and (b).



(a) Gate to Body connection (b) Drain to Body connection

Figure 1. SOI Dynamic Threshold MOS (DTMOS) Configurations

DTMOS on SOI limits the power supply voltage to below 0.7*V*. The low-voltage operation saves the power consumption of circuits. This paper introduces a novel VCO circuit using Schmitt trigger circuit operating at ultra-low voltage.

3 VCO using Schmitt Trigger Circuit

VCO can be implemented using the Schmitt trigger circuits, and Figure 2 shows the conventional VCO using Schmitt trigger circuit. The front MOSFET elements are a current source, where the current is controlled by the Control Voltage of MN1 and MN2. Depending on the current, saw pulse signal is generated on one capacitor in front of Schmitt trigger, and the Schmitt trigger generates square pulse signal.

Using the conventional circuits, the VCO can be implemented on PD-SOI. However, the simple current mirror of the VCO on the conventional circuits is not suitable to design VCO with ultra-low voltage (less than 0.7*V*). Also, the conventional VCO causes the current in M1 and M2 to be nonlinear. To make the current in the current source linearly related to V_C voltage, the new current source is proposed.

This paper proposes a novel current source that works well under ultra-low supply voltage with small temperature dependency as shown in Figure 3. After designing VCO circuit, the output frequency is changed by changing the value of C_{freq} capacitor.

The governing frequency equation for the VCO is given in Equation (1).

$$f_{VCO} = \frac{1}{t_1 + t_2} \tag{1}$$

where $t_1 = \dfrac{C_{freq}(V_H - V_L)}{I_{(MP2)}}$, $t_2 = \dfrac{C_{freq}(V_H - V_L)}{I_{(MN2)}}$, V_H and V_L are the switching threshold voltage of the Schmitt trigger circuit as shown in Figure 4(b).

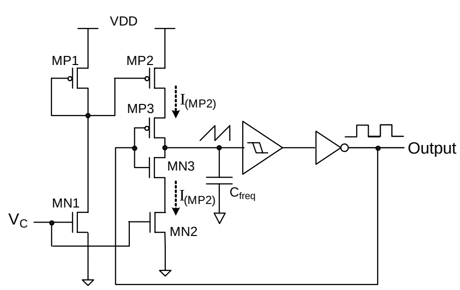


Figure 2. Conventional VCO using Schmitt Trigger

3.1 Current Generation

The current generator is a basic building block in analog circuits as a bias source for oscillator, amplifiers, and PLL(Phase-Locked Loop). The proposed current generator is designed to operate under ultra-low voltage. As shown in Figure 3, the reference current generator consists of a cascode self-biasing current source and a cascode voltage reference in order to bias MN8 MOSFET and make the MN8 operate in the triode region.

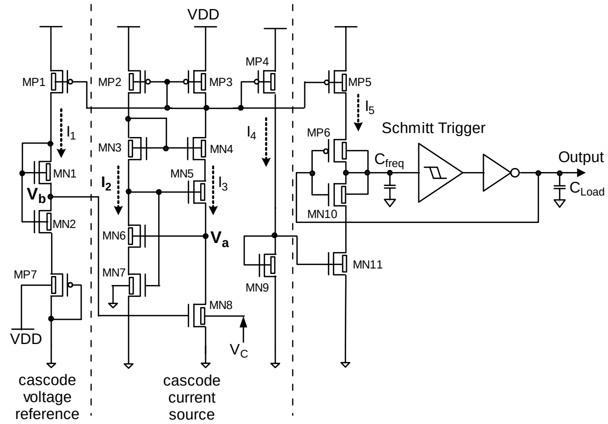


Figure 3. Proposed VCO using Schmitt Trigger

In the cascode self-biasing current source, V_a is determined by gate-source voltage of MN7 and MN5, and it is given by

$$\begin{aligned} V_a &= Vgs_{(MN7)} - Vgs_{(MN5)} \\ &= \sqrt{\frac{2I_{(MN7)}}{\beta_{(MN7)}}} + V_{th(MN7)} - \left[\sqrt{\frac{2I_{(MN5)}}{\beta_{(MN5)}}} + V_{th(MN5)}\right] \end{aligned} \tag{2}$$

where $V_{th(MN7)}$ is greater than $V_{th(MN5)}$ because the floating body of MN7 is connected to ground, and $W/L_{(MN7)}$ is greater than $W/L_{(MN5)}$.

Equation (2) gives an insight about the V_a variation due to temperature. If $I_{(MN7)}$ and $I_{(MN5)}$ are equal and independent on temperature, the low temperature dependence of the V_a is obtained to a certain extent since the positive temperature coefficient of the mobility and the negative temperature coefficient of the threshold voltage cancel each other.

To generate temperature-independent $I_{(MN7)}$ and $I_{(MN5)}$, and operate MN8 in the triode region, an appropriate V_b (V_{gs} for MN8) voltage and low V_a around 0.2*V* are required. Using zero-temperature coefficient biasing point of PD-SOI [7], the variation of the current through MN8 can be small in temperature variation. Typically around 0.4*V* is the zero temperature coefficient biasing point for V_{gs} of SOI-DTMOS. The current on MN8 is given by

$$I_{(MN8)} = I_2 = I_3 = \frac{V_a}{R_{(MN8)}} = V_a \times \left[\beta(V_b - V_{th(MN8)})\right] \tag{3}$$

where $R_{(MN8)}$ is the resistance of MN8 in the triode region.

The control voltage V_C is connected to the floating body of MN8 to use all the range from 0V to 0.7*V* as the control voltage. If an appropriate bias voltage V_b is applied to the gate of MN8, current $I_{(MN8)}$ is passed through MN8 even though V_C is equal to 0*V*.

To increase the output resistance and bias all the MOSFET in the saturation region except MN8, the cascode current source is used as shown in Figure 3. In the cascode voltage reference, in order to generate proper V_b, the gates of MN1 and MN2 are connected.

If the size of MN1 is greater than that of MN2, V_b is given by

$$V_b = Vgs_{(MP7)} + Vgs_{(MN2)} - V_{th(MN1)} \tag{4}$$

where MP7 should be PMOS in order to get higher threshold voltage than that of NMOS.

Finally, a constant I_5 is generated by the current source described above.

3.2 Schmitt Trigger Circuit

Schmitt trigger circuits are widely used for waveform shaping under noisy conditions in SOC systems. Better noise margin and noise stable operation are offered by the hysteresis of a Schmitt trigger circuits. Figure 4(a) shows the traditional Schmitt trigger circuit. The switching voltage V_L and V_H shown in Figure 4(b) are decided by the ratio of each MOSFET, which can be applied to PD-SOI implementation [5]. In [5], body-contact methods are used to remove floating-body induced hysteresis that causes uncertainty in switching time.

Figure 4(c) shows the proposed Schmitt trigger circuit, where DTMOS technique is used to reduce operational voltage and threshold voltage, and also Multi-Threshold CMOS (MTCMOS) with virtual V_{DD} and Ground node is used to make different switching threshold voltage(V_{stv}) in DC Voltage Transfer Characteristics (VTC). Equation (5) presents the basic equation to determine the inverter switching threshold voltage in saturation region.

$$I_D = \frac{\beta_n}{2}(V_{stv} - V_{tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_{stv} - |V_{tp}|)^2 \tag{5}$$

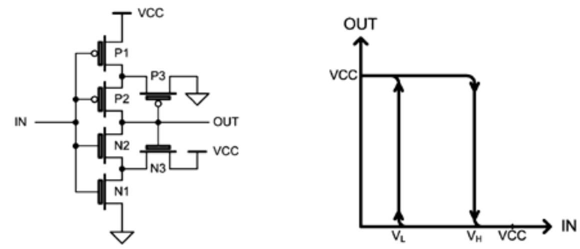
where I_D is the drain current, V_{stv} is the switching threshold voltage, V_{DD} is input voltage, and β_p and β_n are trans-conductance parameters of nMOSFET and pMOSFET, respectively.

The key point of the proposed circuits is to change the V_{DD} in each rising and falling transition of output to make different V_{stv} in the transitions. It assumes that logic Low is entered to Input initially, and then the Input is changed to logic High. The Output1 is decided by the voltage of both the V_x and V_y node to be set by output2 voltage value. The V_{stv} is also decided by the V_x and V_y, and from equation (5) it is given by

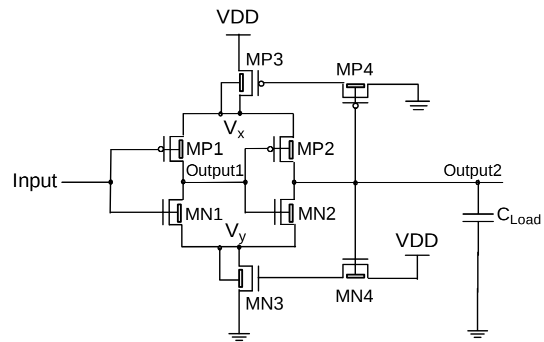
$$I_D = \frac{\beta_n}{2}(V_{stv} - V_y - V_{tn})^2 = \frac{\beta_p}{2}(V_x - V_{stv} - |V_{tp}|)^2 \tag{6}$$

$$V_{stv} = \frac{1}{1+\sqrt{\frac{\beta_n}{\beta_p}}}\left(\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_y + V_x - |V_{tp}| + \sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{tn}\right) \tag{7}$$

where V_x is the virtual V_{DD}, and V_y is the virtual ground.



(a) Traditional implementation (b) Transfer characteristics



(c) Proposed circuit

Figure 4. Schmitt Trigger Circuit

The same equations are used to decide the V_{stv} in case of High-to-Low transition of input that has a different V_{stv} value from the High-to-Low transition due to the different V_x and V_y. In the proposed circuit, all the MOSFETs are implemented using SOI DTMOS technique. It induces low-threshold voltage in ON state and high-threshold voltage in OFF state, which increases the speed of the circuit and decrease the leakage current of the circuit.

4 Experimental Results

The circuit is designed using Hspice in a 0.15μm BSIMSOI3.2 technology. Correct operation of this circuit is verified through simulation. The proposed VCO operates from 40 MHz to 725 *MHz* at 0.7*V* supply voltage. Figure 5 presents transfer characteristics of the proposed Schmitt Trigger circuit. In the transfer characteristics, a good hysteresis of the Schmitt trigger is demonstrated.

When the temperature is changed from -25^{o}C to 50^{o}C, the variation is within 8%. The linear relationship between the frequency and control voltage is shown in Figure 6. As the control voltage increases from 0*V* to 0.7*V*, the current increases almost linearly. The VCO gain is 0.48*MHz*/1*mV*, and the center frequency is 450*MHz*.

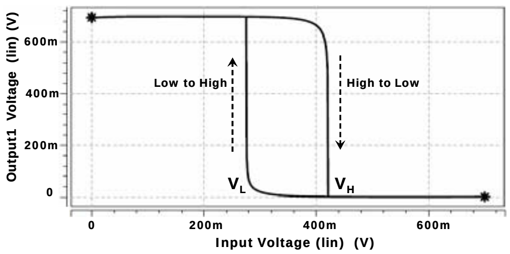


Figure 5. Transfer characteristics of the proposed Schmitt Trigger circuit

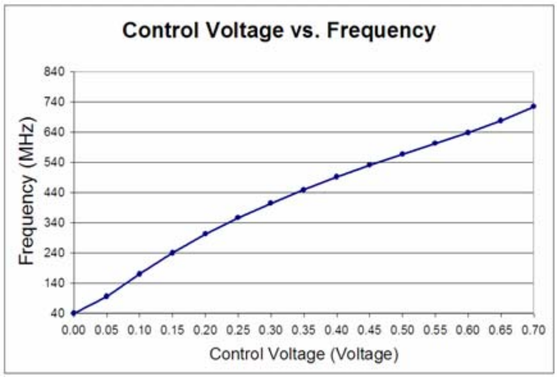


Figure 6. Frequency vs. Control voltage of the proposed VCO

10% supply voltage change causes only 9.3% frequency change (±21*MHz* from the center frequency). Finally, the average power is below 63μW at 0.7*V* power supply.

The proposed VCO performance is compared with previously published ring oscillator based VCOs as shown in Table I. It is presented that the new VCO reduces power dissipation significantly while providing other comparable VCO performance.

Table I: Comparison of different ring VCOs

Ref	Center Freq. (*MHz*)	Tech (μm)	VDD (*V*)	Phase Noise at 600 *KHz* Offset	Power (*mW*)
[8]	430	0.50	1.2	-80.3(dBc/Hz)	0.24
[9]	447	0.25	2.5	-99(dBc/Hz)	10
[10]	412	0.60	3.3	-85.9(dBc/Hz)	5.3
[11]	900	0.50	2.5	-105.1(dBc/Hz)	15.5
[12]	432	0.50 SOI	1.5	-93.5(dBc/Hz)	5.9
This Work	450	0.15 SOI	0.7	-79.98 to -90.76 (dBc/Hz)	< 0.06

5 Conclusions

A new ultra-low voltage VCO using a novel Schmitt trigger is proposed and simulated. The proposed VCO is composed of the Schmitt trigger and a novel current source controlled by bias voltage. By using SOI DTMOS methodology, the circuits operate under 0.7*V* power supply voltage (0.5~0.7*V*). Especially, the proposed VCO provides a very low temperature variation, and the VCO consumes much less power comparing with other published research results. Finally, the VCO demonstrates good frequency linearity with the control voltage.

This paper shows the efficiency of dynamic threshold MOS in both analog circuits and digital circuits, which is an essential device in reducing supply voltage.

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