

# Optimal Body Biasing for Minimum Leakage Power in Standby Mode

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**Abstract**—This paper describes a new power minimizing method by optimizing supply voltage control and minimizing leakage in active and standby modes, respectively. In the active mode, the control system determines the optimal trade-off between supply voltage and the forward body bias voltage to satisfy the performance requirement. In the standby mode, a new optimal body-bias technique in nanoscale CMOS technology is implemented to monitor subthreshold, gate tunneling, and band-to-band tunneling leakage current and reduce leakage current by optimal substrate bias voltage (forward or reverse biasing). The optimal body bias control system reduces the leakage current by up to 1000 times for ISCAS85 benchmark circuits designed using 32nm CMOS technology.

## I. INTRODUCTION

Mobile and portable devices require low power dissipation to extend battery lifetime. Lowering power supply voltage is one of effective schemes to reduce the power dissipation. A number of methods have been proposed to scale down the power supply voltage dynamically [1]. Even though they are effective in decreasing dynamic power dissipation, it does not help reduce leakage power effectively. As transistor geometries are scaled down aggressively, threshold voltage decreases to achieve high performance resulting in exponential increase in leakage current. Due to the continued scaling of technology, supply and threshold voltage, leakage power has become dominant in the power dissipation of nanoscale CMOS circuits. Therefore, optimal power dissipation for a given performance depends not only on power supply voltages but also on the device threshold.

To reduce the leakage power and increase threshold voltage in circuit level, adaptive reverse body biasing (ABB) technique has been proposed during standby mode [2][3]. The ABB decreases the subthreshold leakage current of the scaled MOSFET. However, it increases the depletion width of the MOSFET parasitic junction diode and rapidly band-to-band tunneling current between source/drain and substrate especially in halo implants. Recently, methods using forward body biasing in active mode have also been introduced [4]. The forward biasing increases the dynamic range of device threshold and improves the circuit performance by decreasing threshold voltage.

In addition, previous researches have shown that simultaneous supply voltage scaling and bidirectional body bias-

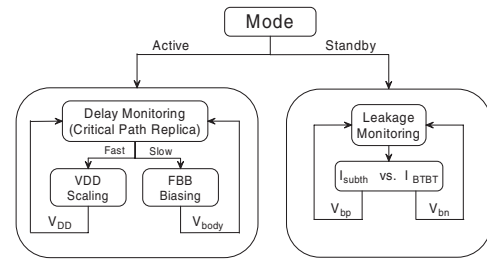


Fig. 1. Optimal  $V_{DD}$  and  $V_{TH}$  control

ing (forward + reverse biasing) are more effective to achieve high performance in active mode and low power dissipation in standby mode. Therefore, the dynamic voltage scaling and bidirectional body biasing determine the optimal trade-off between supply voltage and body bias voltage.

In this paper, a novel power minimizing method by optimal supply voltage and body voltage controls is introduced. In standby mode, a new leakage monitoring circuit is proposed to determine the optimal body bias voltage of CMOS circuits. The new circuits consist of leakage current monitoring circuit, voltage controlled oscillator, phase detector, and decoder-based digital-to-analog converter.

The remainder of this paper is organized as follows. Section 2 illustrates the analysis and modeling of the leakage current. Section 3 describes the novel power minimizing method. In Section 4, the new optimal body biasing circuit is presented. Results from the optimal body bias using the ISCAS85 benchmark circuits are shown and compared with zero body bias in Section 5 followed by conclusion in Section 6.

## II. POWER MINIMIZING SYSTEM

Optimal supply voltage and body bias voltage control can lead the high performance and low power dissipation in active and standby mode CMOS circuits, respectively. The control schemes are shown in Figure 1.

In active mode, the first step is to monitor delay of a critical replica to support operationally stable switching. In the second step, if the delay of the replica is faster than required delay, supply voltage control system starts to decrease the voltage, whereas forward body bias system starts to increase the voltage if the delay of the replica is slower than the

required delay. Using the control system, supply voltage and threshold voltage are adjusted.

In standby mode, the first step is to monitor each leakage component. In the second step, subthreshold leakage current and BTBT(Band-to-Band-Tunneling) leakage are compared each other. If the subthreshold leakage current is greater than the BTBT leakage, the reverse body bias will increase. On the other hands, if the subthreshold leakage current is smaller than the BTBT leakage, forward body bias will increase. It is found out that the optimal leakage point in the standby mode is the point where the subthreshold leakage is equal to the BTBT leakage [5]. Once the optimal body bias is detected, the body voltage adjustment is stopped.

The power consumed in a processor is the sum of dynamic, static leakage, and short circuit power. The short circuit power consumption occurs during signal transitions and is negligible if the circuit is carefully designed. Therefore, the total power is summarized by

$$P_{total} = C_{eff}V^2f + P_{leakage} \quad (1)$$

where the first term is dynamic power, and the second term is leakage power.

The leakage power is

$$P_{leakage} = P_{gate} + P_{subthreshold} + P_{BTBT} \quad (2)$$

Figure 2 shows the effect of body bias voltage and supply voltage on leakage power for a 30nm MOSFET technology NMOS. In this Figure, as supply voltage and body bias voltage decrease, leakage power is also decreased by reduction of  $I_{subth}$ . However, from a voltage around -0.9V to -2.2V body bias voltage, the leakage power increases by high  $I_{BTBT}$ .  $I_{gate}$  has a less effect on the power variation [3]. Therefore, the optimal body bias voltage to minimize the power dissipation is determined by the relationship between  $I_{subth}$  and  $I_{BTBT}$ .

In [6],  $I_{subth}$  and  $I_{BTBT}$  are simplified by

$$I_{subth} \approx A_S e^{B_S V_{Body}} \quad (3)$$

$$I_{BTBT} \approx A_b e^{B_b V_{Body}} \quad (4)$$

where  $A_b$ ,  $B_b$ ,  $A_S$ , and  $B_S$  is technology dependent constants and  $V_{Body}$  is the body bias voltage.

The minimum leakage power is given by

$$\frac{\partial P_{leakage}}{\partial V_{Body}} = 0 \quad (5)$$

where  $I_{gate}$  is ignored because the gate tunneling leakage is not sensitive to the body voltage.

From (2), (3), (4), and (5), the condition of the minimum leakage power is

$$B_S I_{subth} = B_b I_{BTBT} \quad (6)$$

Therefore, the ratio of  $B_b$  and  $B_S$  determines that of  $I_{subth}$  and  $I_{BTBT}$ . Assuming that the  $B_b$  and  $B_S$  are equal, the two leakage components have to be equal to optimize leakage power.

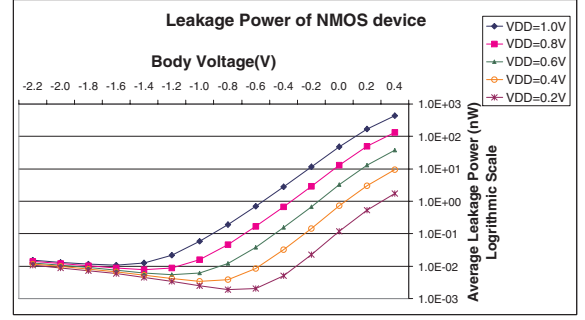


Fig. 2. Leakage Power as a function of body bias voltage and supply voltage

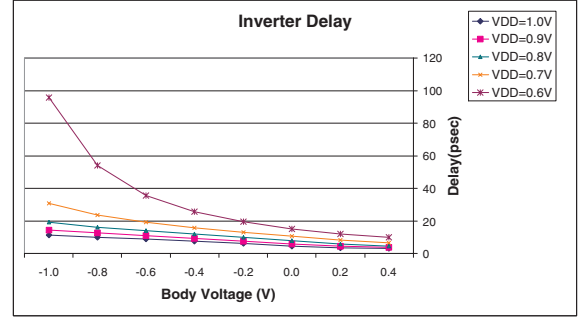


Fig. 3. Inverter delay as a function of body bias voltage and supply voltage

The delay of a gate is a function of both the power supply and the threshold voltage of the transistors. Thus, the delay of a single inverter is expressed as [7]

$$delay = \frac{K C_L V_{DD}}{(V_{DD} - V_{th})^\alpha} \quad (7)$$

where  $K$  is the proportional constant,  $C_L$  is the load capacitance, and  $\alpha$  is the velocity saturation.

Figure 3 is the SPICE result of a CMOS simulation for a 35nm technology and shows that reverse body bias and low supply voltage increase propagation delay whereas forward body bias decreases the propagation delay. Around 0.4V forward body bias, the delay is less sensitive to the supply voltage variation.

Based on the power and delay equation, the optimal supply voltage and body bias voltage are determined for high performance and low power.

### III. LEAKAGE IN NANOSCALE CMOS CIRCUITS

In off-state, the main components of leakage current are subthreshold leakage ( $I_{subth}$ ), gate induced drain leakage ( $I_{GIDL}$ ), gate tunneling leakage ( $I_{GATE}$ ), and bang-to-band tunneling ( $I_{BTBT}$ ) as shown in Figure 4(a). In on-state, gate tunneling leakage ( $I_{GATE}$ ) is the main component as shown in Figure 4(b) [3].

The GIDL(Gate Induced Drain Leakage) is a current from drain to substrate caused by high electric field between gate and drain, and thin gate oxide thickness and high supply voltage increase the GIDL leakage. The gate tunneling leakage

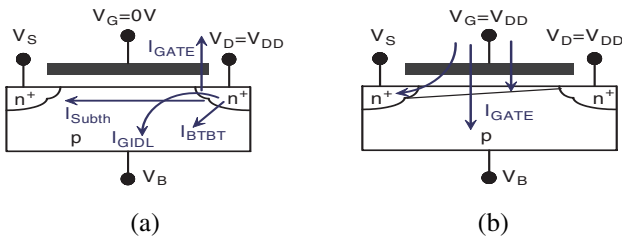


Fig. 4. Leakage Current in Nanoscale CMOS Circuits (a) Off-State Leakage Components (b) On-State Leakage Components

is a current flowing into the gate of the transistor by tunneling effect, and thin gate oxide thickness and high supply voltage increase the gate tunneling leakage. The subthreshold leakage is a weak inversion conduction current that flows the source and the drain of the CMOS transistor when  $V_{gs} < V_{th}$ . It increases exponentially due to reduced threshold voltage, and is a main leakage component in high forward body bias. Finally, the BTBT leakage is a current by electron tunneling across a reverse biased p-n junction between drain/source and substrate of the CMOS transistor. Therefore, in high reverse body bias, the BTBT leakage becomes a major contributor to the total leakage currents. [1] shows that the subthreshold leakage current and the BTBT leakage are much more sensitive to applied body bias than other two leakage components. The minimum leakage current is obtained when the subthreshold leakage current is equal to the BTBT leakage.

#### IV. OPTIMAL BODY BIASING TECHNIQUE IN STANDBY MODE

Reverse body biasing (RBB) is often used to reduce the leakage power of device. However, recent research has shown that if this RBB is too high, the leakage power can be actually increased due to the contribution of band-to-band tunneling currents. Therefore, this paper proposes a new optimal body biasing system to balance the subthreshold leakage with the BTBT leakage. The new system increases  $V_{th}$  by adjusting body voltage in the RBB direction, so as to reduce subthreshold leakage current. When the optimum body bias is detected, the body voltage adjustments is stopped to avoid excessive reverse body bias. In [4] and [6], leakage monitoring circuits are mentioned. However, their circuit models do not extract exact subthreshold leakage and BTBT leakage components in the replica circuit. Figure 5 shows our proposed method to reduce the leakage current in nanometer CMOS circuits. The system consists of five stages; Leakage Monitoring Circuit, Voltage Controlled Oscillator(VCO), Phase Detector, Decoder, and Digital-to-Analog Converter.

Leakage monitoring circuit separates the subthreshold leakage( $I_{subth}$ ) and BTBT leakage current( $I_{BTBT}$ ) from total leakage components. Figure 6 shows a new leakage monitoring circuit for NMOS device, where M2, M11, and M17 MOSFET is the replica circuits to generate leakage components, and M3/M4, M6/M10, and M15/M17 form current mirrors.

In the drain of M2, #1 current consists of gate tunneling leakage current( $I_{gate}$ ) and BTBT leakage current( $I_{BTBT1}$ ).

#2 current in the drain of M11 consists of gate tunneling leakage current( $I_{gate}$ ), BTBT leakage current( $I_{BTBT1}$ ), and subthreshold leakage current( $I_{subth}$ ).

In the source of M16, #3 current is generated, and it consists of gate tunneling leakage current( $I_{gate}$ ), BTBT leakage current( $I_{BTBT2}$ ), and subthreshold leakage current( $I_{subth}$ ). The leakage monitoring circuit for PMOS device consists of the same structure as the monitoring circuit for NMOS device.

Based on the generated leakage components, two current differential amplifiers are used to perform subtraction operation. Through M7, M8, and M9, (#2 current - #1 current) is obtained, whereas (#2 current - #3 current) is obtained through M15, M13, and M12. By the minus operation,  $I_{subth}$  is obtained in M9, and  $(I_{BTBT1} + I_{BTBT2})$  is obtained. The optimal body bias point is determined from the two components.

The separated leakage components are applied to the voltage controlled oscillator(VCO) to generate pulse waveforms proportional to the magnitude of each leakage. The VCO is designed using current starved inverters as shown in Figure 5, where M9 and M12 in the leakage monitoring circuit are connected the VCO.

The Phase detector consists of two D-latches, a nand gate. It generates UP and DOWN signals dependent on the phase difference between two signals from two VCOs.

Using the UP and DOWN signals, the decoder generates four bits signals. Finally, D/A converter generates body bias voltage using resistor network inside the D/A converter.

The PLL(Phased Locked Loop) based circuit provides the optimal body bias voltage to match the subthreshold leakage and the BTBT leakage currents.

#### V. EXPERIMENTAL RESULTS

The proposed optimal body bias technique using 32nm technology has been simulated in HSPICE and evaluated using ISCAS85 benchmark circuits. Table I shows the simulation results of each benchmark circuit both at room temperature( $25^{\circ}C$ ) and  $100^{\circ}C$ . Using leakage monitoring and the balance between subthreshold leakage and BTBT leakage, the new optimal body bias technique gives 1000X reduction in leakage power. Moreover, leakage power is far less sensitive to the temperature variation in the new technique because the optimal body bias is changed according to the temperature. Since the optimal bias results in the minimum leakage current for nanoscale device in standby mode, the power in active mode is also improved by applying the optimal body bias.

#### VI. CONCLUSION

This paper introduces a novel energy reduction technique using simultaneous optimal supply voltage and optimal body bias voltage. In the active mode, the control system determines the optimal trade-off between supply voltage and forward body bias voltage to satisfy the performance requirement. In the standby mode, a new optimal body-bias technique in nanoscale

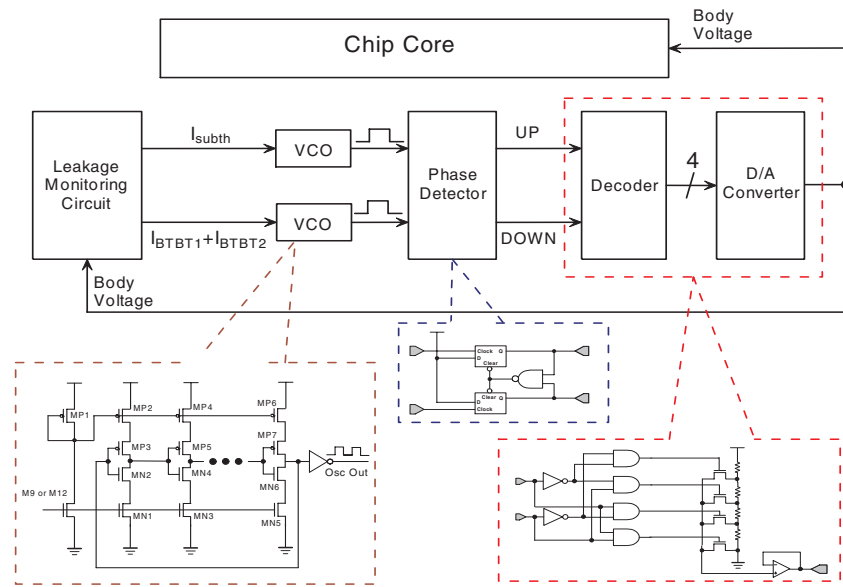


Fig. 5. Proposed Optimal Body Biasing System

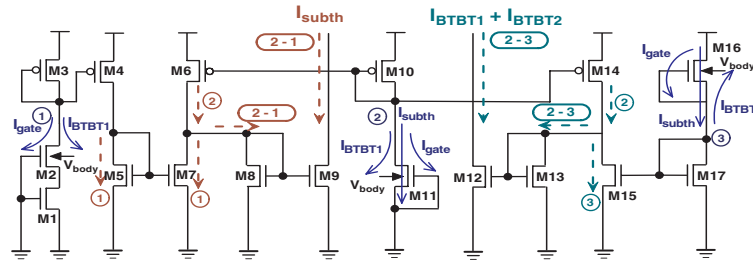


Fig. 6. Leakage Monitoring Circuit

TABLE I  
EXPERIMENTAL RESULTS FOR LEAKAGE POWER

Circuit	# of gates	Function	Leakage ( $\mu W$ ): Temperature = 25°C		Leakage ( $\mu W$ ): Temperature = 100°C	
			Zero Body Bias	Optimal Body Bias	Zero Body Bias	Optimal Body Bias
C432	160	27-channel interrupt controller	5.880	0.013	14.200	0.012
C499	202	32-bit SEC circuit	14.415	0.030	36.761	0.036
C1908	880	16-bit SEC/DED circuit	14.997	0.040	35.641	0.043
C1355	546	32-bit SEC circuit	21.488	0.039	53.703	0.036
C5315	2307	9-bit ALU	49.687	0.125	119.260	0.135

CMOS technology is implemented to monitor subthreshold, gate tunneling, and band-to-band tunneling leakage current and it reduces leakage current by applying the optimal substrate bias voltage (forward or reverse biasing). The results show that the optimal body bias produces high energy reduction in nanoscale CMOS transistor and the feedback loop of the proposed technique compensates for variation in temperature and supply voltage.

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