An investigation into adiabatic circuits

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Abstract—In this paper we discuss some of the results obtained when we conducted an investigation into adiabatic circuits. We provide theoretical proof of power savings in adiabatic circuits when compared to standard static CMOS circuits and relate the power savings as a function of the charging/discharging time. We provide experimental results to support our claim. In addition to this, we also provide results of our study into basic gates such as Nand, Nor, Xnor and more complicated circuits like a 4 and 8-bit adder.

I. INTRODUCTION

As the demand for portable systems like laptops and cell phones increase there is also a simultaneous need for making them consume less power. Conventional methods such as voltage scaling are slowly reaching their limits and hence it is becoming more and more difficult to meet these exacting power requirements especially as system complexities increase. Given this, the need to adopt unconventional yet logical means to lower power consumption have become paramount. Adiabatic circuits are one such approach. In this approach, we extend some of the concepts of thermodynamics to electrical circuits. In thermodynamics, it is possible to transfer energy between two heat sinks, losing very small amounts of energy, if the transfer of energy is purposefully slowed. Similarly if the transfer of charge in electrical circuits were to occur much slower when compared to the natural RC, we dissipate very small amounts of power. The amount of power dissipated directly depend on how slowly the charge transfer occurs. This paper is divided into five sections. The first section is an introduction The second section deals with some adiabatic circuit styles. The third section gives a theoretical proof of power savings using the adiabatic approach and tries to relate the magnitude of the power savings to the charging/discharging times. The fourth section provides some experimantal results on basic gates while the fifth deals with experimental results of more complicated arithmetic circuits. The sixth section discusses some of the problems associated with practical implementation of adiabatic circuits, outlines future work and finally concludes. We used a CMOS 0.5 micron technology for all our experiments.

II. ADIABATIC CIRCUIT DESIGN STYLES

Adiabatic circuit styles can be divided into two broad categories, semi-adiabatic circuits and completely adiabatic circuits. Semi-adiabatic circuits have some unadiabatic dissipation at every stage in the adiabatic pipeline, while completely adiabatic do not have any unadiabatic dissipation at every stage in the pipeline. The 2N2N-2P circuit style[1] is a good example of the former while split level charge recovary logic(SCRL)[2] is a good example of the latter. We chose the latter for all our experiments as we were attracted by the fact that they do not have any unadiabatic dissipation at every stage. It should be noted that even though they have no unadiabatic dissipation, they have many disadvantages when compared to the 2N2N-2P style as they require more power-clocks and more area because of the presence of reversible pipelines. For more information on the working of each of these styles the reader is urged to refer to [1],[2] and [3] for a brief summary. In the following sections we assume that the reader has a knowledge of operation of both these circuit styles.

III. THEORETICAL PROOF OF POWER SAVINGS

In this section we attempt to give theoretical proof of power savings with adiabatic charging. Fig(1) shows two waveforms with a charging time, T and T*n where T is the time. The waveform on the left shows a typical waveform observed at any node which is being conventionally charged, while the one on the right shows a typical waveform ob-

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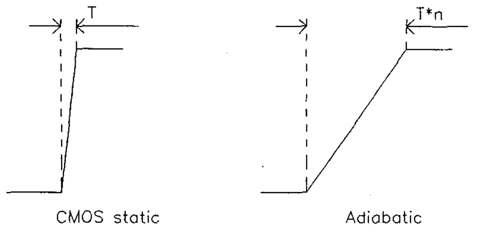

Fig. 1. Conventional and Adiabatic charging schemes

served at the same node when it is adiabatically charged. It can be seen that in the adiabatic case, the charging happens over a longer period of time equal to T*n. If P_s and P_a are the power dissipation and E_s and E_a are the energies consumed for conventional(static) and adiabatic charging respectively, then for the conventinal charging case found in static circuits

$$E_s = I^2 R_s T \qquad (1)$$

where I_s and R_s are the average current and resistance associated with the charging path. We know that

$$I_s = C_s \frac{\Delta V}{T} \qquad (2)$$

Power dissipated P_s in the conventional case is given by,

$$\begin{aligned} P_s &= \frac{E_s}{T} \\ &= [C_s \frac{\Delta V}{T}] R_s \end{aligned}$$

$$P_s = \frac{C_s^2 (\Delta V)^2 R_s}{T} \qquad (3)$$

Similarly Power dissipated in the adiabatic case is given by,

$$P_a = \frac{C_a^2 (\Delta V)^2 R_a}{n^2 T} \qquad (4)$$

It should be noted that I_a in the case of adiabatic charging is dependent on n and is given by the equation,

$$I_s = C_s \frac{\Delta V}{nT} \qquad (5)$$

Unfortunately equations [3] and [4] cannot be directly compared since the capacitance and resistance are different in each case. This is because the electrical circuits are different for both cases. We now consider a test case, evaluate the resistance, capacitance in each case and substitute these values in [3] and [4] to better appreciate these equations. Our test case consists of an inverter which is loaded by one or more similar inverters. For conventional charging, our test inveters were static and for adiabatic charging we had an SCRL inverter pipeline (The pipeline was 2 phase). We urge the reader to refer to [3] for an exhaustive description of the setup. The capacitance profile for our test setup in both cases are shown in figures 3 and 4.

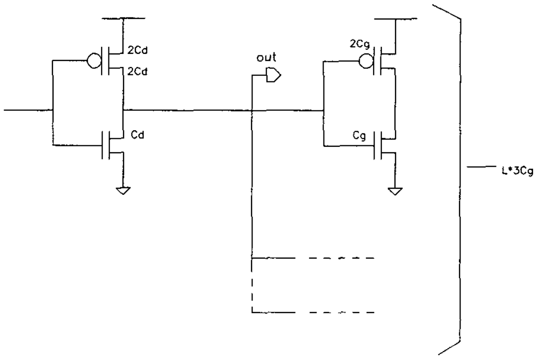

Fig. 2. Capacitance profile for the static case

Referring to fig 2, which is the static CMOS scenario, the total capacitance that has to be charged at the output node is the sum of the drain capacitances and the gate capacitances of the load where L is the fanout. Now C_s is given by,

$$\begin{aligned} C_s &= 2C_d + 2C_d + C_d + L * 3C_g \\ &= 5C_d + L * 3C_g \end{aligned}$$

Refering to fig 3, which is the adiabatic scenario in SCRL circuit style, the total capacitance to be charged increases because of the presence of the reverse pipeline and the transmission gates. Note that the drain capacitance for the pass gates are much larger and commensurate with the size of the transistors which make up the transmission gate. C_a is given by,

$$\begin{aligned} C_a &= 29C_d + L * 3C_g + 12C_d + 3C_g \\ &= 41C_d + 3C_g[L + 1] \end{aligned}$$

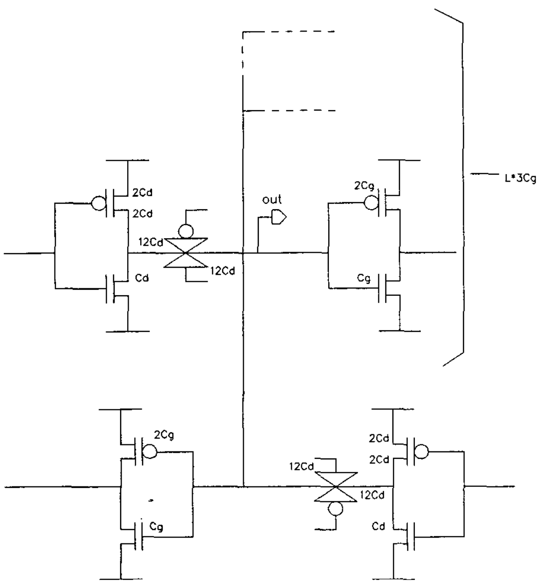

Fig. 3. Capacitance profile for the static case

The resistance of the charging path also increases in the adiabatic case and R_a is about 1.125 times R_s, where R_s is the resistance of the charging path in the static CMOS case. This increase in resistance is due to the presence of the transmission gate. Using the equations for C_s, and C_a, making the assumption that C_d is $0.7C_g$ and also keeping in mind that Δ V for static is V while Δ V for adiabatic case is V/2 and with both n and L equal to 4, we have the ratio P_s/P_a to be equal to 3.5. Our experimental results yielded the ratio to be 2.2, The difference is due to the fact that we did not account for dissipation due to leekage in our equations.

The ratio increases dramatically for higher values of n and is given by the equation

$$\frac{P_s}{P_a} = 0.2234n^2 \tag{6}$$

According to this equation, the ratio takes values of 89.6 and 22.4 for values of n equal to 20 and 10 respectively.

IV. POWER SAVINGS FOR BASIC GATES

We performed similar experiments for other basic gates like Nand, Nor and Xor. Fig 4 shows the ratio P_s/P_a for different gates for n somewhere between 3 to 4. 0.5 micron CMOS technology was used for all our experiments. We urge the reader to refer [3] for a more detailed analysis.

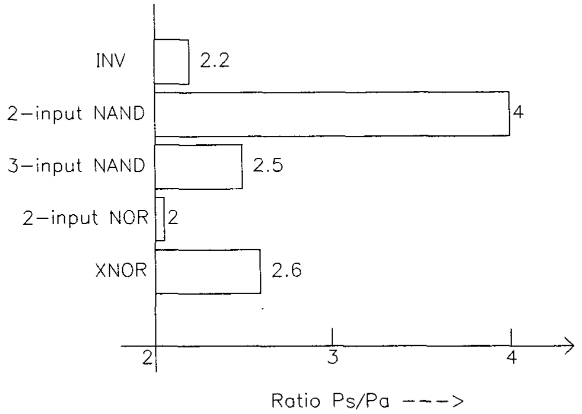

Fig. 4. Ratio P_s/P_a for basic gates

V. POWER SAVINGS FOR ARITHMETIC CIRCUITS

We performed similar experiments for more complicated arithmetic circuits like a 4-bit adder and 8-bit adder. The main aim in doing such experiments was to see whether the good power savings translate to these more complicated circuits. A simple ripple carry scheme was used for the 4 bit version while a carry-select scheme was used for the 8 bit version [3]. The bit slice adder used for both 4 and 8 bit adder is shown in fig(5). Fig(6) shows the transistor implementation of the same in adiabatic SCRL circuit style. Fig(7) shows a diagram of the carry-select scheme which was used to implement the 8-bit adder. Fig(8) shows the ratio P_s/P_a for both the 4-bit and 8-bit adders.

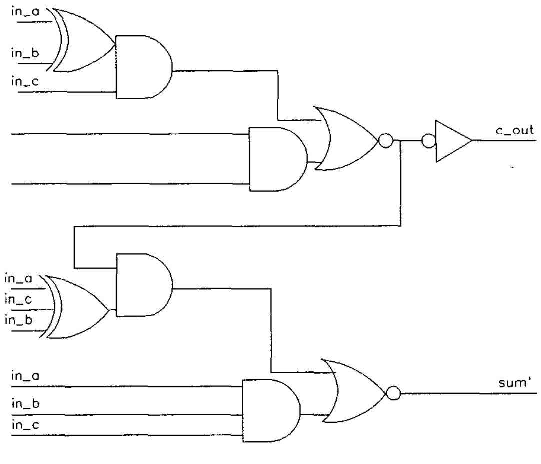

Fig. 5. Adder bit slice

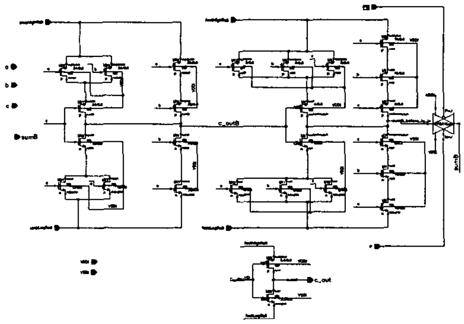

Fig. 6. Transistor schematic of adder bit slice

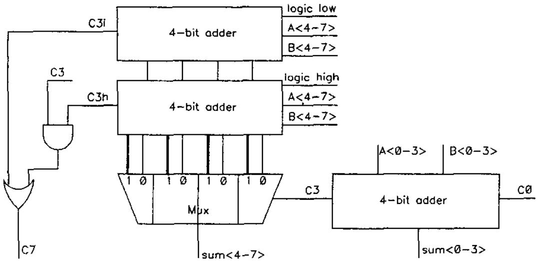

Fig. 7. Carry-select scheme

VI. Problems, future work and conclusions

A. Problems with practical implementation of adiabatic circuits

The power savings that we have in adiabatic circuits come at a cost. We need specially designed charge recycling power-clock supplies which have some dissipation associated with them. Some adiabatic circuit styles such as SCRL require upto 8 different power-clock supplies and their complements and their generation involves complicated circuitry which will have some un-adiabatic dissipation of power. As we have already seen in the previous sections we have good power savings only for large values of n. In other words, if we need to operate a circuit at a frequency f, then we need to make them operate correctly at a frequency f*n and then reduce the frequency to f. This means that adiabatic circuits can only operate at significantly lower frequencies if we want good power savings. This would imply that adiabatic circuits are suitable only for low frequency applications. Another important point to note is that adiabatic circuits occupy rougly twice the area when compared to their static CMOS counterparts because of the need for reversible pipelines and this translates into larger chips.

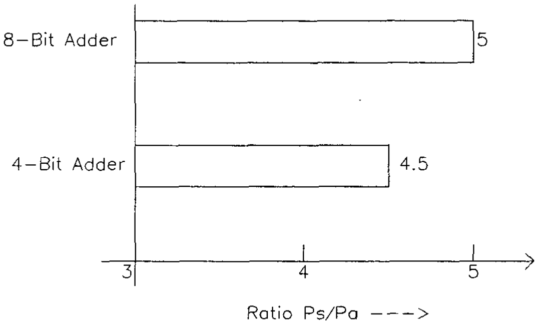

Fig. 8. Ratio P_s/P_a for Adder

B. Future work

Charge recycling power supplies are the key to successful practical implementation of adiabatic circuits. This is an area that needs research. [4] and [5] are good starting points for such an investigation. In addition to this, better circuit styles that use a lower number of power-clock supplies also have to be invented.

B. Conclusions

In this work we have conducted a preliminary investigation of adiabatic circuits. We theoretically show that we can indeed have good power savings with adiabatic circuits. We also verified our theoretical results with experiments on basic gates and more complicated arithmetic circuits.

References

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