Accurate Macro-modeling for Leakage Current for I_{DDQ} Test

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Extended abstract: Due to the continued scaling of technology and supply and threshold voltage, leakage power has become more and more significant in the power supply dissipation of nanoscale CMOS circuits. Therefore, testing deep sub-micron (DSM) chips with millions of transistors is a difficult challenge.

The aggressive scaling increases variation in fault-free quiescent supply current(I_{DDQ}) of the device under test. As fault-free and faulty I_{DDQ} distributions overlap, it is not clear to distinguish between leakage and defect current. In order to solve the problem, this paper proposes a new micro-modeling for leakage. Although some papers have been published on this modeling for sub-threshold leakage and gate tunneling leakage, they neglected the interactions between the two leakages. They also didn't consider fanin/fanout effect in the leakage current [1][2]. Therefore, better understanding and more accurate model of leakage currents are essential for successful chip testing in sub-90nm CMOS technologies.

This paper proposes a new precise macro-modeling of leakage current in BSIM4 65nm technology considering sub-threshold leakage, gate tunneling leakage, stack effect, and fanin/fanout effect. Using the accurate macro-model, a heuristic algorithm is developed using C language to estimate the leakage power and generate input test pattern for minimum leakage. The algorithm applies to ISCAS85 benchmark circuits, and the results are compared to the results of HSPICE. The experimental result shows that the leakage power estimation using our macro-model is within 5% difference when comparing to HSPICE.

Gate Leakage Current: Gate leakage is a current flowing (tunneling) into the gate of the transistor. The tunneling current decreases exponentially as gate oxide increase as shown in the following equation.

$$I_{gate_tunneling} = (A \cdot C) \cdot (W \cdot L) e^{-B \cdot \frac{T_{ox}}{V_{gs}} \cdot \alpha}) \tag{1}$$

where $A = q_3 / 8\pi h\phi_b$, $B = 8\pi\sqrt{2m_{ox}}\phi_b^{3/2} / 3hq$, $C = (V_{gs} / T_{ox})^2$, *a* is a parameter which is ranged from 1 to 0.1 depending on the voltage drop across the oxide, *H* is the Planck's constant, and φ_b is the barrier height for electronics/holes in the conduction/valance band.

The gate tunneling leakage has already increased to more than double the sub-threshold leakage current in the nanoscale CMOS technology. The magnitude of the gate tunneling is strongly dependent on the voltages of three terminals of CMOS [6][7].

Sub-threshold Leakage Current: Even though the transistor's gate voltage is lowered to below V_{th}, a small current still flows between the source and drain terminals [3]-[5]. The equation for the sub-threshold leakage current is given by

$$I_{sub} = I_0 e^{\frac{V_{gs}-V_{th}}{\eta kT/q}} (1 - e^{-\frac{V_{ds}}{kT/q}}) \quad (2)$$

where $I_0 = \mu_0 C_{ox} (W/L)(\frac{kT}{q})^2 (1 - e^{1.8})$, *W* and *L* are the transistor channel width and length, μ_0 is the low field mobility, C_{ox} is the gate oxide capacitance, *k* is the Boltzmann constant, *q* is the electronic charge, and *N* is the sub-threshold swing factor.

Stacking Effect and Fanin/Fanout Effect: When there are two or more stacked off-transistors, the sub-threshold leakage is reduced. The reduction depends on the input pattern during standby periods since it determines the number of OFF transistor in the stack.

Depending on the primary input pattern, the sub-threshold leakage current and gate tunneling are affected by adjacent (fanin/fanout) logic circuit. In Figure 1, the primary input is logic '1', the number of fanins of inverter G3 is two, and the number of fanouts of inverter G3 is three. First, current I_{gG3} is a gate tunneling leakage of inverter G3. In this circuit, I_{gG2} and I_{gG4} are gate tunneling leakage current of G2 and G4, respectively. The directions of the three currents are converged into the input of inverter G3. According to KCL law, the I_{gG3} is one third less than the gate tunneling leakage without any fanins. Many fanin circuits reduce the gate tunneling leakage current, on the other hand the sub-threshold leakage (I_{subG3}) will be increased by the effect of the reduced gate tunneling on the gate-source voltage of inverter G3 (because increasing gate tunneling reduces the gate-source voltage). Therefore, the sub-threshold current is influenced by the number of fanin circuits. However, the fanouts of inverter G3 cannot have much effect on the leakage current of the inverter G3. As the number of fanout circuits increases, the output voltage is reduced a little, and then sub-threshold leakage and gate tunneling leakage will be reduced a little.

As a result, the leakage of the inverter G3 is influenced by the leakage of the other gates. Therefore, it is necessary to consider propagation of the fanin/fanout effect for accurate leakage estimation in nanoscale CMOS technology. However, the propagation of leakage current path beyond one level is negligible.

Minimum Leakage Test Pattern Generation: Based on the aforementioned fanin/fanout effect in leakage current, the macro-model for each cell(inverter, nand, and nor gate) is generated using SPICE simulator for different number of fanin/fanout, size of the cell, and input pattern under the fixed Vdd, Vth, Tox, and temperature. In order to prove the accuracy of the macro-model for cells, a heuristic methodology is implemented to generate the test pattern that provides the minimum leakage. The test pattern is used to minimize the leakage current in I_{DDQ} testing.

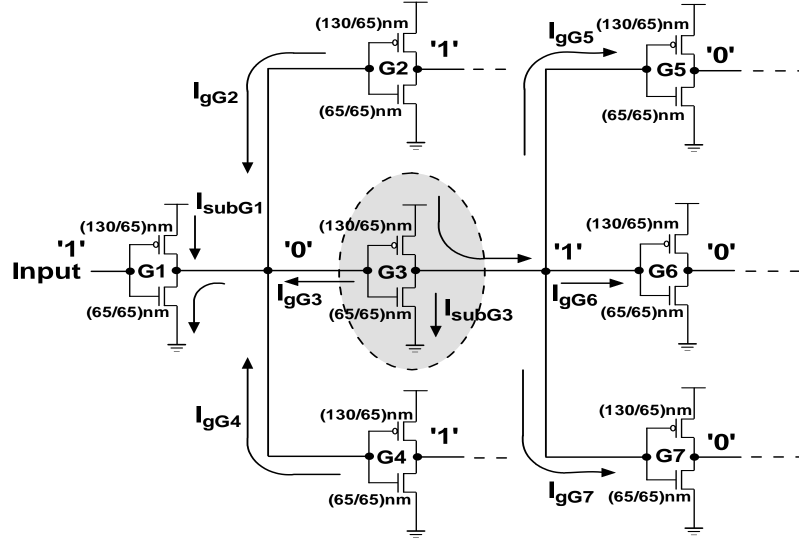

Figure 1. fanin/fanout effect for G3 gate

First, before finding the optimal input vector to reduce the leakage power dissipation, the functional dependencies between the cells should be searched, and dominated cells and conflicting cells for each cell should be listed in order of the cost function given by

$$
\begin{aligned}
&Cost_of_cells(G_i) = \sum_i (MLK_of_conflicting_cells(G_i)) \\
&-\sum_i (MLK_of_dominated_cells(G_i)) - MLK(G_i)
\end{aligned}
\tag{3}
$$

where *MLK* is the mean leakage of the cell that is dependent on input vector and fanin/fanout effect.

Once the list is determined, one cell with the least cost function will be selected. According to the functional constraint, the primary input can be determined to have the least leakage current. After finding the proper input vectors, the cell is removed from the list, and at the same time dominated cells and conflicting cells of the cell are removed from the list. The procedure is repeated until there is no cell in the list or there are only cells that are not defined. If the undefined cells are found, proper vectors have to be assigned considering the condition for low leakage current because they have no dominated cell and no conflicting cells.

Experimental Results: The proposed minimum leakage test pattern generator for nanoscale circuits

(65nm) has been implemented in C language, and run on 500 MHz UltraSPARC-IIe with 500Mbyte memory. The algorithm is tested and compared with HSPICE result using ISCAS85 benchmark circuits that are designed in 65nm technology. The leakage current is measured in HSPICE using the same test vector generated by the proposed methodology. In addition, the proposed methodology using the fanin/fanout effect is compared against the same methodology without considering the fanin/fanout effect. Table I shows the summary of the results of the proposed method and other simulations.

Table1. Leakage estimation results for benchmark circuits

Circuit	# of Gates	Estimated Leakage Current (μA) (Minimum value)		Hspice Minimum Leakae (μA)	Error Rate (%)	CPU Run Time	
		without fanin/fanout effect	with fanin/fanout effect			this work (ms)	Hspice (s)
C432	121	1.75	1.49	1.53	-2.7	0.89	9.45
C499	517	7.48	6.78	7.00	-3.2	5.60	40.34
C880	325	6.67	5.34	5.40	-1.2	3.50	28.88
C1355	478	10.54	7.43	7.21	3.9	5.87	40.41
C1908	750	9.53	6.84	6.57	4.0	6.65	35.94
C2670	890	17.43	11.14	10.75	3.5	9.88	64.83

In this paper, to distinguish leakage current from defect current, an accurate macro-modeling for leakage current is proposed. The proposed methodology focuses on the fanin/fanout effect based on the previous simple modeling. The simulation results show that the modeling without considering the fanin/fanout effect does not estimate accurate leakage current nor generate the best minimum leakage pattern. Finally, the paper proposes a heuristic algorithm for generating the minimum leakage test pattern using the proposed macro-cell model. It is developed and experimented by ISCAS85 benchmark circuits. The experiment shows that the proposed method has high accuracy (within 5 %) and efficiency compared to HSPICE results.

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