Analysis and Simulation of Jitter for High Speed Channels in VLSI Systems

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Extended Abstract: This paper presents a novel modeling analysis and simulation of jitter for high speed (several gigabit per second) IO channels in VLSI systems. Jitter components are analyzed and modeled individually.

As current serial data systems reach rates of several gigabits per second, timing jitter is becoming a significant source of data errors. Timing jitter (henceforth referred to as jitter) is defined as the deviation of a signal transition time from the ideal transition time. A correct model and the analysis of jitter are essential for testing high speed serial data channels.

Many works have been reported on jitter measurement techniques [1][2]. It is relatively simple to measure each jitter component separately, but it is challenging to measure and analyze multiple jitter components if they are either simultaneously injected or already present in a signal over a serial channel. In this paper, a new jitter injection methodology is proposed and the relationship among jitter components is analyzed. Simulation results are used to demonstrate the effectiveness of the proposed method.

Jitter Classification: Total Jitter (TJ) consists of two components: Deterministic Jitter (DJ) and Random Jitter (RJ). On the assumption that each jitter component is independent, the distribution of TJ is given by the convolution of the distributions of DJ and RJ [3][4].

RJ comes from various device noise sources, such as thermal and flicker noise. By the central limit theorem, the distribution of a large number of uncorrelated noise sources approaches a Gaussian distribution and is given by

$$J_{RJ}(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-(\frac{x^2}{2\sigma^2})} \tag{1}$$

where σ is the standard deviation of the jitter distribution or the RMS value, and J_{RJ} is the probability that the edge will occur at time x, where x is the deviation from the mean value of the transition time.

PJ is typically caused by unwanted modulation, such as electromagnetic interference, and is

uncorrelated to any data pattern. PJ is modeled as a sum of cosine functions given by

$$PJ_{total}(t) = \sum_{i=0}^{N} A_i \cos(\omega_i t + \theta_i) \quad (2)$$

where $PJ_{Total}(t)$ denotes the total periodic jitter, N is the number of cosine components (tones), A_i is the amplitude in units of time, ω_i is the modulation frequency, t is the time, and θ_i is the initial phase.

DCD results in HIGH bits (logic 1) having a different width than LOW bits (logic 0). One of the sources of DCD is the difference in propagation delay between LOW to HIGH and HIGH to LOW transitions. Fig. 1 shows the proposed conceptional model of DCD to change the duty cycle in a signal.

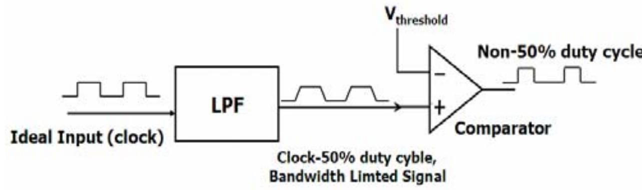


Figure 1. Block Diagram of DCD Model.

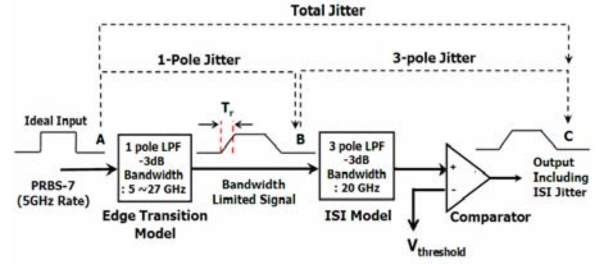


Figure 2. Block Diagram of ISI Model.

ISI comes from the dispersion of signals due to attenuation and reflection in the transmission media. The proposed ISI model has a Low Pass Filter (LPF) with bandwidth limiting effects and ringing. Fig. 2 shows the block diagram of the proposed ISI model.

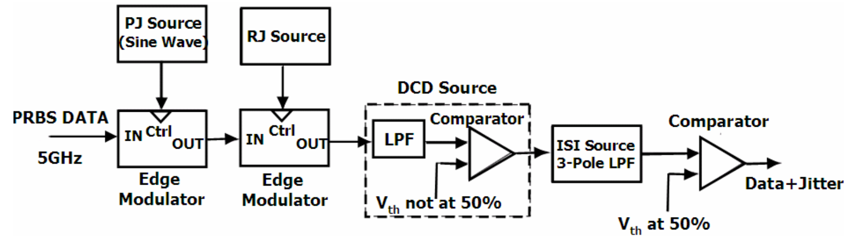


Figure 3. Block Diagram of Jitter Injection.

Jitter Injection: In this paper, an improved jitter injection model is proposed. The new jitter injection model is shown in Fig. 3 in block diagram form. The input is an ideal square wave sequence of pseudo-random data. In the block diagram, the 'Edge Modulator' modulates the edge of the input data by the amount specified by the Control (Ctrl) input. In this paper, four types of jitter components are considered: RJ, PJ, DCD and ISI. Each jitter component is generated and injected into the data signal through its own model.

Simulation Specification: Jitter injection has been simulated using Matlab. The input data is given by an ideal square wave of pseudo-random data, in this case the Pseudo-Random Binary Sequence (PRBS)-7 pattern that has a length of 2^7-1=127 bits. This pattern is repeated 40 times such that a total of

127X40=5080 bits have been simulated. The bit rate of the data pattern generator is 5G bits/sec, and the sampling rate of the simulator is 1,000 samples/bit cell.

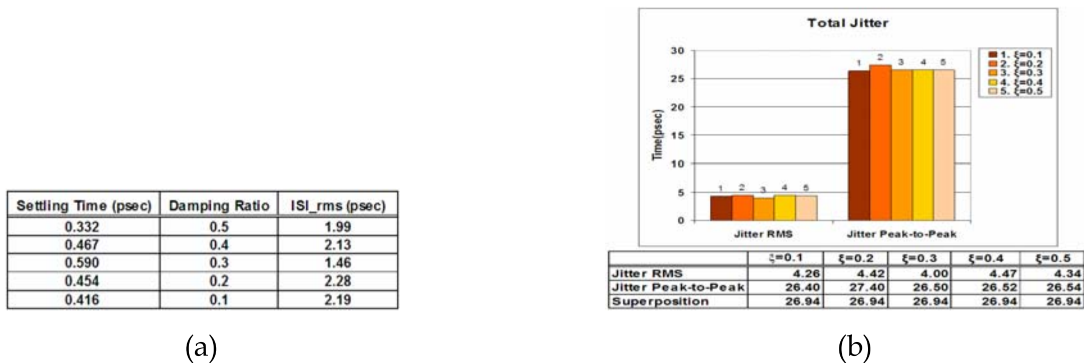
Jitter and Settling Time: As analyzed in [5], the settling time of the step response of the LPF is defined as the system memory length; the length should be greater than 2 Unit Intervals (UIs) to observe the ISI caused by the high/low run length beyond two UIs.

The damping ratio is related to the settling time of the LPF step response and the settling time can change the ISI jitter as predicted in [5]. The effects of the settling time on TJ are shown by using five different damping ratios (therefore different pole locations) of the 2-pole LPF inside the ISI model.

As shown in Fig. 4 (a), the peak-to-peak jitter value injected by the ISI model in all cases is 5 psec, but the damping ratio (that primarily determines the settling time of the LPF) changes from 0.1 to 0.5. The settling time and RMS value of the ISI jitter in the 3-pole ISI change depending on the damping ratio of the 2-pole LPF. The largest settling time for the five cases occurs not at a damping ratio of 0.1, but at 0.3 due to the effect of the 1-pole LPF.

Fig. 4 (b) shows the magnitude of the peak-to-peak and RMS values of TJ for different values of ξ (the damping ratio of the 2-pole LPF). The magnitudes of all other jitter components are the same. Despite the different settling times and pole locations, the peak-to-peak TJ is almost the same (within a 2% difference).

Therefore, for this experiment superposition holds for TJ with different values of settling time, provided the same peak-to-peak value is encountered.



Settling Time (psec)	Damping Ratio	ISI_rms (psec)
0.332	0.5	1.99
0.467	0.4	2.13
0.590	0.3	1.46
0.454	0.2	2.28
0.416	0.1	2.19

	ξ=0.1	ξ=0.2	ξ=0.3	ξ=0.4	ξ=0.5
Jitter RMS	4.26	4.42	4.00	4.47	4.34
Jitter Peak-to-Peak	26.40	27.40	26.50	26.52	26.54
Superposition	26.94	26.94	26.94	26.94	26.94

(a) (b)

Figure 4. Jitter vs. Settling Time of ISI, (a) Effect of the damping ratio, (b) TJ for each damping ratio of LPF.

Relationship among Jitter Components: Simulation is performed by varying DCD against a fixed ISI and PJ (both have 15 psec peak-to-peak value). The results show that a large DCD generates a large difference between the measured DJ and the value found by superposition, as observed in Fig. 5 (a). By varying DCD for a fixed ISI (20 psec peak-to-peak), superposition does not hold for large DCD values, as shown in Fig. 5 (b). Although DCD has an effect on superposition, in practice DCD is significantly smaller than any other component.

Fig. 5 (c) and (d) show that superposition also holds for RJ and DJ. Therefore, DCD and RJ as jitter components seem to have an effect on superposition; however in practice, they have smaller values than

other components, so small DCD and RJ have no significant effect on the overall jitter.

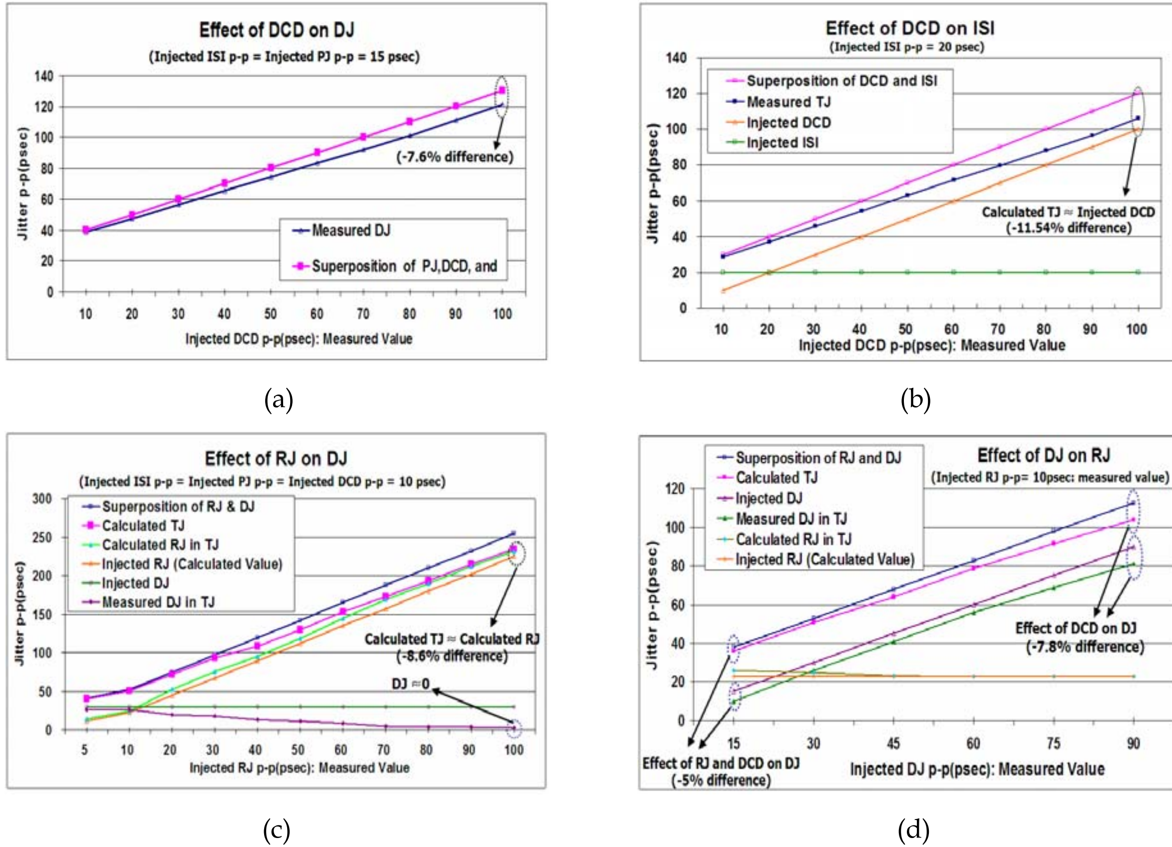


Figure 5: Relationship among Jitter components.

This paper proposes a new method for jitter modeling and analysis for high speed serial data channels in VLSI systems. Jitter is considered by using different models for its components. Jitter components are combined and simulated using Matlab. The effect of the settling time on ISI is evaluated in depth and the superposition of TJ with different settling times is demonstrated. The dependency among jitter components is fully investigated and the validity of superposition for typical jitter values is confirmed.

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