

Jitter Analysis of PWM Scheme in High Speed Serial Link

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Abstract – This paper presents a jitter analysis method for PWM (pulse width modulation) scheme in high-speed serial links. The data rate of PWM with N different pulse widths (PWM- N) scheme is $(\log_2 N) \times (\text{symbol rate})$. However it increases the timing jitter of the transmitted signal. The timing jitter is determined by the pulse widths of PWM symbols and the characteristics of the communication channel. The analysis of the first-order systems and the second-order systems demonstrates that data dependent jitter (DDJ) strongly depends on the -3dB frequency and the damping ratio of the systems. The proposed jitter analysis method makes it possible to determine the pulse width of PWM symbols with the known characteristics of the channel.

Keywords – jitter, high-speed serial link, pulse width modulation.

I. INTRODUCTION

Along with the increasing processing speed of digital systems, the demands for the high speed data communication between systems are also increased. However, the serial interface between different digital systems/blocks, so called digital communication channels, are bandwidth-limited, and the bandwidth-limited channel injects the timing jitter. Timing jitter is composed of random jitter (RJ) and deterministic jitter (DJ)[1][3]. Depending on the noise sources, DJ is classified into several categories such as data dependent jitter (DDJ), periodic jitter (PJ) and bounded and uncorrelated jitter (BUJ). DDJ is a form of jitter caused by the characteristics of the channel environment and the previous transmitted data. Pulse width modulation (PWM) is one form of modulation schemes, which is mostly used in high-speed memory systems[6]. The major advantage of PWM scheme is that it ensures one rising edge during each clock cycle, and the clock signal is embedded in the PWM-encoded signal. Therefore, in receiver end, it is easier to recover the clock from the PWM signal than the traditional non-return to zero (NRZ) data. The clock/data recovery (CDR) circuits can be replaced by a conventional phase-locked loop (PLL), which simplifies the design of the transceiver. In this paper, jitter analysis in high-speed serial links based on

PWM modulation scheme is presented along with simulation results to validate the theoretical estimation.

II. JITTER ANALYSIS

A. PWM and NRZ

For the traditional NRZ data shown in Fig 1(a), if the data width is assumed to be $1UI$ (unit interval), the data rate is $\frac{1}{UI} bps$ and the clock frequency is $\frac{1}{UI} Hz$. PWM-4 scheme shown in Fig 1(b) can double the data rate of the NRZ signal. However the pulse-width of each PWM symbol significantly affects DDJ. The pulse width of every PWM symbol can be represented as:

$$\text{Pulsewidth} = t_b + M \times t_d, M = 1, 2, 3, \dots, 2^N, \quad (1)$$

where N is the number of bits represented by every symbol, t_b is the basic pulse width and t_d is unit pulse width as shown in Fig. 1(b). t_b and t_d are given by $t_b = i \times \delta$ and $t_d = j \times \delta$ respectively, where i and j are integers and δ is the minimum phase shift (the delay of the inverter) that the specific semiconductor technology can accomplish. The entire communication channel can be divided into several individual blocks, and each block can be approximated with a first-order or a second-order system. Therefore, the jitter analysis based on the first-order/second-order system provides a good prediction of the jitter characteristics for the transmitted signals.

B. First-Order Response

Based on the close-form solution from [2], the threshold crossing time of the received NRZ data in the first-order system is given by:

$$t_c = \tau \cdot \ln \left[\frac{-a_0 + \sum_{n=-\infty}^{-1} a_n [\alpha^{-(n+1)} - \alpha^{-n}]}{v_{th} - a_0} \right], \quad (2)$$

where v_{th} is the voltage threshold of the receiver end and a_n is the transmitted binary value. $\alpha = e^{-T/\tau}$ represents the ratio

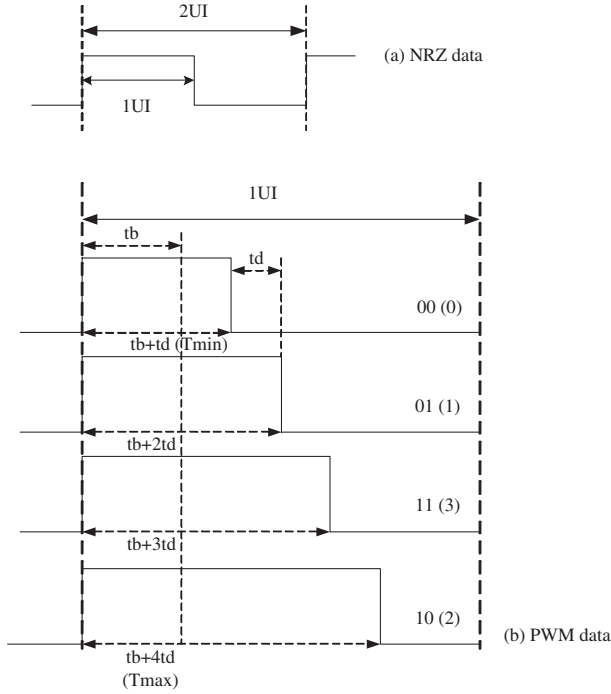


Fig. 1. (a) NRZ data signal (b) PWM-4 signal

between the symbol rate of the system and the bandwidth of the first-order system. For NRZ data, $T = 1UI$ and $\tau = \frac{1}{2\pi f}$, where f is the bandwidth of this low-pass system. Therefore, the timing jitter comes from the difference of the fastest edge and the slowest edge. In the clock/data recovery circuits, the rising edge is compared with the rising edge of the local clock to recover the clock of the transmitted signal. Therefore, the timing jitter of the rising edge needs to be carefully considered. The slowest rising edge has the data pattern: ...00000001 (pattern 1: $a_0 = 1$) and the fastest rising edge has the data pattern:1111101 (pattern 2: $a_0 = 1$). Therefore,

$$t_c(\text{pattern1}) = \tau \ln 2, \quad (3)$$

$$t_c(\text{pattern2}) = \tau \ln 2(1 - \alpha + \alpha^n), \quad (4)$$

$$DDJ_1 = \Delta t_c = t_c(\text{pattern1}) - t_c(\text{pattern2}), \quad (5)$$

$$= \lim_{n \rightarrow \infty} \tau \ln \frac{1}{1 - \alpha + \alpha^n} = \tau \ln \frac{1}{1 - \alpha}. \quad (6)$$

For PWM symbols, if the channel is approximated with a first-order system, the received pulse responses are obtained as:

$$g(t) = \begin{cases} 0, & t < 0 \\ 1 - e^{-\frac{t}{\tau}}, & 0 < t < Tw \\ e^{-\frac{(t-Tw)}{\tau}}(1 - e^{-\frac{Tw}{\tau}}), & Tw < t \end{cases}$$

where Tw is the pulse width of the symbol. If only two previous symbols are considered to affect the rising edge of the current symbol, the voltage threshold can be estimated as:

$$v_{th} = 1 - e^{-\frac{t_c}{\tau}} + e^{-\frac{(t_c+T-Tw_1)}{\tau}}(1 - e^{-\frac{Tw_1}{\tau}})$$

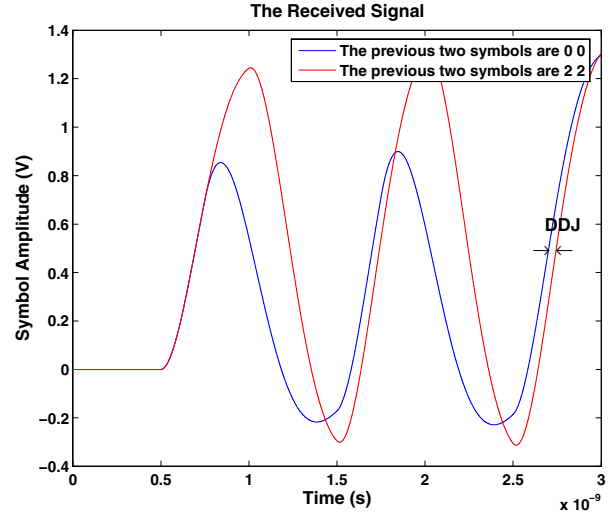


Fig. 2. The DDJ of PWM scheme

$$+ e^{-\frac{(t_c+2T-Tw_2)}{\tau}}(1 - e^{-\frac{Tw_2}{\tau}}), \quad (7)$$

where T is the symbol period, Tw_1 and Tw_2 are the pulse widths of the two previous symbols, and t_c is the threshold crossing time. From equation (7), t_c is obtained by:

$$t_c = \tau \ln \frac{1 + \alpha + \alpha^2 - \alpha^{1-w_1} - \alpha^{2-w_2}}{1 - v_{th}}, \quad (8)$$

where $\alpha = e^{-\frac{T}{\tau}}$, $w_1 = \frac{Tw_1}{T}$ and $w_2 = \frac{Tw_2}{T}$. Equation (8) implies that t_c decreases monotonously as w_1 and w_2 increase. Therefore, the two previous symbols with smallest pulse widths cause the slowest rising edge of the current symbol while two previous symbols with largest pulse widths cause the fastest rising edge of the current symbol. DDJ comes from the threshold crossing time of the slowest rising edge and that of the fastest rising edge as shown in Fig 2. The expression of DDJ in the first-order system is obtained as following:

$$\begin{aligned} DDJ_2 &= \tau \ln \frac{1 + \alpha + \alpha^2 - \alpha^{1-w_{min}} - \alpha^{2-w_{min}}}{1 + \alpha + \alpha^2 - \alpha^{1-w_{min}-\Delta w} - \alpha^{2-w_{min}-\Delta w}}, \\ &= \tau \ln \left(1 + \frac{\alpha^{-\Delta w} - 1}{\frac{1 + \alpha + \alpha^2}{\alpha^{1-w_{min} + \alpha^{2-w_{min}}} - \alpha^{-\Delta w}}} \right), \end{aligned} \quad (9)$$

where $\Delta w = \frac{T_{max}-T_{min}}{T}$, $w_{min} = \frac{T_{min}}{T}$, $T_{max} = t_b + 2^N \times t_d$ and $T_{min} = t_b + t_d$. Equation(9) implies that DDJ increases monotonously as Δw and w_{min} increase.

C. Second-Order Response

The received pulse response $g(t)$ for the second-order systems are obtained as follows[7]:

$$g(t) = \begin{cases} 0, & t < 0 \\ 1 - \frac{1}{\beta} e^{-\zeta \omega_n t} \sin(\omega_n \beta t + \theta), & 0 < t < Tw \\ g(Tw) \left(\frac{\omega_n}{\beta} e^{-\zeta \omega_n t} \sin \omega_n \beta t \right), & Tw < t \end{cases}$$

where $\beta = \sqrt{1 - \zeta^2}$, $\theta = \cos^{-1}\zeta$, ζ is the damping ratio and w_n is the natural frequency of the second-order systems. Qualitatively, if $\zeta \geq 1$, systems are overdamped or critically damped. In those cases, the second-order system can be considered as the catenation of the two first-order systems. Underdamped systems ($\zeta < 1$) have complex poles that result in ringing. The ringing strengthens the impacts of the previous symbols on t_c of the current symbol. The symbol patterns demonstrated for the first-order system to generate the slowest rising edge and the fastest rising edge of the current symbol can not be used for the second-order system. The symbol patterns causing the slowest t_c and the fastest t_c depend on the damping ratio of the systems. The first-order Taylor series is usually used to approximate the step response of the second-order system[2]:

$$g(t - nT) = g(t_0 - nT) + (t - t_0)g'(t_0 - nT) \quad (10)$$

The superscript denotes the derivative. Therefore, the threshold crossing time, t_c , is

$$t_c = t_0 + \frac{v_{th} - g(t_0) - g(t_0 + T) - g(t_0 + 2T)}{g'(t_0) + g'(t_0 + T) + g'(t_0 + 2T)}. \quad (11)$$

Since the symbol patterns causing the slowest rising edge and the fastest rising edge are unknown, there is no closed-form solution for DDJ estimation in the second-order systems. Experimental results from the next section illustrate DDJ dependence on the damping ratio and natural frequency.

III. EXPERIMENTAL RESULTS

PWM-4 scheme (Fig. 1(b)) is used as an instance to illustrate the jitter analysis of PWM scheme. One PWM-4 symbol denotes 2-bit data. Table I shows the different combination of t_b and t_d (generated by different clock signal) and their corresponding DDJs in the first-order systems. The measured DDJ is close to the estimated value. The double data-rate NRZ signal (the unit interval is 500 ps and clock frequency is 1GHz) can achieve the same data rate as PWM-4 scheme. If double data-rate NRZ signal passes the same first-order low pass filter (with 1GHz $-3dB$ frequency), the estimated DDJ is around 7ps, which is close to DDJ of PWM scheme 7. For PWM symbols, the DDJ of the rising edges affects the jitter of the recovered clock at the receiver end. The accuracy of the pulse width demodulation depends on the ratio of the timing jitter of the recovered clock over the unit pulse width. So DDJ_{ratio} is a good figure of merit to evaluate the choices of t_b and t_d . It is observed in Table I that if t_b and t_d are smaller, DDJ is smaller. However if the pulse width of the transmitted signal is smaller, the corresponding received signal has more attenuation. And t_d and t_b can not be too small since they are limited by hardware. For the second-order systems, DDJ strongly depends on the damping ratio. Fig 3 shows the simulation results of DDJ versus the damping ratio for different natural frequencies. DDJ increases with the decrease of the natural frequency.

For the fixed natural frequency, DDJ has the minimum value when the damping ratio is around 0.7 – 0.9. Table II shows the different combination of t_b and t_d and their corresponding DDJs in the second-order systems. The conclusion for the second-order systems is different from the first-order systems. DDJ increases monotonously as t_b increases, however there is no monotonous relationship between t_d and DDJ. Therefore, basic pulse width t_b equal to 0 is a good option for any system.

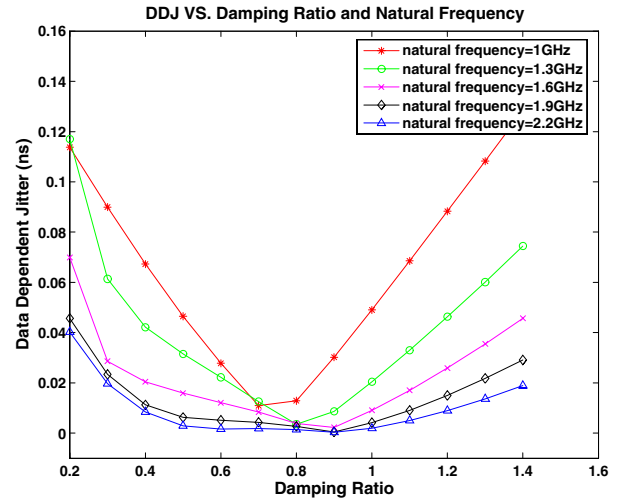


Fig. 3. DDJ of the PWM-4 scheme with respect to the damping ratio and natural frequency for the second-order systems ($t_d = 125ps$ and $t_b = 125ps$)

Since the high speed data communication link is a low pass channel, the pre-emphasis architecture that plays a role of high pass filter is most frequently used at the transmitter end to cancel the low pass characteristic of the communication link[5]. Therefore, the overall frequency response at the receiver side becomes uniform within the desired frequency range. In another words, it increases the bandwidth of the communication channel. It is obvious that the peak-peak DDJ decreases with the increment of the bandwidth as shown in Fig 3. Pre-emphasis architecture implemented by the symbol spaced FIR filter (SSF) can also be utilized to improve the jitter performance of the PWM signal. In real system, the electrical link can be modelled as a transmission line. With the measured or simulated S-parameter, the tap values of the FIR filter can be determined with the Matlab program developed by [4].

IV. CONCLUSIONS

This paper presents an analytical method to estimate DDJ of PWM symbol in the low-pass communication channel. Experimental results show that the estimated DDJs of the first-order systems are close to the measured ones. There is no close-form solution for DDJ of PWM symbols in the undamped second-order systems. From the simulation results, the dependence of

TABLE I
DIFFERENT PWM-4 SCHEMES AND THEIR DDJS ($-3dB$ FREQUENCY IS 1GHZ)

Scheme NO.	Clock	Basic Pulse Width t_b (ps)	Unit Pulse Width t_d (ps)	Measured DDJ_{max} (ps)	DDJ_{ratio} ($\frac{DDJ_{max}}{t_d}$)	Estimated DDJ_{max} (ps)
1	5-phase clock	0.0	200.0	52.25	0.261	52.26
2	6-phase clock	0.0	166.6	20.05	0.120	20.03
3		166.6	166.6	66.15	0.397	66.18
4	7-phase clock	0.0	142.8	10.40	0.073	10.41
5		142.8	142.8	27.05	0.189	27.05
6		285.6	142.8	78.65	0.551	78.63
7	8-phase clock	0.0	125.0	6.40	0.051	6.38
8		125.0	125.0	14.40	0.115	14.41
9		250.0	125.0	33.90	0.271	33.92
10		375.0	125.0	89.85	0.719	89.85

TABLE II

DIFFERENT PWM-4 SCHEMES AND THEIR DDJS (THE NATURAL FREQUENCY OF THE SECOND ORDER SYSTEM IS 2GHZ AND THE DAMPING RATIO IS 0.4)

Scheme NO.	Clock	Basic Pulse Width t_b (ps)	Unit Pulse Width t_d (ps)	DDJ_{max} (ps)	DDJ_{ratio} ($\frac{DDJ_{max}}{t_d}$)
1	5-phase clock	0.0	200.0	34.15	0.171
2	6-phase clock	0.0	166.6	9.40	0.056
3		166.6	166.6	40.00	0.240
4	7-phase clock	0.0	142.8	10.20	0.071
5		142.8	142.8	18.80	0.132
6		285.6	142.8	42.50	0.298
7	8-phase clock	0.0	125.0	9.35	0.075
8		125.0	125.0	9.40	0.075
9		250.0	125.0	25.40	0.203
10		375.0	125.0	41.20	0.330

DDJ on the damping ratio and the natural frequency is illustrated. If the characteristics of the communication channel are known, the pulse widths of PWM symbols can be determined and pre-emphasis architecture can be added to cancel the channel loss and decrease DDJ.

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