

transistor M10, M11, M14 and M15 turn on and *Out* nodes and *Sw* nodes are charged up to V_{DD} while both NMOS transistors M12 and M13 are off.

During evaluation (decision-making) phase ($Clk=V_{DD}$), each *Di* node capacitance is discharged from V_{DD} to ground in a different rate proportional to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between *Di+* and *Di-* nodes. Once either *Di+* or *Di-* node voltage drops below $V_{DD}-|V_{tp}|$, the inverter pairs (M18/M16 and M19/M17) invert each *Di* node signal into the regenerated (amplified) *Di'* node signals. Then the regenerated and different phased *Di'* node voltages are relayed to the output-latch stage by M10–M13. As the regenerated each *Di'* node voltage is rising from 0V to V_{DD} with a different time interval (or a phase difference which increases with the increasing input voltage difference ΔV_{in}), M12 and M13 turn on one after another and the output latch starts regenerating the small voltage difference transmitted from *Di'* nodes into a full-scale digital level: *Out+* node will output logic high (V_{DD}) if *Di+* node voltage is rising faster than *Di-* node voltage and *Out+* will output logic low (0V) otherwise. Once either of *Out* node voltages drops below $V_{DD}-|V_{tp}|$, this positive feedback becomes stronger because either PMOS transistor M8 or M9 will turn on.

Since the dynamic comparator shown in Figure 1 can be divided into three stages, the total offset voltage ($V_{OS, tot}$) can be expressed as

$$V_{OS, tot} = \sqrt{V_{OS, Diff, Input}^2 + \frac{1}{G_1^2} \cdot V_{OS, Inv, Pair}^2 + \frac{1}{G_1^2 \cdot G_2^2} \cdot V_{OS, Output Latch}^2} \quad (1)$$

where $V_{OS, Diff, Input}$, $V_{OS, Inv, Pairs}$, and $V_{OS, Output Latch}$ are the offset voltages resulting from the mismatched transistor pairs in each stage, respectively. G_1 is the voltage gain between *Di* nodes and *In* nodes and G_2 is the voltage gain between *Di'* nodes and *Di* nodes.

To optimize the comparator in terms of the minimal offset voltage, the offset voltage contributions of each stage have to be verified first. Therefore, all transistors (but the inverter pairs) are designed to have the same aspect ratio of $W/L=1\mu m/0.1\mu m$. In order for the inverter pair to have the proper gain and correct functionality, PMOS transistors of the inverter pair are designed three times bigger than NMOS transistors ($W_p/W_n=1.5\mu m/0.5\mu m$). To simulate 1-sigma offset voltages for each stage, the random mismatch in threshold voltage V_{th} and current factor β ($=\mu C_{ox}W/L$) for each transistor pair are modeled as follows [1],

$$\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{WL}}, \quad \sigma_{\beta} = \frac{A_{\beta}}{\sqrt{WL}} \quad \text{where } W, L \text{ are in } \mu m \quad (2)$$

$A_{V_{th}}$ and A_{β} are process dependent parameters and are assumed to be $4.5mV \cdot \mu m$ and $1\% \cdot \mu m$, respectively in this mismatch analysis. As shown in Figure 2 (in Grey), the input referred offset voltages of each stage of the comparator with respect to the different the input common mode voltages are extracted from 100 times of transient Monte-Carlo simulations ($V_{DD}=1V$,

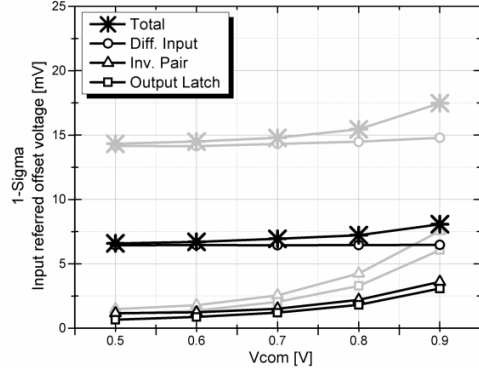


Figure 2 Offset voltage contributions of each stage before (Grey) and after (Black) optimization.

$f_{clk}=3GHz$). As expected, the offset voltage resulting from the mismatched transistor pairs in the regenerative output-latch stage is the smallest since it is reduced by the gain of $G_I \times G_2$ and the offset voltage from the mismatch between the inverter pair, which is reduced by the gain of G_I , is also small comparing to the offset voltage of the differential input stage. The offset voltage of the differential input stage can be approximated as [10]

$$V_{OS, Diff, Input}^2 = \left(\frac{V_{GS2,3} - V_{tn}}{2} \right)^2 \left\{ \left(\frac{\Delta C_{Di}}{C_{Di}} \right)^2 + \left(\frac{\Delta \beta_{2,3}}{\beta_{2,3}} \right)^2 \right\} + \Delta V_{tn2,3}^2 \quad (3)$$

Since the threshold voltage mismatch between transistor M2 and M3 ($V_{m2,3}$) is directly related to the total random offset voltage, it becomes the dominant factor at the same aspect ratio ($W/L=1\mu m/0.1\mu m$). Therefore, to get the minimal offset voltage at the power and area constraints, the size of the input transistor pair (M2 and M3) have to be sized up first. For our design we sized both input transistors to have $W/L=4\mu m/1.2\mu m$. Next the critical transistor pairs are M18/19, M12/13, M10/11 and M6/7 since those pairs also amplify the input voltage difference ΔV_{in} during the evaluation phase.

Using balanced method presented in [2], input referred offset voltages of those transistor pairs can be obtained as follows;

$$V_{OS12,13}^2 = \frac{1}{G_1^2 \cdot G_2^2} \cdot \left[\left(\frac{V_{Di'} - V_{tn}}{2} \right)^2 \left(\frac{\Delta \beta_{12,13}}{\beta_{12,13}} \right)^2 + \Delta V_{tn12,13}^2 \right] \cdot \left\{ 1 + \frac{V_{Di'} - V_{tn}}{2(V_{DD} - V_{Di'} - |V_{tp10}|)} \left(\frac{I_{D10(11)}}{I_1} \right) \right\}^{-2} \quad (4)$$

$$V_{OS10,11}^2 = \frac{1}{G_1^2 \cdot G_2^2} \cdot \left[(V_{DD} - V_{Di'} - |V_{tp}|)^2 \left(\frac{\Delta \beta_{10,11}}{\beta_{10,11}} \right)^2 + \Delta V_{tp10,11}^2 \right] \cdot \left\{ 1 + (V_{DD} - V_{Di'} - |V_{tp}|) \left(\frac{g_{m12(13)}}{I_1 - I''} \right) \right\}^{-2} \quad (5)$$

where I_1 is the drain current of M12 and I'' is the external load capacitor current, which direct is inside the *Out±* node. Equation (4) shows the influence of transistor M10 and M11 (which are used as both reset switches and input transistors for the output-latch stage). Since this comparator have two pairs of the input transistors in the output latch stage, the offset

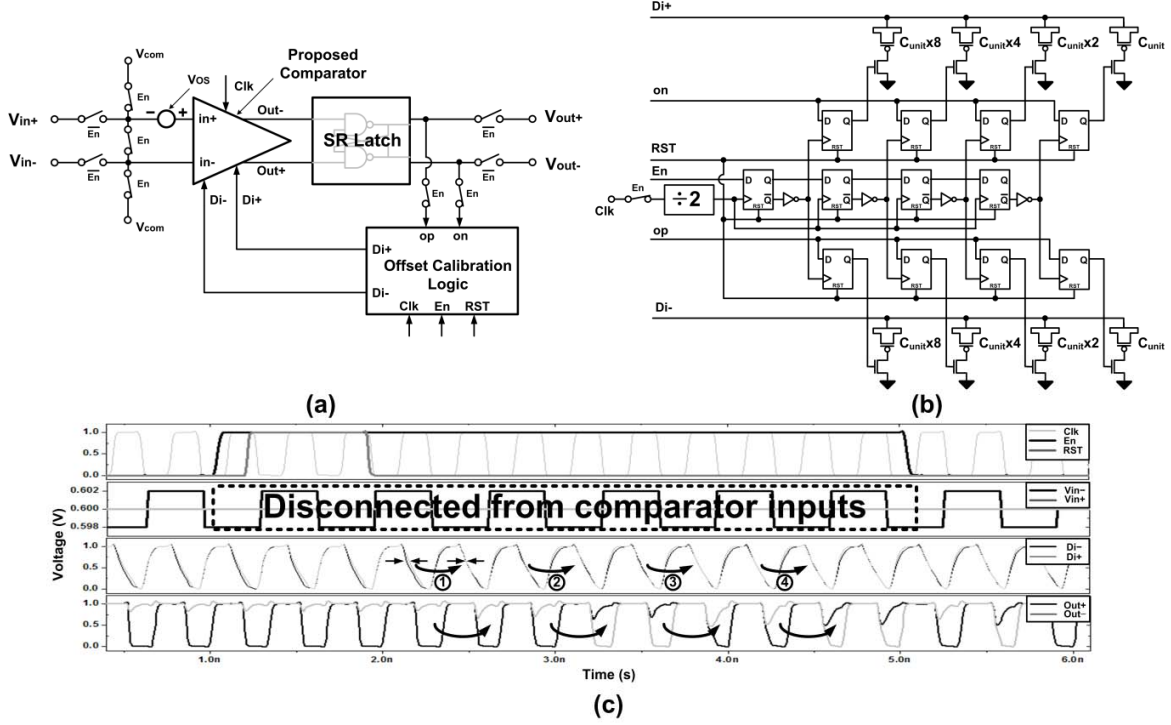


Figure 3 (a) Proposed offset voltage calibration technique using Di node capacitance compensation. (b) Offset voltage calibration logic. (c) Signal waveforms of the proposed offset calibration process with the intentional V_{os} of +20mV and $f_{clk}=3$ GHz.

voltages caused from one pair are compensated by the other input transistor pair. Therefore, the additional term followed by the negative square root term in equation (4) compensates the former offset voltage term caused from transistor mismatch between M12 and M13. As $V_{Di'}$ increases from V_{in} to $V_{DD}-|V_{tp}|$, the input referred offset voltage is further reduced since the influence of the additional denominator term increases. While larger NMOS transistor M12 and M13 are desirable for the low offset and the large drive currents for the fast latching, larger PMOS transistor M10 and M11 are also required for low offset to increase I_{D10}/I_1 ratio. Therefore, there is the optimal ratio between $W_{12(13)}$ and $W_{10(11)}$ at a limited area for the minimum offset voltage.

For mismatch between transistor M6 and M7, $\mu_n C_{ox,6,7}$ mismatch is considered instead of current factor β mismatch to find out the optimal ratio between the width of transistor M6(M7) and M12(M13).

$$V_{OS6,7}^2 = \frac{1}{G_1^2 \cdot G_2^2 \cdot G_3^2} \cdot \frac{W_{6(7)}}{W_{12(13)}} \left[\left(\frac{\Delta \mu_n C_{ox,6,7}}{\mu_n C_{ox,6,7}} \right)^2 \frac{(V_{out\pm} - V_{D13} - V_{tn})^2}{4} + (V_{D13} - V_{D12})^2 + \Delta V_{tn6,7}^2 \right] \quad (6)$$

where G_3 is the voltage gain between Sw nodes and Di' nodes. Equation (6) shows that the offset voltage caused by the mismatch between the transistor M6 and M7 is a function of size between transistor M6(M7) and M12(M13). Although

$V_{OS6,7}$ seems to decrease as $W_{6(7)}/W_{12(13)}$ ratio decreases, the random mismatches of $\Delta \mu_n C_{ox,6,7}$ and $\Delta V_{tn6,7}$ increase as $W_{6(7)}$ decreases. Therefore, there is a particular $W_{6(7)}/W_{12(13)}$ ratio which makes an optimum trade-off between them to have the minimum $V_{OS6,7}$.

In consequence, for the minimal offset voltage, the comparator has to be optimized at a limited area and power first. Based on the offset voltage analysis and Monte-Carlo simulation, the dynamic latched comparator is optimized to have the minimal offset voltage. As a result, as shown in Figure 2 (in Black), 1-sigma offset voltage is reduced from 12.5mV to 6.5mV in 0.6V of the input common mode voltage with only 9% increase of the power dissipation (152 μ W from 136 μ W). To further reduce the offset voltage of the dynamic latched comparator without pre-amplifier, digitally controlled capacitive offset voltage compensation technique is suggested.

III. OFFSET CALIBRATION TECHNIQUES

As explained in equation (3), the offset voltage can be compensated by controlling Di node capacitance, current or $V_{in2,3}$ [5]–[8]. The current calibration technique introduced in [7] exploits additional one pair of NMOS compensation transistors in parallel with the differential input pair and a charge pump. Even though this calibration technique consumes no static power, the calibration process has to be done frequently since the charged voltage in the compensation capacitor (which is connected to the gate of one of NMOS compensation transistor pair) falls down due to

the leakage current. In addition, the calibration speed and accuracy are limited by the size of the charging/discharging current sources of charge pump. Digital calibration technique from [6] uses additional capacitance arrays to calibrate the offset voltage. Although the calibration resolution and the maximum offset coverage range are limited by the minimum unit capacitance and the number of bits of the capacitance arrays, this technique does not require the refresh process and does not consume static power as well. In addition, the increase of the node capacitance at Di node reduces the input referred noise. However, it slows down the speed of the comparator since the increased internal node capacitance increases the discharge time. The degree of speed degradation is more severe when this technique is applied to the internal nodes ($Di\pm$) of the comparator from [7] since those internal node voltages are directly applied to the both input transistor pairs of the second stage. On the other hand, the speed of the comparator [10] is relatively less sensitive to the increase of the Di node capacitance since the Di node voltages in the comparator are buffered by the inverter pair.

Figure 3 shows the proposed offset calibration technique using 4-bit capacitor array, which consists of 4-bit shift register, divided by two-circuit, D flip-flops, and 4-bit capacitor arrays, while the size of an unit capacitance is implemented with PMOS transistors ($W/L=120nm/100nm$). Since the offset calibration logic uses 2 times less clock frequency, the timing requirement for the offset calibration logic is relaxed with an extra clock cycle added after switching on each binary weighted capacitor. Therefore, the comparator can be operated above the clock frequency of 3GHz. Before calibration, as shown in Figure 3 (c), the output of the comparator outputs logic low ($0V$) regardless of the input differential voltage of $\pm 2mV$ due to the intentional input referred offset voltage of 20mV. After calibration, however, the comparator can distinguish the input differential voltage even less than $\pm 2mV$. The required calibration time is only around 4ns at $f_{clk}=3GHz$ and the reset signal (RST) can be simply generated using 3-bit shift register, inverters, switches and an AND gate, which is initiated by the enable signal (En).

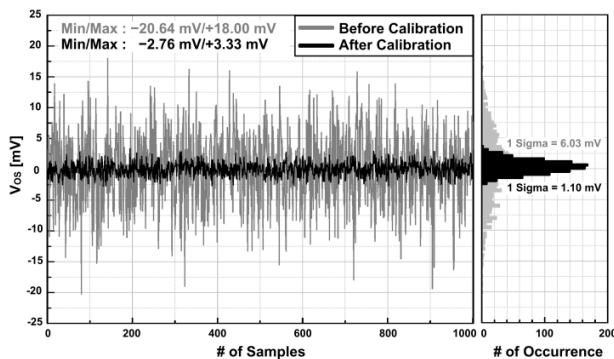


Figure 4 Input referred offset voltage before and after offset calibration obtained from 1000 samples of transient Monte-Carlo simulations

IV. SIMULATION RESULT

The dynamic latched comparator with a capacitive offset voltage calibration circuit was designed and simulated in HSPICE using 90 nm PTM process. To compare the input referred random offset voltages of the comparator before and after offset calibration, 1000 times of transient Monte-Carlo simulations were performed with the random mismatch model from (2), where $A_{vth}=4.5mV\cdot\mu m$ and $A_{\beta}=1\%\cdot\mu m$, and the total input referred offset voltage was measured by applying slowly varying slope signals to the comparator inputs. As shown in Figure 4, 1-sigma offset voltage of 6.03mV was reduced to 1.10mV after the offset calibration with the switching frequency of 3 GHz while it consumes 162 μ W after calibration.

V. CONCLUSION

The offset voltage of the dynamic latched comparator is analyzed. Based on the analysis, the comparator was optimized in terms of the minimal offset voltage. As a result, 1-sigma offset voltage was reduced from 12.5mV to 6.5mV at the cost of 9% increase of the power dissipation (152 μ W from 136 μ W). In addition, with a digitally controlled capacitive offset calibration technique, the offset voltage of the comparator was further reduced from 6.50mV to 1.10mV at 1-sigma at the operating clock frequency of 3 GHz and it consumes 54 μ W/GHz after the calibration.

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