

# *A novel low-power, low-offset, and high-speed CMOS dynamic latched comparator*

*HeungJun Jeon & Yong-Bin Kim*

**Analog Integrated Circuits  
and Signal Processing**  
An International Journal

ISSN 0925-1030

Analog Integr Circ Sig Process  
DOI 10.1007/  
s10470-011-9687-5

## **ANALOG INTEGRATED CIRCUITS AND SIGNAL PROCESSING** An International Journal

Volume 43, Number 1, April 2005

### RFICs

- Thyristor Input-Protection Device Suitable for CMOS RF IC's ..... Jin-Young Choi, Woo Suk Yang, Dongmin Kim and Youngju Kim 5
- A Broadband Double-Conversion RF Tuner ..... Karl Stadius, Arto Malinen, Petri Järviö, Petteri Paatsila and Karl Halonen 15

### Data Converters

- 1.1 V Low-Power  $\Sigma\Delta$  Modulator for 14-bit, 16 KHz A/D Conversion Using a New Low-Voltage Class-AB Op-amp ..... F. Muñoz, A.P. Vegaleal, R.G. Carvajal, A. Torralba, J. Tombs and J. Ramírez-Angulo 31

### Amplifiers and Filters

- Simplified Modeling of a Multipole Amplifier Using All-Pass Network Functions ..... Yihong Dai, Donald T. Comer, David J. Comer and Darren Korh 39
- Design of Square-Root Domain Filters ..... Guo-Jeng Yu, Chun-Yueh Huang, Bin-Da Liu and Jenn-Jiun Chen 49
- Fully Differential CMOS Current Feedback Operational Amplifier ..... Soltman A. Mahmoud and Inas A. Awad 61
- Single DDCC Bi-quads with High Input Impedance and Minimum Number of Passive Elements ..... Muhammed A. Ibrahim, Hakan Kuntman and Oguzhan Cicekoglu 71

(continued on back cover)

 SPRINGER

ISSN: 0925-1030

Available  
online  
  
[www.springerlink.com](http://www.springerlink.com)

 Springer

**Your article is protected by copyright and all rights are held exclusively by Springer Science+Business Media, LLC. This e-offprint is for personal use only and shall not be self-archived in electronic repositories. If you wish to self-archive your work, please use the accepted author's version for posting to your own website or your institution's repository. You may further deposit the accepted author's version on a funder's repository at a funder's request, provided it is not made publicly available until 12 months after publication.**

# A novel low-power, low-offset, and high-speed CMOS dynamic latched comparator

HeungJun Jeon · Yong-Bin Kim

Received: 26 April 2011 / Revised: 5 July 2011 / Accepted: 5 July 2011  
© Springer Science+Business Media, LLC 2011

**Abstract** A novel dynamic latched comparator with offset voltage compensation is presented. The proposed comparator uses one phase clock signal for its operation and can drive a larger capacitive load with complementary version of the regenerative output latch stage. As it provides a larger voltage gain up to 22 V/V to the regenerative latch, the input-referred offset voltage of the latch is reduced and metastability is improved. The proposed comparator is designed using 90 nm PTM technology and 1 V power supply voltage. It demonstrates up to 24.6% less offset voltage and 30.0% less sensitivity of delay to decreasing input voltage difference (17 ps/decade) than the conventional double-tail latched comparator at approximately the same area and power consumption. In addition, with a digitally controlled capacitive offset calibration technique, the offset voltage of the proposed comparator is further reduced from 6.03 to 1.10 mV at 1-sigma at the operating clock frequency of 3 GHz, and it consumes 54  $\mu$ W/GHz after calibration.

**Keywords** Dynamic comparator · Latched comparator · Voltage sense amplifier (SA) · Low-offset low-power high-speed

## 1 Introduction

Due to fast-speed, low-power consumption, high-input impedance and full-swing output, CMOS dynamic latched

comparators are very attractive for many applications such as high-speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers. The conventional dynamic latched comparators use positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) to convert a small input-voltage difference to a full-scale digital level in a short time. However, the accuracy of such comparators is limited by the random offset voltage resulting from the device mismatches such as threshold voltage  $V_{th}$ , current factor  $\beta$  ( $=\mu C_{ox}W/L$ ), and internal-parasitic/external load capacitance mismatches [1–3]. Therefore, the offset voltage is one of the most important design parameters in designing dynamic latched comparator.

Conventionally, as shown in Fig. 1, a pre-amplifier has been used preceding the regenerative latch stage to reduce the latch offset voltage. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also it reduces the kickback noise [4]. However, the pre-amplifier based comparators suffer from both the large static-power consumption for a large bandwidth and the reduced intrinsic gain with a reduction of the drain-to-source resistance  $r_{ds}$  due to the continuous technology scaling [5]. Therefore, for the high-speed low-power CMOS applications, a dynamic comparator without pre-amplifier is highly desirable. This can be realized in terms of a dynamic comparator with digital offset calibration techniques. Recently, dynamic comparators with offset calibration techniques have been proposed [6–8]. However, those approaches show a higher sensitivity of the speed variations and offset voltages to a different input common mode voltage or require a tight timing relationship between clock's true and complementary phases. Furthermore those conventional approaches cannot drive a large load due to its weak drivability.

---

H. Jeon (✉) · Y.-B. Kim  
Department of Electrical and Computer Engineering,  
Northeastern University, Boston, MA, USA  
e-mail: hjeon@ece.neu.edu

Y.-B. Kim  
e-mail: ybk@ece.neu.edu

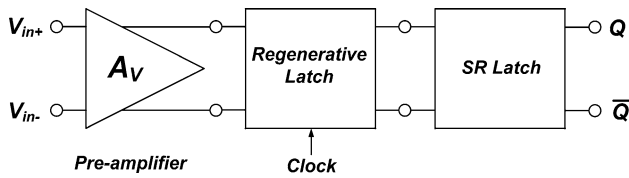


Fig. 1 Typical block diagram of a high-speed voltage comparator

In this article, a novel dynamic latched comparator with offset voltage analysis and compensation is presented. The proposed comparator demonstrates lower offset voltage and it can drive larger load than the conventional dynamic latched comparators at approximately the same area and power consumption. The digitally controlled capacitive offset voltage compensation circuit is designed and simulated using 90 nm PTM technology [9] and 1 V power supply voltage.

The remaining sections of the article are organized as follows. Section 2 provides an overview of the previous works about the dynamic latched comparators in terms of their advantages and drawbacks, and Sect. 3 describes the proposed dynamic latched comparator and its operation principle with the random offset voltage analysis. Section 4 introduces a capacitive offset voltage calibration technique applicable to the proposed comparator, followed by simulation results and comparison with the previous works in Sect. 5. Finally, conclusion is drawn in Sect. 6.

## 2 Previous works

With the advantages such as fast-speed, ideally zero static-power consumption, high input-impedance and full-swing output, the dynamic latched comparator shown in

Fig. 2(a) has been most widely used [10, 11]. However, this comparator has only one tail current transistor M1 which controls the currents flowing through both the differential input pair (M2 and M3) and the latch (M6–M9). Therefore, in order to increase the drive currents of the latch, it is inevitable to size up the transistor M1. If the size of transistor M1 is increased, the drain currents of the both input transistors M2 and M3 will increase during the evaluation phase ( $Clk = V_{DD}$ ). This, in turn, reduces the time duration for which the input transistors operate in the saturation region, because  $Di$  nodes discharge from  $V_{DD}$  to ground in a very short period. Consequently, lower amplification of the input voltage difference will be made between  $Di$  nodes and a small  $V_{th}$  mismatch between transistor M6 and M7 can yield a large input-referred offset voltage. In addition, since it shows large variations of speed and offset voltage with a different input common-mode voltage  $V_{com}$  [11], it is less attractive in applications that need wide input common-mode ranges such as ADCs [12].

To circumvent these drawbacks, the comparator with separated differential input-gain stage and output-latch stage shown in Fig. 2(b) was introduced in [12]. This stage separation makes this comparator be able to operate at a lower supply voltage ( $V_{DD}$ ) and have a more stable offset voltage and speed over wide input common-mode voltage ( $V_{com}$ ) ranges. However, this comparator requires both  $Clk$  and  $Clkb$  signals and the highly accurate timing relationship between those clocks is required for its optimal operation. Since the voltage difference formed between  $Di$  nodes during the evaluation phase ( $Clk = V_{DD}$ ) is time varying, the speed and offset voltage are affected by the clock skew between  $Clk$  and  $Clkb$  signals. If a simple inverter is used to generate  $Clkb$ ,  $Clk$  should be able to drive an additional inverter (at the cost of increased clock

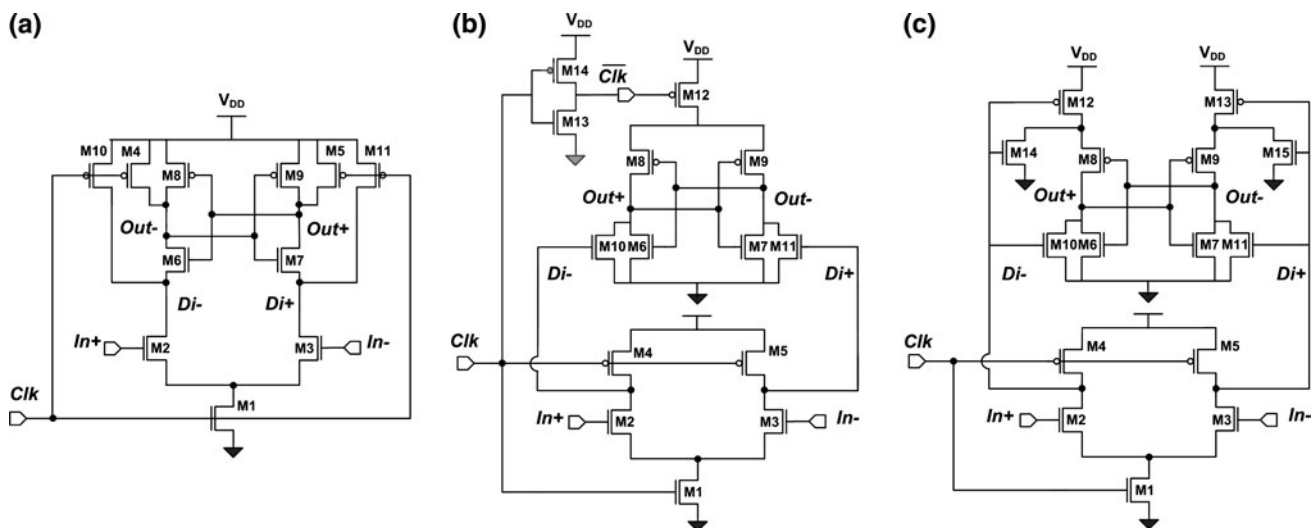


Fig. 2 a Conventional dynamic latched comparator [10, 11], b comparator 1 [12], and c comparator 2 [6]

loading) that drives the largest transistor M12 for a small delay. If  $Clkb$  is lagging the  $Clk$ , it results in increased delay. If  $Clkb$  is leading the  $Clk$ , it results in increased power dissipation due to the short circuit current path M12 to M10/M11 though M8/M9.

The comparator from [6] without offset calibration technique is shown in Fig. 2(c), where the  $Clk$  skew problem is resolved by replacing  $Clkb$  with  $Di$  nodes. As a result, the performance is not affected by clock skew and the clock load is reduced. In addition, the input-referred offset voltage and noise are reduced since this comparator has larger  $Di$  nodes capacitance and has double transconductance ( $g_m$ ) at  $Di$  nodes. However, these improvements are compromised with the increased delay since the current drivability of the output load is weakened due to the fact that transistor M12 and M13 use  $Di$  node voltages instead of  $Clkb$  signals, which are slow exponential decaying shape. Furthermore, the maximum drive current of each  $Out$  node is reduced to half of the single tail-current transistor (M12) in the comparator 1 of Fig. 2 since M12 is divided into two transistors (M12 and M13) in the comparator 2 of Fig. 2.

### 3 Proposed comparator

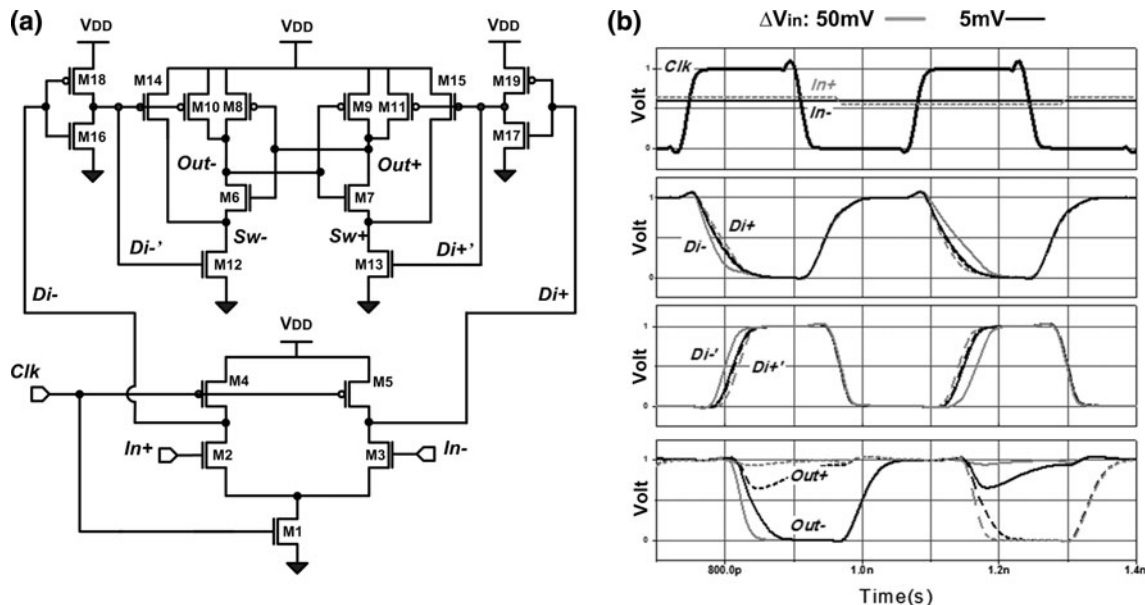
#### 3.1 Operation principles

The schematic and simulated waveforms of the proposed comparator [13] are shown in Fig. 3. The circuit is designed and simulated with HSPICE using 90 nm PTM Technology [9] at  $V_{DD} = 1$  V,  $f_{clk} = 3$  GHz,  $C_{load} = 7$  fF,

Temp. = 25°C, and input common-mode voltage  $V_{com}$  of 0.6 V. The basic structure of the proposed comparator stems from the comparators from [12] and [14]. The proposed comparator provides lower input-referred offset voltage and faster operation at the same area and power consumption while the advantages from the previous works are maintained.

During pre-charge (or reset) phase ( $Clk = 0$  V), both PMOS transistors M4 and M5 turn on and  $Di$  nodes' capacitances are charged to  $V_{DD}$ , which, in turn, make both NMOS transistor M16 and M17 of the inverter pair on and  $Di'$  nodes discharge to ground. Sequentially, PMOS transistor M10, M11, M14 and M15 turn on and  $Out$  nodes and  $Sw$  nodes are charged up to  $V_{DD}$  while both NMOS transistors M12 and M13 are off.

During evaluation (decision-making) phase ( $Clk = V_{DD}$ ), each  $Di$  node capacitance is discharged from  $V_{DD}$  to ground in a different rate proportional to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between  $Di+$  and  $Di-$  nodes. Once either  $Di+$  or  $Di-$  node voltage drops below  $V_{DD} - V_{tp}$ , the inverter pairs (M18/M16 and M19/M17) invert each  $Di$  node signal into the regenerated (amplified)  $Di'$  node signals. Then the regenerated and different phased  $Di'$  node voltages are relayed to the output-latch stage by M10–M13. As the regenerated  $Di'$  node voltage is rising from 0 V to  $V_{DD}$  with a different time interval (or a phase difference which increases with the increasing input voltage difference  $\Delta V_{in}$ ), M12 and M13 turn on one after another and the output latch starts regenerating the small voltage difference transmitted from  $Di'$  nodes into a full-scale digital level:  $Out+$  node outputs logic high ( $V_{DD}$ ) if  $Di+$  node voltage rises faster than  $Di-$  node voltage and  $Out+$  outputs logic low (0 V) otherwise. Once either of  $Out$  node



**Fig. 3** a Schematic of proposed comparator; b Signal behavior of proposed comparator ( $\Delta V_{in} = 50$  mV (Grey), 5 mV (Black) with  $V_{DD} = 1$  V,  $f_{clk} = 3$  GHz,  $C_{load} = 7$ fF, Temperature = 25°C and  $V_{com} = 0.6$  V)

voltages drops below  $V_{DD} - |V_{tp}|$ , this positive feedback becomes stronger because either PMOS transistor M8 or M9 will turn on.

Transistor M14 and M15 are used to reset  $S_w$  nodes to  $V_{DD}$  during pre-charge phase to prevent the pre-charge voltage mismatch between  $S_w$  nodes due to  $v_{th}$  mismatch between transistor M6 and M7 and to increase the voltage gain formed between  $S_w$  nodes during the evaluation phase by increasing the time duration for which transistor M12 and M13 operate in the saturation region.

As shown in Fig. 4(i) and (ii), the initial input voltage difference of 5 mV is amplified up to 110 mV before the transistor pair M6 and M7 in the latch (M6–M9) turn on. Therefore, the input referred offset voltage resulting from the mismatch between transistor M6 and M7 is attenuated by the voltage gain of  $G_1 \times G_2 \times G_3$  ( $= 22$  V/V); where  $G_1$  is the voltage gain between  $Di$  nodes and  $In$  nodes,  $G_2$  is the voltage gain between  $Di'$  nodes and  $Di$  nodes, and  $G_3$  is the voltage gain between  $S_w$  nodes and  $Di'$  nodes. In a similar way, the offset voltage of the output latch stage is attenuated by the gain of  $G_1 \times G_2$  and the offset voltage resulting from the mismatched inverter pair is attenuated by  $G_1$ .

In summary, the two additional inverters inserted between  $Di$  and  $Di'$  nodes enable the proposed comparator to have less input referred offset voltage in the output latch by amplifying (regenerating) the weakened  $Di$  node signals to  $Di'$  node signals. The output latch stage of the proposed comparator is the complementary version of the latch stage in the conventional design, which makes the proposed comparator deliver bigger load currents.

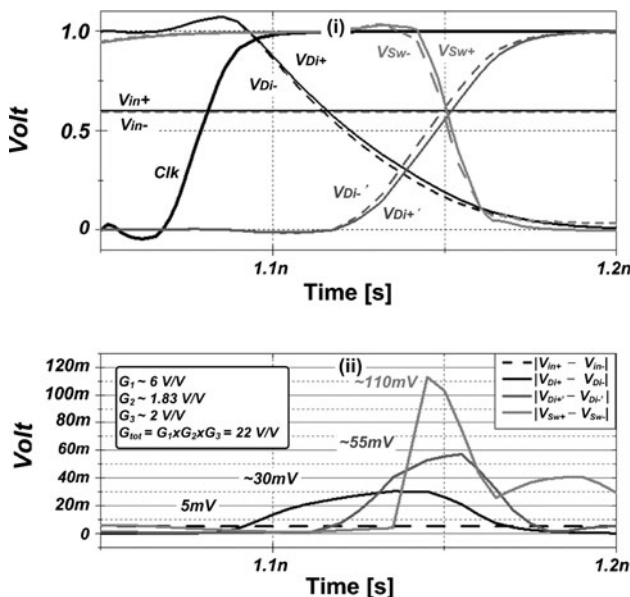


Fig. 4 *i* Detailed waveforms of Fig. 3(b) and *ii* absolute values of the voltage differences at between  $Di$ ,  $Di'$ , and  $S_w$  nodes

### 3.2 Offset voltage analysis

The offset voltage of the comparator results from the device mismatches, and the offset voltage of the proposed comparator can be expressed as

$$V_{OS\_Total} = \sqrt{V_{OS\_Diff\_Input}^2 + \frac{1}{G_1^2} V_{OS\_Inv\_Pair}^2 + \frac{1}{G_1^2 \times G_2^2} V_{OS\_Output\_Latch}^2} \quad (1)$$

where  $V_{OS\_Diff\_Input}$ ,  $V_{OS\_Inv\_Pair}$ , and  $V_{OS\_Output\_Latch}$  are the offset voltages resulting from the mismatched transistor pairs in each stage, respectively.  $G_1$  is the voltage gain between  $Di$  nodes and  $In$  nodes, and  $G_2$  is the voltage gain between  $Di'$  nodes and  $Di$  nodes.

To optimize the comparator in terms of the minimal offset voltage, the offset voltage contributions of each stage have to be verified first. Therefore, all transistors (but the inverter pairs) are designed to have the same aspect ratio of  $W/L = 1 \mu\text{m}/0.1 \mu\text{m}$ . In order for the inverter pair to have the proper gain and correct functionality, PMOS transistors of the inverter pair are designed three times larger than NMOS transistors ( $W_p/W_n = 1.5 \mu\text{m}/0.5 \mu\text{m}$ ). To simulate 1-sigma offset voltages for each stage, the random mismatch in threshold voltage  $V_{th}$  and current factor  $\beta$  ( $=\mu C_{ox} W/L$ ) for each transistor pair are modeled as follows [1],

$$\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{WL}}, \quad \sigma_{\beta} = \frac{A_{\beta}}{\sqrt{WL}} \quad (2)$$

where  $A_{V_{th}}$  and  $A_{\beta}$  are process dependent parameters and are assumed to be  $4.5 \text{ mV } \mu\text{m}$  and  $1\% \mu\text{m}$ , respectively in this mismatch analysis. As shown in Fig. 5 (in grey), the

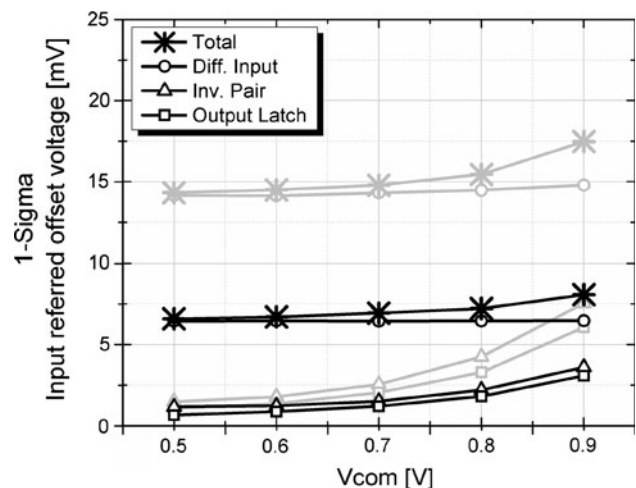
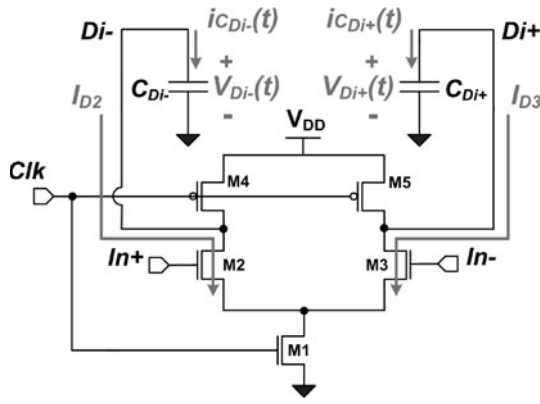


Fig. 5 Offset voltage contributions of each stage before (Grey) and after (Black) optimization



**Fig. 6** Simplified schematic of the dynamic differential input gain stage

input referred offset voltages of each stage of the comparator with respect to the different the input common mode voltages are extracted from 100 times of transient Monte-Carlo simulations ( $V_{DD} = 1$  V,  $f_{clk} = 3$  GHz). As expected, the offset voltage resulting from the mismatched transistor pairs in the regenerative output-latch stage is the smallest since it is reduced by the gain of  $G_1 \times G_2$ . The offset voltage from the mismatch between the inverter pair is reduced by the gain of  $G_1$ , and it is also small comparing to the offset voltage of the differential input stage.

As a result, the dominant part of the overall input referred offset voltage is caused by the mismatch between the differential input pair transistors. If less than 2 mV of 1-sigma offset voltage is required, each stage should have less than 1.2 mV of 1-sigma input referred offset voltage, which means the size of the input differential pair (M2/M3) has to be sized up around 140 times larger than the initial size (1  $\mu$ m). In the same way, other transistors also have to be sized up and the overall power consumption and the area increase considerably. Therefore, the technique to reduce the offset voltage without increasing power and area of the comparator is required and it has to be located between the input differential stage and the inverter pair to maximize the efficiency.

### 3.2.1 Offset voltage in differential input gain stage

The differential input stage of the proposed comparator is simplified for offset analysis as shown in Fig. 6. During evaluation phase ( $Clk = V_{DD}$ ), the input differential pair discharges each  $Di$  node voltage from  $V_{DD}$  down to 0 V with a different time rate proportional to each input voltage. Assuming  $\lambda = \gamma = 0$  for simplicity, since both transistor M2 and M3 operate in the saturation region between the time  $t_1$  and  $t_2$  ( $t_1$ : time at which transistor M1 is just turned on at the rising  $Clk$  edge and transistor M2 and M3

start operating in the saturation region,  $t_2$ : time at which either of transistor M2 or M3 moves out of the saturation region and goes into the linear region), the drain-to-source current of transistor M2 and M3 are constant over  $[t_1, t_2]$ . Therefore, these currents can be expressed as

$$C_{Di-} \frac{dV_{Di-}(t)}{dt} = -I_{D2} \quad C_{Di+} \frac{dV_{Di+}(t)}{dt} = -I_{D3} \quad (3)$$

Integrating both sides of (3) over  $[t_1, t]$  and applying the initial condition:  $V_{Di}(t_1) = V_{DD}$ , the following equations are obtained,

$$V_{Di-}(t) = V_{DD} - \frac{I_{D2}}{C_{Di-}} t \quad V_{Di+}(t) = V_{DD} - \frac{I_{D3}}{C_{Di+}} t \quad (4)$$

Then the dynamic voltage gain formed from inputs to  $Di$  nodes can be defined as (where  $\Delta V_{Di}(t) = V_{Di-}(t) - V_{Di+}(t)$  and  $\Delta V_{in} = V_{in+} - V_{in-}$ )

$$A_{V\_Diff.Input}(t) = \frac{\Delta V_{Di}(t)}{\Delta V_{in}} \quad (5)$$

Applying the small signal approximation:  $2(V_{GS2,3} - V_m) \gg \Delta V_{in}$  and assuming that  $C_{Di} = C_{Di+} = C_{Di}$ , Eq. 5 can be expressed as

$$A_{V\_Diff.Input}(t) = -\frac{g_{m2,3}}{C_{Di}} t \quad (6)$$

where

$$g_{m2,3} = \mu_n C_{ox} \frac{W_{2,3}}{L} (V_{com} - V_{D1}(t) - V_{m2,3})$$

and

$$V_{D1}(t) = (I_{D2} + I_{D3}) \times r_{ds1} \approx Constant$$

Equation 6 reveals that as long as the input transistor pair M2 and M3 operates in the saturation region, the dynamic gain  $A_{V\_Diff}(t)$  keeps increasing linearly as time increases. To maximize the gain  $|A_{V\_Diff}(t)|$ ,  $|g_{m2,3}/I_{D2,3}|$  should be maximized because the integration time  $t$  is proportional to  $C_{Di}/I_{D2,3}$  from Eq. 4. Since  $g_m$  in the saturation region is larger than the one in the linear region except for the sub-threshold operation, the input transistor pair M1 and M2 keeps operating in the saturation region longer by reducing the size of transistor M1. However, higher gain is obtained at the cost of the increased delay since the reduced  $I_{D2,3}$  increases the discharging time of  $Di$  node voltages during the evaluation phase.

The offset voltage ( $V_{OS\_Diff}$ ) of the input differential stage can be derived as [15] while the input transistor pair (M2 and M3) is operating in the saturation region.

$$V_{OS\_Diff.Input} = V_{OS2,3} = V_{GS2} - V_{GS3} \quad (7)$$

$$= \frac{1}{2} \sqrt{\frac{2I_D}{\beta}} \left[ -\frac{\Delta I_D}{I_D} + \frac{\Delta \beta}{\beta} \right] - \Delta V_m \quad (8)$$

$$= \frac{V_{GS2,3} - V_m}{2} \left[ -\frac{\Delta C_{Di}}{C_{Di}} + \frac{\Delta \beta}{\beta} \right] - \Delta V_m \tag{9}$$

Since mismatches are independent statistical variables, the random offset voltage ( $V_{OS,Diff}$ ) can be expressed as the variance of Eq. 9

$$V_{OS\_Diff\_Input}^2 = \Delta V_m^2 + \left( \frac{V_{GS2,3} - V_m}{2} \right)^2 \left\{ \left( \frac{\Delta C_{Di}}{C_{Di}} \right)^2 + \left( \frac{\Delta \beta}{\beta} \right)^2 \right\} \tag{10}$$

Equation 10 reveals that (i) the threshold voltage mismatch is directly referred to the offset voltage; (ii) the influence of  $Di$  node capacitance mismatch (which consists of the mismatch between the gate capacitances of inverter pair (M18/M16 and M19/M17) and the mismatch between the drain diffusion capacitances of the input transistor pair (M2 and M3)) and the mismatch between the current factor  $\beta$  mismatch on the offset voltage increase with the increasing common mode voltage  $V_{com}$ . Since the random device mismatch parameters are related to the size of transistors, the offset voltage can be reduced at the cost of the increasing size of the transistors, hence increasing area and power consumption. Equation 10 also presents that the offset voltage can be compensated by controlling the threshold voltages or the drain currents of transistor M2 and M3 and the size of the capacitances at  $Di$  nodes.

### 3.2.2 Offset voltage in regenerative output latch stage

The inputs of the regenerative output latch stage are at the gates of transistor M10–13 which are connected to  $Di-'$  and  $Di+'$  nodes. During the evaluation phase ( $Clk = V_{DD}$ ), each  $Di'$  node voltage rises from 0 V to  $V_{DD}$  with a different time interval if  $V_{in+} \neq V_{in-}$ . Therefore the output latch stage can make a decision whether logic high or low. However, both  $Di'$  node voltages rise up exactly at the same time rate if  $V_{in+} = V_{in-}$  and no mismatch exists. This makes both branches of the output latch stage maintain a balanced state [2], which means  $V_{out+(t)} = V_{out-(t)}$  during all the transient time. However, if a mismatch exists at the output latch stage, the circuit will be unbalanced and make  $V_{out+(t)} \neq V_{out-(t)}$ . In order for the circuit to be balanced, a voltage  $V_{OS\_Output\ latch}$  should be applied between the output of the inverter (M18/M16) and  $Di-'$  node to compensate the mismatch when  $Di'$  nodes rises. To calculate the offset voltage  $V_{OS\_Output\ latch}$  of the output latch stage, two random mismatches, current factor  $\beta$  ( $=\mu C_{ox}W/L$ ) and threshold voltage  $V_{th}$ , are considered as they are the dominant factors to cause the offset voltage in this analysis.

Although the operation regions of the transistors of the output latch stage vary with time, at the time point when

$Di'$  node voltage is around the threshold voltage of the transistor M12 (M13)  $V_{m12(13)}$ , those transistors just turn on and operate in the saturation region. Once  $V_{D12,13}$  ( $Sw$ ) node voltages drop down below  $V_{DD} - V_{m6(7)}$  from  $V_{DD}$ , transistor M6 and M7 also start turning on and operate in the saturation region since both their drain and gate voltages are dropping down at the same rate under the balanced condition. At this time, the transistor M10 and M11 operate in the linear region since both  $V_{out+}$  and  $V_{out-}$  are still around  $V_{DD}$ , and the effects of the reset transistor M14 and M15 on node  $V_{D12,13}$  are negligible because they are designed to be much smaller than transistor M12 and M13. The effects of the transistor M8 and M9 on  $Out\pm$  nodes are also ignored because they are in the cut-off region. Therefore, the output latch stage can be simplified as shown in Fig. 7 for analysis.

First, mismatch between transistor M12 and M13 is considered and other pairs are assumed to be perfectly matched. The load capacitance  $C_{L1}$  and  $C_{L2}$  are assumed to include the parasitic capacitances at  $Out\pm$  nodes and at this time,  $C_{L1}$  and  $C_{L2}$  are assumed to be the same and it is denoted as C.

$$I_{D12} = I_1 \quad I_{D13} = I_2 = I_1 + \Delta I_1 \tag{11}$$

$$I_1'' = -C_{L1} \frac{dV_{out-}}{dt} \quad I_2'' = -C_{L2} \frac{dV_{out+}}{dt} \tag{12}$$

Since  $V_{out-} = V_{out+}$  and  $dV_{out-}/dt = dV_{out+}/dt$  in the balanced condition [2], it is fair to say that

$$I_1'' = I_2'' = I'' \tag{13}$$

Also, from KCL and KVL, the followings are obtained

$$I_1' = I_1 - I_1'' \quad I_2' = I_2 - I'' \tag{14}$$

$$I_1'R_{10} = I_2'R_{11} \tag{15}$$

From (11) and (13)–(15),

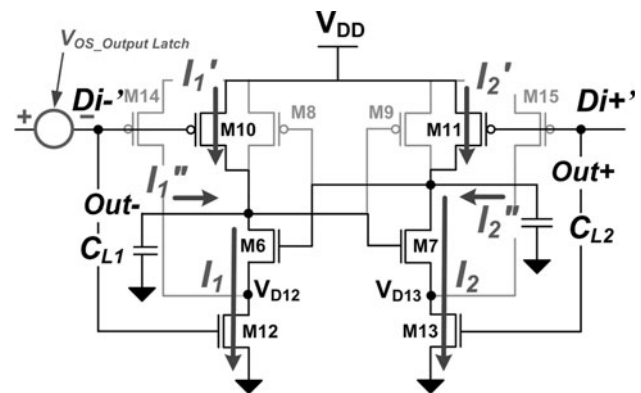


Fig. 7 Simplified schematic of the output stage combined with latch when  $Di'$  node voltages ( $V'_{Di}$ ) are reaching around  $V_{m12,13}$  during evaluation phase

$$\frac{\Delta I_1}{I_1} = \frac{\Delta I_D}{I_D} = \frac{R_{10} - R_{11}}{R_{10}} \left( 1 - \frac{I''}{I_1} \right) \quad (16)$$

From Eqs. 16 and 8, the following equation is obtained

$$V_{OS12,13}^2 = \left[ \left( \frac{V_{Di'} - V_{m12}}{2} \right)^2 \left( \frac{\Delta \beta_{12}}{\beta_{12}} \right)^2 + \Delta V_{m12}^2 \right] \times \left[ 1 + \frac{V_{Di'} - V_{m12}}{2(V_{DD} - V_{Di'} - |V_{tp10}|)} \left( \frac{I''_1}{I_1} \right) \right]^{-2} \quad (17)$$

The Eq. 17 shows the influence of transistor M10 and M11 (which are used as both reset switches and input transistors for the output-latch stage) on the output-latch stage offset voltage  $V_{OS\_Output\ latch}$ . In the double-tail comparators from [6, 12], since both the output branches of the output-latch stage are activated by *Clkb* signal (not by the signals generated from the dynamic pre-amplifier stage), only the pair of the input transistors transfers the gain generated from the previous stage. However, since the proposed comparator and comparator from [14] have two pairs of the input transistors which are linked each other, the offset voltages caused from one pair are compensated by the other input transistor pair. Therefore, the additional term followed by the negative square root term in Eq. 17 compensates the former offset voltage term caused by transistor mismatch between M12 and M13. As  $V_{Di'}$  increases from  $V_m$  to  $V_{DD} - |V_{tp}|$  and  $I''_1/I_1$  increases,  $V_{OS\_Output\ latch}$  is further reduced since the influence of the additional denominator term increases. While larger NMOS transistor M12 and M13 are desirable for low offset and large drive currents, larger PMOS transistor M10 and M11 are also required to have low offset by increasing  $I''_1/I_1$  ratio. Therefore, there is an optimal ratio between  $W_{12(11)}$  and  $W_{10(11)}$  at a limited area for minimum offset voltage.

For mismatch between transistor M6 and M7,  $\mu_n C_{ox}$  mismatch is considered instead of current factor  $\beta$  mismatch to find out the optimal ratio between the width of transistor M6(M7) and M12(M13). From the fact that  $I_{D12} = I_{D6}$  and  $I_{D13} = I_{D7}$ , we have

$$V_{OS6,7}^2 \approx \frac{W_6}{W_{12}} \left[ \left( \frac{\Delta \mu_n C_{ox}}{\mu_n C_{ox}} \right)^2 \frac{(V_{out+(-)} - V_{D12(13)} - V_{m6})^2}{4} + \Delta V_{m6,7}^2 \right] \quad (18)$$

Equation 18 shows that the offset voltage caused by the mismatch between the transistor M6 and M7 is a function of the sizes of the transistor M6(M7) and M12(M13). It seems as  $W_6/W_{12}$  increases,  $V_{OS6,7}$  decreases. However, as  $W_6$  decreases, the random mismatches of  $\Delta \mu_n C_{ox}$  and  $\Delta V_m$  increase. Therefore, there is a particular  $W_6/W_{12}$  ratio that makes an optimum tradeoff between them to have the minimum  $V_{OS6,7}$ .

In a similar way, the offset voltage  $V_{OS10,11}$  caused by the transistor mismatch between M10 and M11 can be found as follows.

$$V_{OS10,11}^2 = \left[ (V_{DD} - V_{Di'} - |V_{tp}|)^2 \left( \frac{\Delta \beta_{10}}{\beta_{10}} \right)^2 + \Delta V_{tp10}^2 \right] \times \left[ 1 + (V_{DD} - V_{Di'} - |V_{tp10}|) \left( \frac{g_{m12}}{I''_1} \right) \right]^{-2} \quad (19)$$

To calculate the offset voltage resulting from the capacitance mismatches at *Out* nodes (which includes the load capacitance and parasitic capacitance), it is necessary to assume that  $C_{L1} = C$  and  $C_{L2} = C + \Delta C$ . Applying this relationship to Eq. 12,

$$I''_1 = I'' \quad I''_2 = I'' + \Delta I'' \quad (20)$$

From (8), (14), (15) and (20), the following result is obtained.

$$V_{OS\_Clload}^2 = \left( \frac{V_{Di'} - V_m}{2} \right)^2 \left( \frac{\Delta C}{C} \right)^2 \times \left[ 1 + \frac{V_{Di'} - V_{m12}}{2(V_{DD} - V_{Di'} - |V_{tp10}|)} \left( \frac{I''_1}{I_1} \right) \right]^{-2} \quad (21)$$

Equation 21 shows that the offset voltage caused by the capacitance mismatch at the output nodes is affected more by the relative capacitance mismatch  $\Delta C/C$  than the absolute capacitance mismatch  $\Delta C$ . In addition, the Eq. 21 can be added to Eq. 17 because it has the same additional term in Eq. 17.

#### 4 Offset calibration techniques

Based on the offset voltage analysis and Monte-Carlo simulation, the proposed comparator was optimized for the minimal offset voltage. As a result, as shown in Fig. 5 (in Black), 1-sigma offset voltage was reduced from 12.5 to 6.5 mV at 0.6 V of input common mode voltage at the cost of 9% increase in the power dissipation (152  $\mu$ W from 136  $\mu$ W). To further reduce the offset voltage of the proposed comparator without pre-amplifier, digitally controlled capacitive offset voltage compensation technique is developed in this research.

As explained in Eq. 10, the offset voltage can be compensated by controlling *Di* node capacitance, current or threshold voltage of the differential input pair ( $V_{m2,3}$ ) [6–8]. The current calibration technique introduced in [6] exploits additional one pair of NMOS compensation transistors in parallel with the differential input pair and a charge pump. Even though these calibration techniques

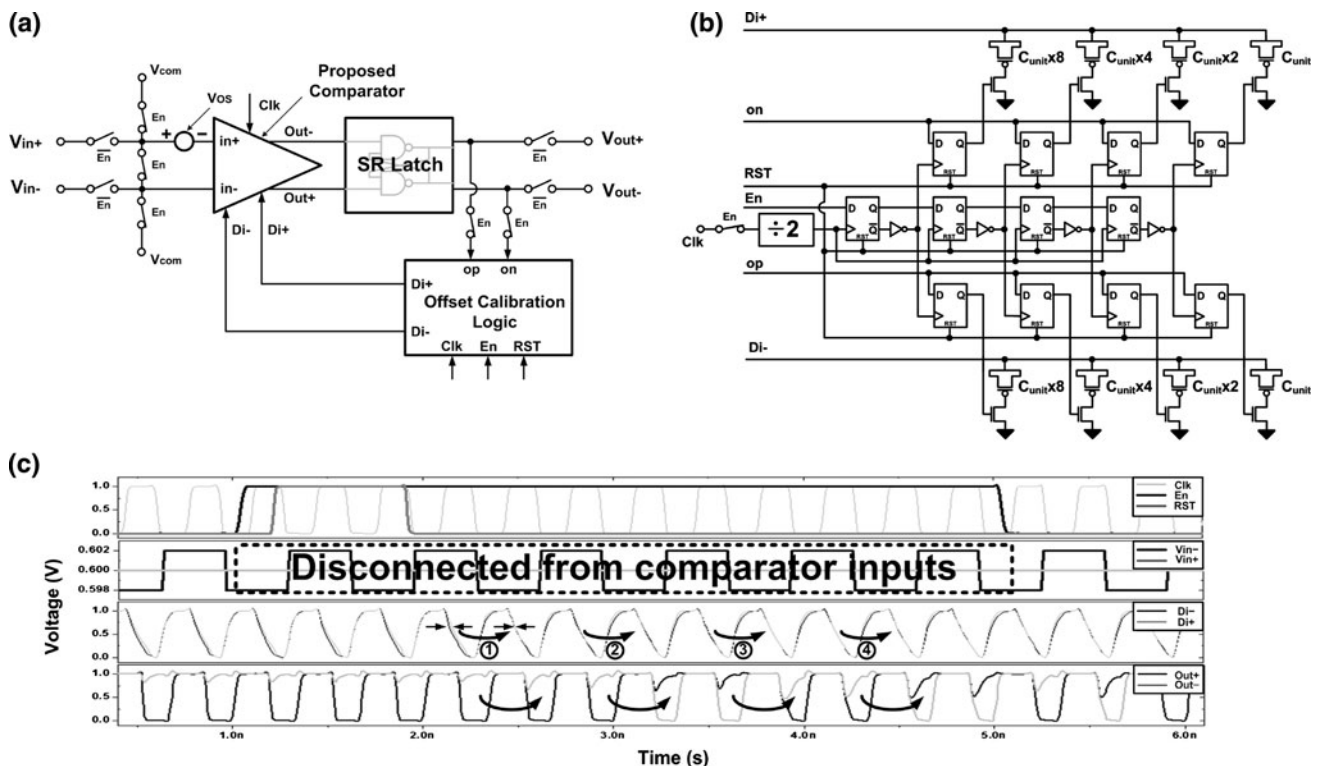
consume no static power, the calibration process has to be done frequently since the charged voltage in the compensation capacitor (which is connected to the gate of one of NMOS compensation transistor pair) falls down due to the leakage current. In addition, the calibration speed and accuracy are limited by the size of the charging/discharging current sources of charge pump. The digital calibration technique from [16] uses additional capacitance arrays to calibrate the offset voltage. Although the calibration resolution and the maximum offset coverage range are limited by the minimum unit capacitance and the number of bits of the capacitance arrays, this technique does not require the calibration refresh process and does not consume static power as well. In addition, the increase of the node

capacitance at  $Di$  node reduces the input referred noise. However, it slows down the speed of the comparator since  $Di$  node voltages in the comparators from [10, 12] and [6] are directly linked to the latch stage. The degree of speed degradation is more severe when this technique is applied to the internal nodes ( $Di\pm$ ) of the comparator from [6] since those internal node voltages are directly applied to the both input transistor pairs of the second stage. On the other hand, the speed of the proposed comparator is relatively less sensitive to the increase of the  $Di$  node capacitance due to the fact that the  $Di$  node voltages in the comparator are buffered by the inverter pair (Table 1).

Figure 8 shows the proposed offset calibration technique using 4-bit capacitor array, which consists of 4-bit

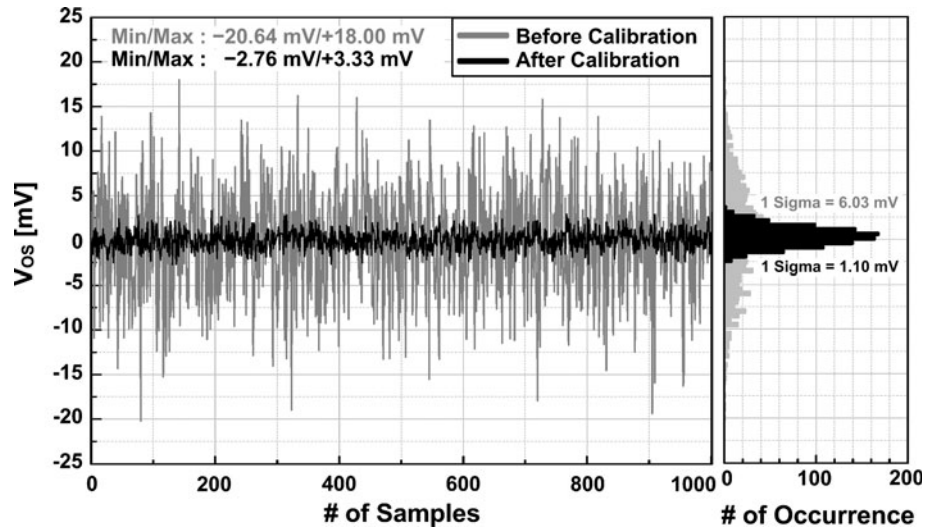
**Table 1** Performance comparison

	Ref. [12]	Ref. [6]	Ref. [7]	Ref. [8]	This work
$\sigma$ Vos (before cal.) (mV)	8	13.7	12.8	31.8	6.03
$\sigma$ Vos (after cal.) (mV)	–	1.68	3.8	4.3	1.10
Clock frequency	1 GHz	250 MHz	500 MHz	1.4 GHz	3 GHz
Delay [ps]/log( $\Delta V_{in}$ ) (ps/decade)	44	24.3	–	–	17
Power	113 $\mu$ W	40 $\mu$ W	39 $\mu$ W	350 $\mu$ W	162 $\mu$ W
	113 $\mu$ W/GHz	160 $\mu$ W/GHz	78 $\mu$ W/GHz	250 $\mu$ W/GHz	54 $\mu$ W/GHz
Process	90 nm	90 nm	90 nm	0.18 $\mu$ m	90 nm



**Fig. 8** a Proposed offset voltage calibration technique using  $Di$  node capacitance compensation. b Offset voltage calibration logic. c Signal waveforms of the proposed offset calibration process with the intentional  $V_{os}$  of +20 mV and  $f_{Clk} = 3$  GHz

**Fig. 9** Input referred offset voltage before and after offset calibration obtained from 1000 samples of transient Monte-Carlo simulations



shift register, divide-by-two circuit, D flip-flops, and 4-bit capacitor arrays, while the size of the unit capacitance is implemented with PMOS transistors ( $W/L = 120 \text{ nm}/100 \text{ nm}$ ). The proposed comparator operates above the clock frequency of 3 GHz. However, the calibration logic timing needs more time and the calibration logic uses the half clock frequency using the divide-by-two clock frequency divider. Therefore, the timing requirement for the offset calibration logic is relaxed with an extra clock cycle added after switching on each binary weighted capacitor. Before calibration, as shown in Fig. 7(c), the output of the comparator outputs logic low (0 V) regardless of the input differential voltage of  $\pm 2 \text{ mV}$  due to the intentional input referred offset voltage of 20 mV. After calibration, however, the proposed comparator can distinguish the input differential voltage that is even less than  $\pm 2 \text{ mV}$ . The required calibration time is only about 4 ns at  $f_{clk} = 3 \text{ GHz}$  and the reset signal (RST) can be simply generated using 3-bit shift register, inverters, switches and an AND gate, which is initiated by the enable signal (En).

## 5 Simulation result

The proposed comparator with a capacitive offset voltage calibration circuit is designed and simulated in HSPICE using 90 nm PTM process. To compare the input referred random offset voltages of the proposed comparator before and after offset calibration, 1000 times of transient Monte-Carlo simulations are performed with the random mismatch model from Eq. 2, where  $A_{vth} = 4.5 \text{ mV } \mu\text{m}$  and  $A_{\beta} = 1\% \mu\text{m}$ , and the total input referred offset voltage was measured by applying slowly varying slope signals to the comparator inputs. As shown in Fig. 9, 1-sigma offset

voltage of 6.03 mV was reduced to 1.10 mV with switching frequency of 3 GHz and the power consumption of 162  $\mu\text{W}$  after the offset calibration.

## 6 Conclusion

A novel dynamic latched comparator is proposed, designed and simulated using 90 nm PTM technology. The proposed comparator requires one phase clock signal for its operation and can drive a larger capacitive load with a complementary version of the output-latch stage of the conventional comparator design. As it provides a larger voltage gain up to 22 V/V to the regenerative latch, the input referred latch offset voltage is reduced and metastability characteristic is improved. The simulation result shows 24.6% less offset voltage and 30.0% less sensitivity of delay to the decreasing input voltage difference (17 ps/decade) than the conventional double-tail latched comparator at approximately the same area and power consumption. In addition, with a digitally controlled capacitive offset calibration technique, the offset voltage of the proposed comparator is further reduced from 6.03 to 1.10 mV at 1-sigma at the operating clock frequency of 3 GHz and it consumes 54  $\mu\text{W}/\text{GHz}$  after the calibration.

## References

- Pelgrom, M. J. M., Duinmaijer, A. C. J., & Weblbers, A. P. G. (1995). Matching properties of MOS transistors. *IEEE Journal of Solid-State Circuits*, 24(10), 1433–1439.
- He, J., Sanyi, Z., Chen, D., & Geiger, R. L. (2009). Analyses of static and dynamic random offset voltages in dynamic comparators.

*IEEE Transactions on Circuits and Systems I: Regular Papers*, 56, 911–919.

3. Nikoozadeh, A., & Murmann, B. (2006). An analysis of latch comparator offset due to load capacitor mismatch. *IEEE Transactions on Circuits and Systems Part II: Express Briefs*, 53(12), 1398–1402.
4. Figueiredo, P. M., & Vital, J. C. (2006). Kickback noise reduction techniques for CMOS latched comparator. *IEEE Transactions on Circuits and Systems*, 53(7), 541–545.
5. Murmann, B., et al. (2006). Impact of scaling on analog performance and associated modeling needs. *IEEE Transactions on Electron Devices*, 53(9), 2160–2167.
6. Miyahara, M., Asada, Y., Daehwa, P., & Matsuzawa, A. (2008). A low-noise self-calibrating dynamic comparator for high-speed ADCs. In *Proc. A-SSCC*, Nov 2008, pp. 269–272.
7. Miyahara, M., et al. (2009). A low-offset latched comparator using zero-static power dynamic offset cancellation technique. In *IEEE A-SSCC*, Taiwan, pp. 233–236.
8. Wong, J., et al. (2004). Offset compensation in comparators with minimum input-referred supply noise. In *IEEE JSSC*, May 2004, pp. 837–840.
9. <http://www.eas.asu.edu/~ptm/latest.htm>.
10. Kobayashi, T., Nogami, K., Shirotori, T., & Fujimoto, Y. (1993). A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture. *IEEE Journal of Solid-State Circuits*, 28, 523–552.
11. Wicht, B., Nirschl, T., & Schmitt-Landsiedel, D. (2004). Yield and speed optimization of a latch-type voltage sense amplifier. *IEEE Journal of Solid-State Circuits*, 39, 1148–1158.
12. Schinkel, D., Mensink, E., Klumperink, E., van Tuijl, E., & Nauta, B. (2007). A double-tail latch-type voltage sense amplifier with 18 ps setup + hold time. In *ISSCC Dig. Tech. Papers*, Feb 2007, pp. 314–315 and 605.
13. Jeon, H. J., & Kim, Y.-B. (2010). A low-offset high-speed double-tail dual-rail dynamic latched comparator. In *ACM GLSVLSI*, Providence, May 2010.
14. van Elzakker, M., van Tuijl, A. J. M., Geraedts, P. F. J., Schinkel, D., Klumperink, E. A. M., & Nauta, B. (2008). A 1.9  $\mu$ W 4.4fJ/conversion-step 10b 1MS/s charge-redistribution ADC. In *ISSCC Dig. Tech. Papers*, Feb 2008, pp. 244–245.
15. Razavi, B. (1995). *Principles of data conversion system design*. Piscataway, NJ: IEEE Press.
16. Van der Plas, G., Decoutere, S., & Donnay, S. (2006). A 0.16 pJ/conversion-step 2.5 mW 1.25 GS/S 4b ADC in a 90 nm digital CMOS process. In *IEEE ISSCC Dig. Tech. Papers*, Feb 2006, pp. 566–567.



**HeungJun Jeon** was born in Seoul, Korea, in 1981. He received the BS degree in electrical and electronics engineering from Hanyang University, Ansan, Korea, in 2006. He is currently working toward the PhD degree with Northeastern University, Boston, MA. His research interests include low-power high-speed analog and mixed-signal circuit design and DC–DC converters.



**Yong-Bin Kim** (S'88-M'88-SM'00) received the BS degree in electrical engineering from Sogang University, Seoul, Korea, in 1982, the MS degree in electrical engineering from New Jersey Institute of Technology, Newark, NJ, in 1989, and the PhD degree in electrical and computer engineering from Colorado State University, Fort Collins, in 1996. From 1982 to 1987, he was with Electronics and Telecommunications Research Institute, Korea, as a

member of the technical staff. From 1990 to 1993, he was with Intel Corp. as a Senior Design Engineer and involved in micro-controller chip design and Intel P6 microprocessor chip design. From 1993 to 1996, he was with Hewlett Packard Co., Fort Collins, as a member of the technical staff and involved in HP PA-8000 RISC microprocessor chip design. From 1996 to 1998, he was with Sun Microsystems, Palo Alto, CA, as an individual contributor and involved in 1.5 GHz Ultra Sparc5 CPU chip design. From 1998 to 2000, he was an Assistant Professor in the Department of Electrical Engineering of the University of Utah, Salt Lake City. He is currently Associate Professor in the Department of Electrical and Computer Engineering at Northeastern University, Boston, MA. His research focuses on low-power analog and digital circuit design as well as high-speed low-power VLSI circuit design and methodology.