

8Gb/s Capacitive Low Power and High Speed 4-PWAM Transceiver Design

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ABSTRACT

In this paper, capacitive 4-PWAM transmitter architectures and circuits are proposed and its performances are analyzed with random jitter and PVT variation comparing with other works. A novel technique is proposed to reduce power and to increase speed by using capacitive driven low swing transceiver. The proposed design saves 1.74-2.4x power and 4x higher data rate than conventional designs. To implement 4-PWAM transmitter new phase controller and adaptive capacitance network are designed. At receiver side, new architectures for PWM and PAM demodulation are proposed.

Categories and Subject Descriptors

B.7.1 [Integrated Circuit]: Input/output circuits

General Terms

Algorithms, Measurement, Performance, Design, Reliability, Experimentation, Verification.

Keywords

Capacitive, Transmitter, Receiver, Transceiver, Pulse Width Modulation, Pulse Amplitude Modulation, PWM, PAM, PWAM. Low Power, High Speed, High Performance.

1. INTRODUCTION

In the past decade, the data processing speed of the computer systems has increased dramatically. On the other hand, the capabilities of data communication become a bottleneck of the whole system. Therefore, high-speed, low power wire-line communication is required by the modern computer systems, and the demand for more sophisticated input/output (I/O) transceiver design is increased accordingly. Serial link transceivers have a very wide application from chip-to-chip communications to the backplane and Ethernet.

However, the environment of the communication channel and the

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semiconductor technology limit the maximum symbol rate of the serial data transmission. Therefore, many researches have been published to increase the data rate while keeping the same symbol rate and sustaining the signal integrity. Among them, pulse-amplitude modulation (PAM) [1] and pulse-width modulation (PWM) [2] are two advanced modulation schemes. [3] firstly introduced a transceiver that uses both PWM and PAM modulation to boost the data transmission rate. However, its application is limited to a relatively low-speed data transmission (250M symbol/s) and it utilizes the conventional PWM and PAM symbol representations. The pulse width and pulse amplitude of each symbol are equally divided as shown in Fig. 1(a) and (b). This paper presents a novel and universal PAM and PWM combination scheme, where the unit pulse width and the basic pulse width are determined by the channel environment and the jitter specification instead.

Due to switched capacitances of interconnect, on-chip wires also present an increasing energy problem. A CMOS wire driver running at an effective frequency must switch a total wire capacitance C_w through the voltage, leading to a power cost proportional to $C_w V_{dd}^2 f$. Under technology scaling C_w remains largely constant (for global wires spanning constant-sized die), voltage scales down only slowly, and frequency (f) scales up, leading to nearly constant power per wire. However, as chip's device integration level is increasing continuously, this constant power per wire gets multiplied by an ever-increasing number of wires. Novel techniques are also proposed in this paper to compensate the channel loss of different symbols.

Circuits using optimized low-voltage swings have shown 10X energy savings, but at 30% latency penalty and reduced noise margins [4]. More problematically, such low-swing systems typically require an expensive second power supply, which breaks up power distribution planes on the chip and in the package and necessitates additional voltage regulator modules at low target impedances.

To overcome these drawback of the low swing techniques, a coupling capacitor in line with the long wire pre-emphasizes transitions is proposed in [5][6] to reduce wire delay and to reduce the load seen by the driver. It also lowers the wire's voltage swing without additional power supply. In this paper, to maximize the speed and minimize the power, new PWAM scheme with capacitive transceiver is proposed

2. PWAM SCHEME

PWAM-(M×N) scheme combines PAM-M (M is the number of different voltage levels) and PWM-N (N is the number of different pulse widths) together.

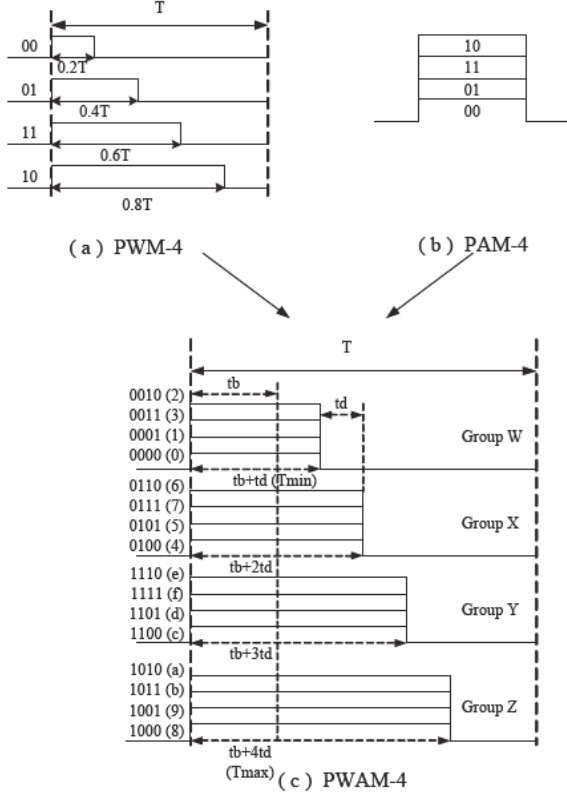


Figure 1. The PWAM Signaling (a) Conventional Symbols (b) Conventional PAM-4 Symbols (c)PWAM-(4×4) Symbols

With M different pulse amplitudes and N different pulse widths, there exist M×N different symbol representations [8]. M×N symbols represent $\log_2 M + \log_2 N$ bit binary information. Therefore, the bit rate of PWAM-(M×N) is $\log_2 M + \log_2 N$ times the symbol rate. PWAM-(4×4) is illustrated in Fig. 1(c) as an example to show the symbol representations of PWAM. One PWAM-(4×4) symbol denotes 4-bit data. The 4-bit data have 16 different values, thus 16 PWAM-(4×4) symbols are used to stand for 16 different values (hereafter, 4-bit data are represented by hex 0, 1, ..., a, b, c, d, e, f). These 16 symbols are divided into four groups as shown in Fig. 1(c): Group W, X, Y, Z consists of symbol 0 1 2 3, symbol 4 5 6 7, symbol c d e f, and symbol 8 9 a b, respectively.

3. DRIVING A WIRE WITH A CAPACITOR

Driving a long wire of capacitance C_w through a capacitor C_c reduces the signal swing on the wire through capacitive voltage divider [7]. As shown in Fig. 2, including parasitic capacitance on the right side of the coupling capacitor and including the final load capacitance gives a final wire voltage swing of $V_{swing} =$

$V_{DD} C_c / (C_c + C_w + C_{p2} + C_l)$. Typically, C_{p2} and C_l are both small compared to C_w .

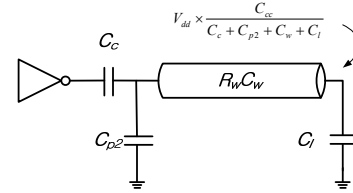


Figure 2. The capacitively driven wire

The node immediately after the coupling capacitance will initially overshoot and then settle to V_{swing} , while the end of the wire will show a rapid rise to the final V_{swing} voltage.

Because it acts as a high-frequency short, the capacitor increases the 3-dB bandwidth of the long wire, allowing shorter cycle times and decreasing latency. Long wires have a low-pass frequency response that limits their operating speed. Capacitive coupling to a long wire creates a pole-zero pair, giving high-frequency emphasis that mitigates the low-pass wire response and increases performance

4. ENERGY CONSUMPTION OF TRANSCIEVER

The energy-cost for a rising edge with swing V equals the well-known $E = CV^2$. Half of this energy is dissipated during charging. The other half is stored in the interconnect and dissipated at a later time when the interconnect is discharged (the resistance of the interconnect prevents efficient charge-recycling techniques). To reduce the link power, it hence makes sense to reduce the swing. If only a single supply voltage is available and active circuits are used to reduce the swing, there is no quadratic but linearly relation with the swing. When a dedicated supply voltage is available to generate the low-swing signal, then the power is again quadratically dependent on the swing. Therefore, many low-swing techniques with a dedicated supply voltage (either generated on- or off-chip) for the transmitter have been introduced in the past [11], [12], [13].

The capacitive transmitter uses a series capacitance (C_c) to drive the interconnect, as shown earlier in Fig. 2. This capacitance, together with the wire capacitance, acts as a capacitive divider which reduces the swing by a factor of $C_c / (C_c + C_w + C_{p2} + C_l)$. The capacitive transmitter also increases the bandwidth of the interconnect [5],[9], as it emphasizes each transition with an overshoot. Compared to the low-swing transmitters that switch between supplies, the capacitive transmitter is much less sensitive to supply noise, as the capacitor divider also attenuates this noise. Furthermore, it does not require a special supply voltage, and lowers the energy consumption by using a simple structure at the driver circuits.

5. 4-PWAM CIRCUIT DESIGN

In this chapter block diagram and circuits of the proposed 4-PWAM transceiver will be described.

5.1 Transmitter circuit

The PWAM transmitter is shown in detail in Fig. 5. It contains three main building blocks: a PWM modulator, a PAM modulator, and 8 phase PLL. An 8 Phase PLL provides evenly spaced clock

phases that are used to produce PWM-encoded signals. After processing Tx-bit0 and Tx-bit1 using the PWM technique, PAM signaling is used to modulate the information from Tx-bit2 and Tx-bit3. In addition to the PWAM modulator, In addition to the PWAM modulator, capacitively driven wire act as a pre-emphasis block. Pre-emphasis compensates for the limited bandwidth of the package leads and channel medium [8].

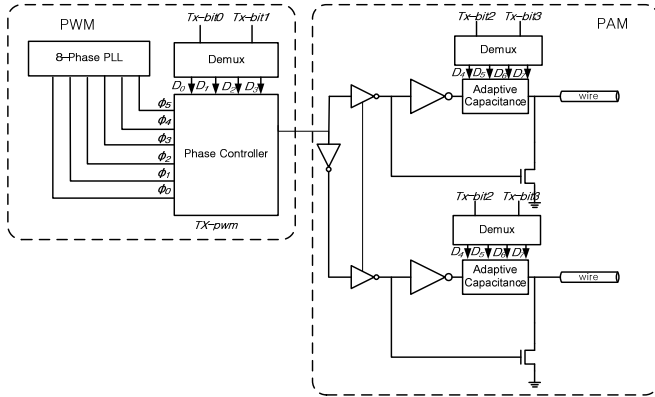


Figure 3: The block diagram of the transmitter

5.1.1 2-PWM modulator

The pulse width modulation can be implemented by the 8 phase PLL and phase controller. 6 phase signals and control data D0~D3 are used as inputs. Based on their combinations, the pulse width is determined. The phase controller and its timing diagram are shown in Fig 4 and Fig 5, respectively.

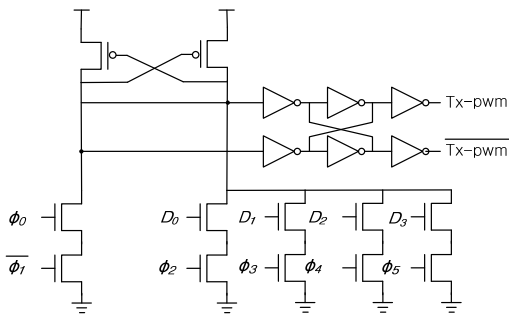


Figure 4: Phase controller

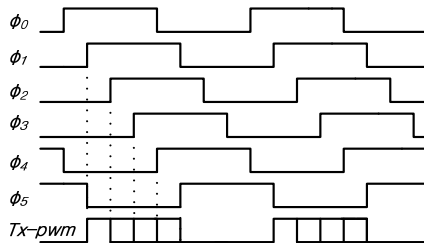


Figure 5: Timing diagram of Phase controller

5.1.2 2-PAM Modulator with capacitive pulse amplitude scheme

In order to realize low power PAM modulator, the low swing capacitive pulse amplitude modulation scheme is proposed in this paper. The capacitive PAM driver can be implemented using adaptive capacitance which is shown in Fig. 6. The bit3, bit4 determine the output of the Demux D1 ,D2 ,D3 ,D4 which consequently decide the capacitance. By changing the capacitance, multiple V_{swing} can be obtained, and the level of the voltage swing V_{swing} is expressed as Equation (1)

$$V_{swing} = V_{DD} (\sum D_k C_{ck} + C_W + C_{p2} + C_1) \quad (1)$$

Where D_k is $\{0,1\}$ and C_{ck} is a capacitance element of adaptive capacitance network.

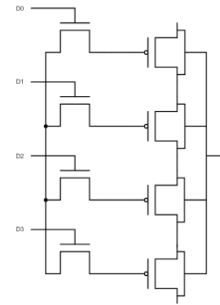


Figure 6: Adaptive Capacitance

5.2 RECEIVER CIRCUITS

Fig.7 shows the block diagram of the receiver. The receiver consists of 4 differential amplifier, 4 comparators, one PLL, the pulse width demodulation circuits, and supplementary circuits. Bit2 and bit3 are recovered by PAM demodulator and bit1 and bit0 are generated from pulse width demodulation circuits. As shown in Fig 7. The architecture of the PWM demodulator is quite simple. It is composed of three D-latch and a 3bit to 2bit decoder. The PLL in the receiver end provides 8-phase clock required by the pulse width demodulation circuit. The timing diagram of the PWM architecture is shown in Fig. 8.

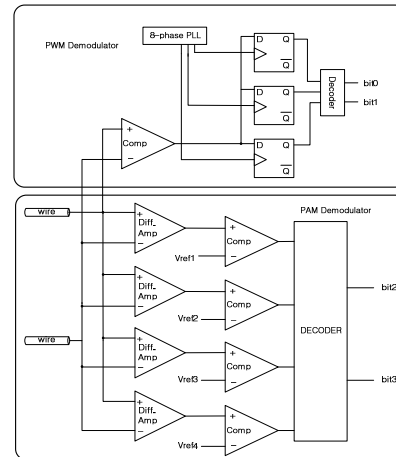


Figure 7: Receiver circuits

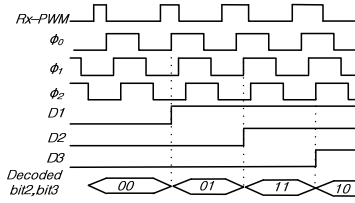


Figure 8: Timing diagram of PWM Demodulation

Because the voltage swing of the signal received from wire is small, it is amplified by differential amplifier ($\Delta V_{swing} = 100\text{mv}$). The different amplitude level of the received signal after amplification is 200mV. Accordingly, the reference voltages for comparators are $V_{ref1} = 1.5V$, $V_{ref2} = 1.3V$, $V_{ref3} = 1.1V$, and $V_{ref4} = 0.9V$. This multiple voltage references can be obtained from [10]. After amplification, the signal is fed into the comparator which determines digital output 0 or V_{DD} . The final bit2 and bit 3 are recovered by the decoder based on comparator output. Table 1 shows the comparator out mapping with bit2 and bit3.

Table 1. Decoded bit2, bit 3 from comparator out

Comparator out: 1,2,3,4				Bit2	Bit3
1	1	1	1	0	0
0	1	1	1	0	1
0	0	1	1	1	0
0	0	0	1	1	1

6. SIMULATION RESULTS

The circuit simulation has been done with $0.18\mu\text{m}$ CMOS technology, wire length of 2 mm, $C_{wire} = 560\text{fF}$, $R_{wire} = 400\Omega$, $=1.2V$, and $V_{DD} = 1.8V$. Figure 9 shows eye diagrams of the 4 different pulse widths and 4 different levels of voltage amplitudes. The voltage difference of each level is around 100mv in the proposed design. In order to test the proposed 4-PWAM transceiver, the PRBS-11 signal is used. The test was done with various environments with Monte Carlo method with 1000 times iteration.

The first test was accomplished without any random jitter and PVT variations. The eye diagram for this was shown in figure 9 (a). The proposed transceiver works without any error (BER=0) and there is only data dependent jitter which is $\Delta T_{rms} = 11.2\text{ps}$ and $\Delta T_{pk-pk} = 70.1\text{ps}$.

The second simulation was done by adding random jitter which has Gaussian distribution with nominal value = 50ps and variation = 0.1, $\sigma = 3$. The eye diagram of this environment is shown in figure 9 (b). As shown in the figure 9 (b), the eye is almost 90% opened. As a result, the bit errors are too small to measure.

The third simulation is done by putting process variation with Gaussian distribution which of 0.1 channel length and width variation and 3σ . Its eye diagram is shown in figure 9 (c). The eye is almost closed between 1.29 ~ 1.49. As the eye is getting closed, the bit error happens because of misreading in comparator voltage level. In this case the bit error rate is expected to be less than 10^{-10} .

The fourth simulation is combining the random jitter and process variation used in second and third simulation. As shown in figure 9 (d), the only difference between the third and the fourth simulation result is the random jitter increase. Because the random jitter in this case is not affecting the bit error rate, the fourth simulation case has same bit error rate with the third one.

In order to see the effect of the supply voltage variation, another simulation was done. The simulation of supply voltage variation was performed with Gaussian distribution which has 0.01 ~ 0.1 variations and 3σ for voltage. By changing the voltage variation, it is observed that the eye opening is changing drastically. Figure 9 (e) shows eye-diagram for 0.01 variation and figure 9 (f) shows eye-diagram for 0.5 variation. At 0.01 variation the eye is almost 60~70% open and as the variation goes over 0.5, the eye is completely closed. As a result, the bit error rate is increased about 10^{-8} which can be expected from Gaussian distribution function. The figure 10 shows the expected bit error rate with supply voltage variation.

From the eye-diagram analysis, it is concluded that the proposed transceiver is sensitive to voltage variations which come from process and supply voltage variation but not from random jitter.

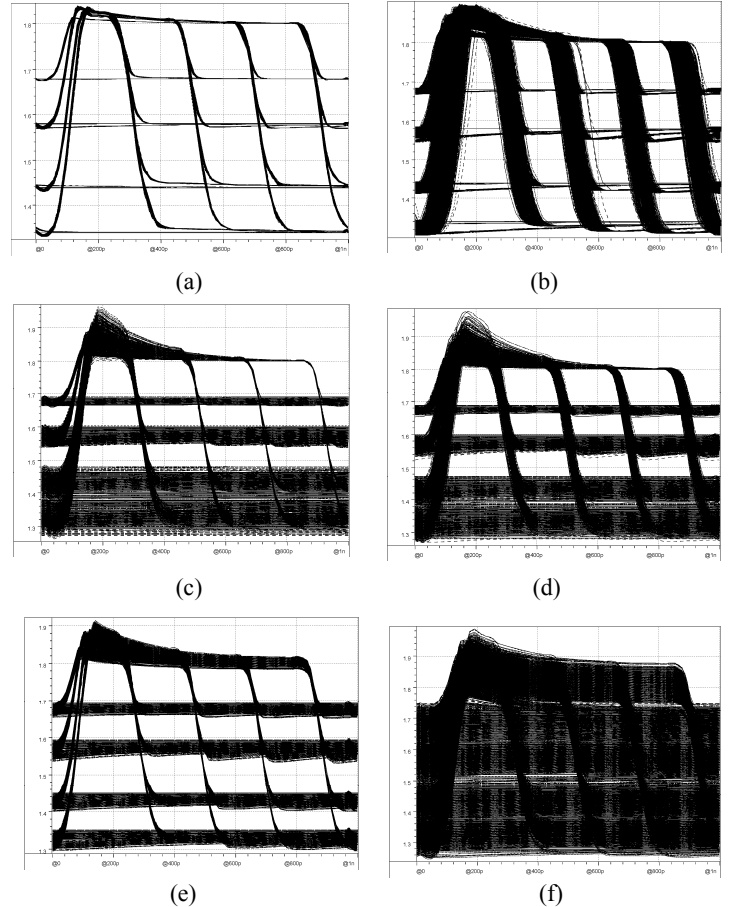


Figure 9. Eye-diagram of received PWAM signals (a) without random jitter, PVT variations (b) with random jitter (c) with process variation (d) with process variation and random jitter (e) supply voltage variation (variation = 0.01) (f) supply voltage variation (variation = 0.05)

Because of the PWAM scheme and capacitively driven method, the data rate in this work is higher than any other scheme. It is impossible to make the pulse width 20% of clock cycle over 1.5GHz, consequently the maximum frequency of this work is 1.5GHz. However, in the [9], it does not need to separate the clock cycle and it can increase the clock up to 5GHz with 50% eye opening. In case of capacitively driven wire, the data dependant jitter is less than other method. The voltage swing determines data dependant jitter because large voltage swing generally takes more ring and falling time. Consequently the data dependant jitter of this is less than [7] but larger than [9].

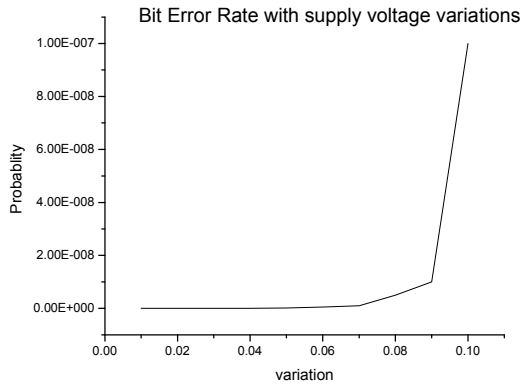


Figure 10. Bit error rate with supply voltage variations.

The bit rate was summarized in Table 2 in the worst case of each simulation environments.

To compare the performance of this work to others, [7] and [9] were implemented and its simulation results are summarized in Table 3. The proposed transceiver consumes more power than [9] but shows less power consumption than [7]. The results prove that the voltage swing is dominant for power consumption.

Table 2. Bit Error rate with Random jitter and PVT variation

	Random Jitter	Process Variation	Voltage Variation	Temperature Variation
BER	N/A	$<10^{-10}$	$<10^{-8}$	N/A

Table 3. Summary of the performances and comparison

Reference	[7]	[9]	This work
Technology	0.18 μ	90nm	0.18 μ
Supply	1.8V	1.2V	1.8V
Max. Voltage Swing	900mV	120mv	400mv
Power dissipation	Tx : 86mW Rx : 79mW	Tx : 14.4mW Rx : 18.4 mW	Tx : 36.5 mW Rx : 45.2 mW
Data rate	2Gb/s	5Gb/s	8Gb/s
Jitter	$T_{rms} = 49.9$ ps $T_{pk-pk} = 180$ ps	$T_{rms} = 9.8$ ps $T_{pk-pk} = 58.2$ ps	$T_{rms} = 11.2$ ps $T_{pk-pk} = 70.1$ ps

7. CONCLUSION

In this paper, capacitive 4-PWAM transmitter architecture is proposed and its performances are analyzed with random jitter and PVT variation comparing with other works. To implement 4-PWAM transmitter new phase controller and adaptive capacitance network is designed. At the receiver side, new architecture for PWM and PAM demodulation is proposed.

The 4-PWAM transceiver in this work has low data dependant jitter which does not affect the bit error rate. But it is very sensitive to supply voltage variation. It is because voltage difference between amplitude modulation is relatively low (100mv) which causes low noise margin. But if the supply voltage variation is lower than 5%, the bit error rate will be less than 10^{-10} .

The proposed capacitive 4-PWAM transmitter with low swing voltage can save a lot of power consumption comparing with the full swing one and other PAM scheme. Furthermore it can increase data rate with PWAM modulation and pre-emphasis [5]. In this paper, the proposed transceiver demonstrates that almost 1.74~2.4 times power is saved compared to [7] and 4 times higher data rate than [9] is accomplished.

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