Read-Out Schemes for a CNTFET-based Crossbar Memory

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ABSTRACT
This paper investigates read-out schemes for a crossbar memory using CNTFET-based elements as cross-points. Two read-out schemes are presented in this paper; the first scheme biases the selected junction and measures the current flowing from the junction toward the ground while the second scheme involves biasing all other unselected bits and/or wordlines. Two figures of merit (the sense voltage on/off ratio and the sense current noise margin) are used to investigate the effectiveness of the proposed schemes for the CNTFET-based crossbar memory. Simulation results show that the CNTFET-based crossbar memory achieves improvements in both sense voltages on/off ratio and noise margin compared to the molecular memory implementation. Therefore, this paper demonstrates that these schemes make the CNTFET-based design a viable candidate for crossbar memory in the nanoscale era.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles –*Memory technologies*

General Terms
Measurement, Performance, Design.

Keywords
Carbon Nanotube Field Effect Transistor; crossbar design; read-out circuit; noise margin.

1. INTRODUCTION
Crossbar arrays equipped with molecular switches have been used to configure interconnects, memories as well as logic units [1][2]. Molecular switches are placed at the intersection of the wires (hence referred to as crosspoints) and data is stored in the memory by switching the cross-point devices on and off (i.e. acting as a diode). The significant advantage of a crossbar memory is its simplicity, because only a switchable (antifuse) layer and a diode are required per cell [3]. The small size of a crosspoint makes it possible to fabricate an extremely dense memory structure based on a configurable two dimensional array of wires, also known as a crossbar. However, there are few drawbacks associated to a crossbar memory the small on-off resistance ratio requires a large sense resistor at the output of the crossbar memory. Also, if the diode is non-ideal, then the parasitic currents overwhelm the sense current, thus limiting the dimension of a crossbar memory; moreover, crossbar memories are mostly passive circuits and have no amplifying/signal restoring element. This can severely limit their scalability [4].

Carbon nanotube field effect transistors (CNTFETs) utilize semiconducting single-wall CNTs to assemble electron devices similar to MOSFETs, and the efficient fabrication of CNTFETs has been reported in recent years. CNTFETs are especially promising in nanoscale devices because their unique one-dimensional band-structure suppresses backscattering and makes near-ballistic operation a realistic possibility [5]. A CNTFET has a significantly smaller off current; therefore, the power consumed when the transistor is off, is greatly reduced in CNTFET-based designs. These properties make the CNTFET one of the promising new devices to extend or complement a traditional silicon technology for high performance and low power. The MOSFET-like CNTFET model has been reported to be scalable down to 10nm channel length or less [6]. This makes the CNTFET a promising candidate as crosspoint of a crossbar memory. Meanwhile, the large on-off current ratio of the CNTFET greatly limits the leakage current from affecting the sense current.

The objective of this paper is to propose two read-out schemes for a crossbar memory in which rather than molecular switching devices, CNTFET-based elements are utilized as crosspoints. Two figures of merit (the sense voltage on/off ratio and the sense current noise margin) are used in this paper to compare the effectiveness of the CNTFET-based memory with an existing molecular-based memory. Extensive simulations are performed on both the molecular and the CNTFET-based crossbar memories. HSPICE simulation results confirm that using the two read-out schemes, the CNTFET-based crossbar memory has a significantly higher sense voltage on/off ratio and sense current noise margin compared with the molecular crossbar memory.

2. CARBON NANOTUBE FIELD EFFECT TRANSISTOR
A single-wall Carbon nanotube (or SWCNT) consists of one cylinder only, and is one of the most promising CNT structures for use as a transistor. A SWCNT can act as either a conductor or a semiconductor depending on the angle of the atom arrangement along the tube. This is called the chirality vector and is

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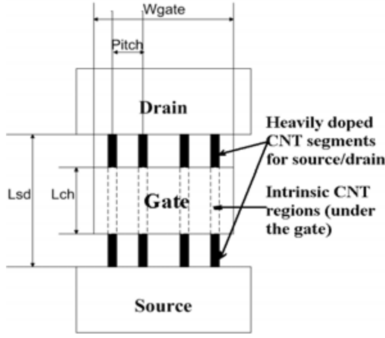

Figure 1. CNTFET top view

represented by the integer pair (*n, m*). In this paper, the same chirality vector of all CNTs is assumed (i.e. (19, 0)). Fig.1 shows the schematic diagram of a CNTFET [6]. Similar to a traditional silicon device, the CNTFET has also four terminals. A dielectric film is wrapped around a portion of an undoped semiconducting nanotube, and a metal gate surrounds the dielectric. Heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance during the on-state [7]. As the gate potential increases, the device is turned on or off electrostatically via the gate. For high-performance, an area efficient design must be considered and a channel length of 20nm is selected in this paper.

The CNTFET can be configured to be ON or OFF by connecting its gate to V_{dd} or leaving it floating. This configuration can be implemented by using an antifuse technology such as in existing reconfigurable architectures. For example, a layer of amorphous silicon can be sandwiched between two layers of metal. The two layers of metal are initially not connected, unless a large programming voltage is forced through the layer [9]. Therefore, this is a one-time programmable memory. A Reconfigurable Double Gate CNTFET (RDG-CNTFET) introduced in [10] can be used as a switch for a reconfigurable crossbar memory design; the RDG-CNTFET is fabricated by sandwiching electrically bistable molecules in a double gate CNTFET. The electrically bistable molecules are coated around the front gate and sandwiched between the front gate and the source/drain regions. Dielectric and redox active molecules are coated around the back gate and sandwiched between the back gate and the source/drain region. The RDG-CNTFET is reconfigurable to vias or opens by controlling the gate voltage and its fabrication process has been described in [10]. In this paper, we just focus on the CNTFET shown in Fig.1 and the one-time programmable memory.

3. CROSSBAR MEMORIES

A crossbar memory is built by placing a switching element at the intersection of the horizontal and vertical conducting wires (crosspoint). The switch, or the junction of the wires, can have two distinct states: the ON and the OFF states, respectively. Each memory element can be programmed by a sufficiently high voltage pulse on the corresponding word and bit lines. The state of the molecular crossbar memory can be read-out by either detecting the corresponding sense voltage, or the sense current. The small dimension of the molecular switches provides an opportunity to achieve a high density design. The molecular switch used in the molecular crossbar memory can be modeled by

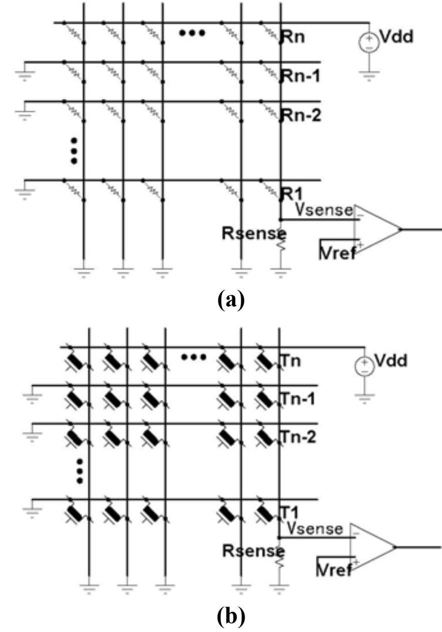

Figure 2. Read-out Scheme I of a) molecular crossbar; b) proposed CNTFET-based crossbar

setting the resistance of the molecular switch to be in the ON or OFF position [4]. The switches are modeled as resistors and set to R_{ON} or R_{OFF}, depending on the state of the crosspoints. In this paper, R_{ON} = 3.5MΩ and R_{OFF} = 23 MΩ are used, as shown in [4].

In a CNTFET-based crossbar memory, all switches and resistors are replaced by CNTFET-based elements. The small dimension of the CNTFET makes it possible to use the device as a switch and as an alternative to the molecular switch. As shown in Fig.1, four tubes are used as channel of the CNTFET, with a channel length L_{ch} = 20nm. The pitch, which is the distance between the centers of two adjacent tubes, is 20nm. The drain to source distance, L_{sd}, is 40nm. Process variations for the CNTs are not considered in this paper (as currently investigated). The metal interconnect of the crossbar is assumed to be 32nm in width, with a unit resistance of 16.526 Ω/um and capacitance of 276.214 aF/um [11]. Both the interconnect parasitic components above and the transistor parasitic components in the model of [6] are included in the HSPICE simulation presented in the next section.

4. READ-OUT SCHEMES FOR THE CROSSBAR

In this section, two read-out schemes are proposed and two figures of merit for these two schemes will be used to investigate their effectiveness for a CNTFET-based crossbar memory.

4.1 Read-out Scheme I

The simple read-out scheme biases the selected junction and measures the current flowing from the junction toward the ground [4]. As shown in Fig.2 (a), all unselected bit and word lines are connected to ground. A resistor, Rsense, is connected to the selected column to detect the current of the column. The voltage drop across the resistor, Vsense, is compared with the reference voltage Vref, to determine the state of a selected bit. Fig. 2(b)

shows this read-out circuitry for the CNTFET-based crossbar memory, while all resistors are replaced by CNTFET-based elements. As analyzed in [4], the sense voltage of the crossbar memory is influenced only by the resistances connected to the same bitline as the interrogated bit. The larger the array size is, the smaller the absolute value of the sense voltage is. Also, the more ON cells in an array, the smaller the sense voltage is. Therefore, materials/switches with high R_{ON}/R_{OFF} ratios are more suitable to construct larger memory arrays.

For an n x n array, the worst case scenario is when the state of Rn in Fig.2 is read and all other bits on the same column are ON. The sense voltage on/off ratio is defined as the sense voltage ratio between the states ON and OFF from the selected bit. When all other bits on the same column are OFF, the sense voltage on/off ratio is very large because the leakage current on the column is very small. However, some other bits are ON, and then the leakage currents will have a significant effect on the current of the selected column for the molecular crossbar. However, for the CNTFET-based crossbar, due to the small off leakage current of the CNTFET, the read-out voltage will not be affected by the leakage current from other bits on the same column.

Initially, HSPICE simulation has been performed on a 100 x 100 array for both crossbar memory configurations. Rsense is set to 100 kΩ and the sense voltages Vsense are shown in Table 1. In Table 1 the voltage level of the molecular crossbar memory at "All cells ON" and "One cell OFF, others ON" are very close (the sense voltage on/off ratio is 2.4) while the difference between the voltage levels for the CNTFET-based crossbar is much larger than for the molecular crossbar (the sense voltage on/off ratio is 430). Fig.3 shows the values of Vsense for a 100 x 100 array at different sense resistor values, assuming the worse case scenario

Table 1. Sense voltage of crossbar memories

Memory type	One cell ON, others OFF (V)	All cells OFF (V)	All cells ON (V)	One cell OFF, others ON (V)
Molecular	0.0176	1.021e-3	6.667e-3	2.727e-3
CNTFET-based	0.4489	0	3.345e-3	7.807e-6

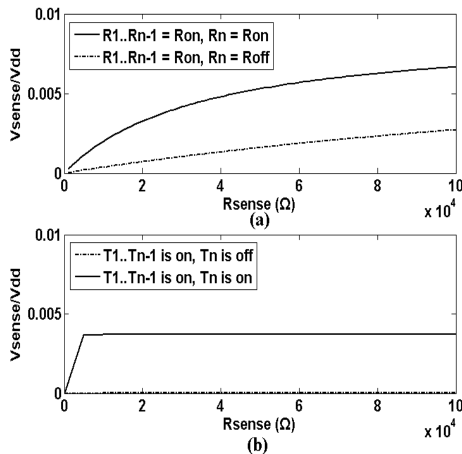

Figure 3. Sense voltage of a) molecular crossbar; b) CNTFET-based crossbar

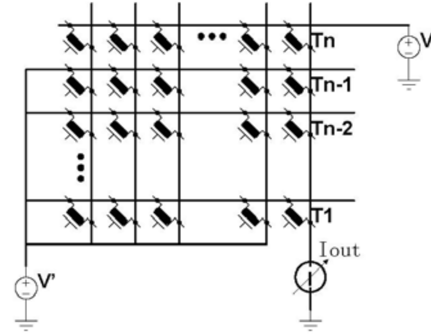

Figure 4. Read-out scheme II of CNTFET-based crossbar

in which all other bits are ON. As shown in Fig.3(a), the voltage difference between ON and OFF states increases as the value of Rsense increases. Therefore, for a larger read-out margin, Rsense needs to be as large as possible. However, for the CNTFET-based crossbar memory, the voltage difference between Tn ON and Tn OFF is large such that no large Rsense is needed. A large sense voltage on/off ratio provides a large read-out margin for the CNTFET- based crossbar memory design.

4.2 Read-out scheme II

Another possible read-out scheme involves biasing all other unselected bits and/or wordlines [4]. Fig. 4 shows the read-out scheme for the proposed CNTFET-based crossbar circuit. All unselected wordlines and bitlines are connected to a biased voltage source V'. An ideal current measurement is assumed at the selected column, i.e., we measure the current on a zero-resistance meter between crossbar array and ground instead of the voltage drop on a sense resistor. For a fair comparison, the same crossbar circuit scheme with molecular switches is used. The only difference is that CNTFETs are replaced with molecular devices.

In general cases, the biased voltage source V' is connected to the ground. The on and off current of the crossbar arrays are shown in Table 2. As the dimension of the crossbar array increases, the on/off current ratio of the crossbar decreases. For the molecular crossbar array, the on/off current ratio is very small at large dimensions, which makes the current sensor design extremely difficult. On the other hand, the CNTFET-based crossbar provides a larger on/off current ratio due to its ultra-low off current, which makes the CNTFET-based crossbar design more promising and realistic solution.

In this read-out scheme, the absolute current difference between the "ON" and "OFF" states of the junction remains constant, but the leakage and parasitic currents increase with array size. For this read-out scheme, a figure of merit (i.e. the relative noise

Table 2. On/off current of crossbar memories

Memory type	On Current	Off Current	On/Off ratio
20x20 Molecular	1 uA	0.82 uA	1.22
100x100 Molecular	4.2 uA	4.0 uA	1.05
20x20 CNTFET-based	23.71 uA	0.578 nA	4.1e+4
100x100 CNTFET-based	23.71 uA	2.78 nA	8.53e+3

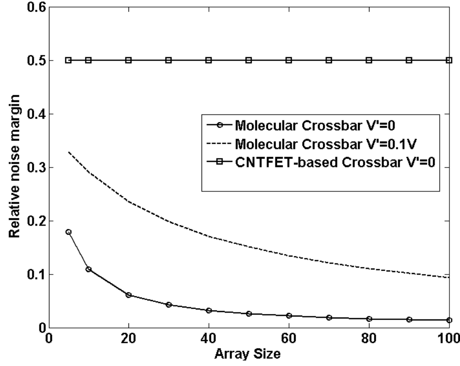

Figure 5. Relative noise margins of crossbars

margin of the sense current) is considered, which is given as:

$$Noise\ Margin = \frac{1}{2}\frac{I_{ON} - I_{OFF}}{I_{ON} + I_{OFF}} \quad (1)$$

Simulation has been performed by HSPICE on the crossbar memory arrays to find the noise margin. For the molecular crossbar memory, when V' = 0, the leakage currents from all accessed devices on the same column flow to ground. The ON and OFF current of the molecular crossbar can be found as follows:

$$I_{ON} = V\left(\frac{1}{R_{ON}} + \frac{n}{R_{OFF}}\right) \quad (2)$$

$$I_{OFF} = V\frac{n+1}{R_{OFF}} \quad (3)$$

where n is the dimension of the array. The larger the array size is, the larger the OFF current is. Therefore, the noise margin of the molecular crossbar is very small when the array size is large. By setting the biased voltage to 0.1V it is possible to improve the noise margin significantly as shown in Fig.5. However, the noise margin is still not large enough when the array size increases. For the CNTFET-based crossbar array, when V' = 0, the ON and OFF currents can be written as:

$$I_{ON} = I_{on} + nI_{off} \quad (4)$$

$$I_{OFF} = (n+1)I_{off} \quad (5)$$

where I_{on} and I_{off} are the ON and OFF currents of an individual CNTFET, n is the dimension of the memory array. Due to the high on/off current ratio of the CNTFET, the noise margin is very high for the CNTFET-based crossbar array. Fig.5 also shows the noise margin of the CNTFET-based crossbar array. As the array size increases, the noise margin of the molecular crossbar decreases significantly. However, for the CNTFET-based crossbar, the noise margin remains at about 0.5 as the array size increases. Fig.5 confirms high noise margin achieved by the CNTFET-based crossbar. The big on/off current ratio of the CNTFET makes the CNTFET-based crossbar a promising candidate for nanoscale ultra-high scale array design.

5. CONCLUSION

This paper has investigated two read-out schemes for a nanoscale crossbar memory based on CNTFET-based technology. The operation of these read-out schemes has been analyzed, simulated, and compared with a molecular crossbar memory. The first scheme biases the selected junction and measures the current flowing from the junction toward the ground. The second read-out scheme proposed in this manuscript involves biasing all other unselected bits and/or wordlines.

Two figures of merit have been used to investigate the effectiveness of the proposed read-out schemes on the CNTFET-based crossbar memory. Simulation results show that the CNTFET-based crossbar achieves a significant improvement in sense voltage on/off ratio and noise margin. Therefore, this paper demonstrates that the CNTFET design is a viable candidate for crossbar memory design in nanoscale.

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