

A Low-offset High-speed Double-tail Dual-rail Dynamic Latched Comparator

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ABSTRACT

This paper presents a new dynamic latched comparator which shows lower input-referred latch offset voltage and higher load drivability than the conventional dynamic latched comparators. With two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage was improved and the complementary version of the output-latch stage, which has bigger output drive current capability at the same area, was implemented. As a result, the circuit shows up to 25% less input-referred latch offset voltage and 44% less sensitivity of the delay versus the input voltage difference ($\text{delay}/\log(\Delta V_{in})$), which is about 17.2ps/decade, than the conventional double-tail latched comparator at approximately the same area and power consumption.

Categories and Subject Descriptors

B.7.0 [Integrated Circuits]: General

General Terms

Performance, Design

Keywords

Clocked Comparator, Dynamic Latched Comparator, Low-offset Low-power High-speed, Voltage Sense Amplifier (SA)

1. INTRODUCTION

Due to fast speed, low power consumption, high input impedance and full-swing output, dynamic latched comparators are very attractive for many applications such as high-speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers. They use positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) in order to convert a small input-voltage difference to a full-scale digital level in a short time. However, an input-referred latch offset voltage, resulting from static mismatches such as threshold

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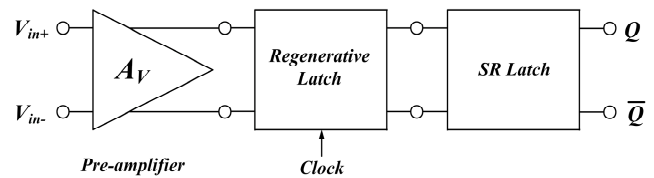


Figure 1 Typical block diagram of a high-speed voltage comparator

voltage V_{th} and μC_{ox} variations in the regenerative latch, deteriorates the accuracy of such comparators. Moreover, dynamic mismatch from the unbalanced parasitic capacitances on the output nodes of the latch causes the additional offset term during evaluation phase [5], [6]. Because of this reason, the input-referred latch offset voltage is one of the most important design parameters of the latched comparator. If large devices are used for the latching stage, a low offset can be achieved at the cost of the reduced speed due to slowing the regeneration time and the increased power dissipation. More practically, the input-referred latch offset voltage can be reduced by using the pre-amplifier preceding the regenerative output latch stage as shown in Figure 1. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage. However, the pre-amplifier based comparators suffer not only from large power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain-to-source resistance r_{ds} due to the continuous technology scaling [7].

In this paper, we present a new dynamic latched comparator which shows lower input-referred latch offset voltage and higher load drivability than the conventional dynamic latched comparators. With two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage was improved and the complementary version of the output-latch stage, which has bigger output drive current capability at the same area, was implemented. As a result, the circuit shows up to 25% less input-referred latch offset voltage and 44% less sensitivity of the delay versus the input voltage difference ($\text{delay}/\log(\Delta V_{in})$), which is about 17.2ps/decade, than the conventional double-tail latched comparator at approximately the same area and power consumption.

The remaining sections of the paper are organized as follows. Section II provides an overview of the previous works about the dynamic latched comparators in terms of their advantages and drawbacks, and section III describes the proposed dynamic latched comparator which is based on the structures from [3], [4].

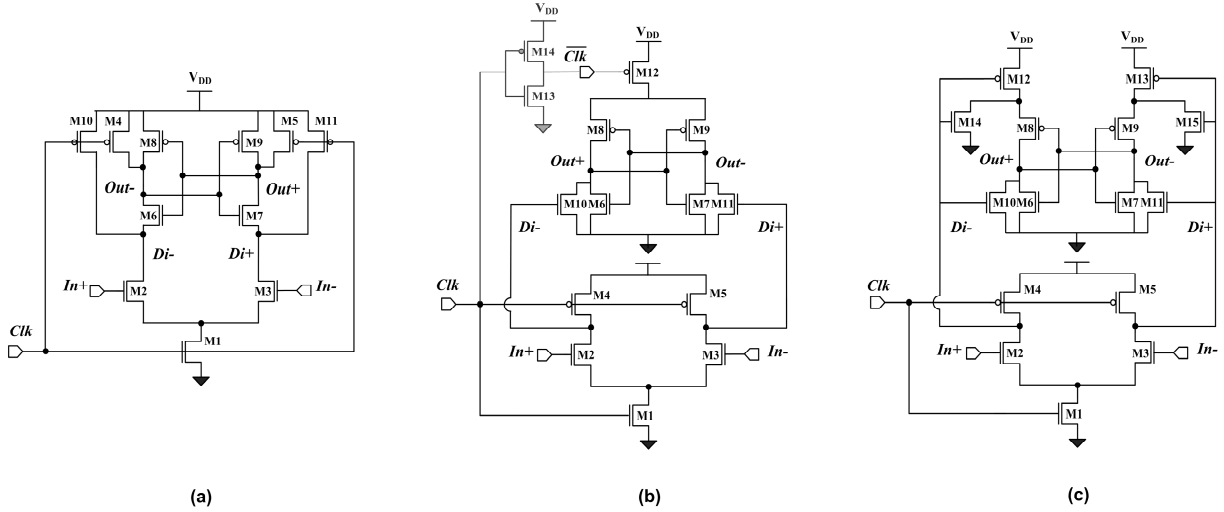


Figure 2 (a) Conventional dynamic latched comparator [1, 2]; (b) Comparator 1 [3]; (c) Comparator 2 [4]

Simulation results from HSPICE using 90nm PTM technology [8] with $V_{DD}=1V$ and their comparisons are presented in Section IV and conclusion is drawn in Section V.

2. PREVIOUS WORKS

With aforementioned advantages such as fast speed, ideally zero static power consumption, high input impedance and full-swing output swing, the dynamic latched comparator shown in Figure 2 (a) has been most widely used [1, 2]. However, in order to increase the drive currents of the latch, it is inevitable to size up the transistor M1 since this comparator has only one tail current transistor M1. If the size of transistor M1 is increased, the drain currents of both input transistors M2 and M3 will increase during the evaluation phase ($clk=V_{DD}$). This, in turn, means the reduction of the time duration for transistor M2 and M3 being operated in saturation region because Di nodes discharge from V_{DD} to ground in a very short period. Consequently, lower amplification of the input voltage difference will be made and such a small V_{th} variation from mismatch between transistor M6 and M7 can yield high input-referred offset. In addition, since it shows the strong dependency on speed and offset with different common-mode input voltage V_{com} [2], it is less attractive in applications with wide common-mode ranges such as ADCs [3].

In order to circumvent these drawbacks, the comparator with separated input-gain stage and output-latch stage shown in Figure 2 (b) was introduced in [3]. This separation made it possible that this comparator can operate at a lower supply voltage (V_{DD}) and have a more stable offset voltage over wide common-mode voltage (V_{com}) ranges. However, since it requires both clk and $clkb$ for its operation, high accuracy timing of $clkb$ is required because the output-latch has to detect the voltage difference at Di nodes at very limited time. If a simple inverter replaces the $clkb$, clk has to be able to drive an additional large inverter (heavier clock load) in order to drive the largest transistor M12 in a small delay. If $clkb$ is lagging the clk , it results in increased delay and if $clkb$ is leading the clk , it results in increased power dissipation due to existing the short circuit current path M12 to M10/M11 though M8/M9 and it can even increase the latch offset voltage if the device mismatch between M8 and M9 is significant.

The comparator from [4] without offset calibration technique, shown in Figure 2 (c), resolved the problem by replacing $clkb$ with Di nodes. As a result, clk load was lessened and the input-referred offset was reduced. However, the improved offset has to trade off with the increased delay since the current drivability of the output load was weakened due to the fact that transistor M12 and M13 use Di node voltages as their $clkb$ signal, which show slow exponential decay shape, and that the maximum drive current of each Out node was reduced to half of the single output tail current of M12 comparing with Comparator 1 since it was separated into two transistors M12 and M13.

3. PROPOSED COMPARATOR

The schematic and simulated waveforms of the proposed comparator are shown in Figure 3. The simulated waveforms were obtained from HSPICE using 90nm PTM technology [8] and the operating conditions were $V_{DD}=1V$, $f_{clk}=3GHz$, $C_{load}=7fF$, $Temp.=25^{\circ}C$, and $V_{com}=0.7V$. The basic structure of this comparator stems from Comparator 1 and 2 shown in Figure 2 (b) and (c). Therefore, while maintaining the existing advantages from the both of the comparators such as fast operation over a wide common-mode and supply voltage range with improved offset, less kickback noise and reduced clock load or timing requirement over conventional dynamic latched comparator, the proposed comparator shows better offset characteristic and faster operation.

Two additional inverters M18/M16 and M19/M17 are inserted between the input- and output-stage in order to amplify or regenerate weakened Di nodes signal of the proposed comparator while the structure of the input-gain stage remains the same as the previous works. In addition to the amplification, they make it possible to use a complementary version of the output-latch stage of the previous ones. Therefore, the positive (regenerative) feedback based on PMOS transistors M8 and M9 was replaced with the NMOS transistors M6 and M7, which increases the output drive current at the same area since the drive current of a NMOS transistor is larger than that of the PMOS transistor at the same width.

For its operation, during the pre-charge (or reset) phase ($clk=0V$), both PMOS transistors M4 and M5 turn on and they charge Di

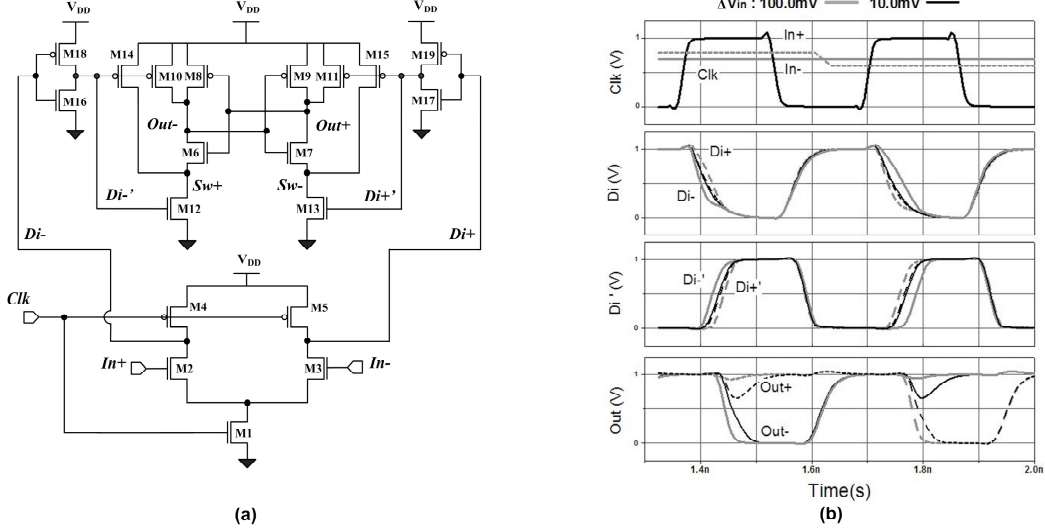


Figure 3 (a) Schematic of proposed comparator; (b) Signal behavior of proposed comparator ($\Delta V_{in}=100\text{mV}$ (Grey), 10mV (Black) with $V_{DD}=1\text{V}$, $f_{clk}=3\text{GHz}$, $C_{load}=7\text{fF}$, $\text{Temp.}=25^\circ\text{C}$ and $V_{com}=0.7\text{V}$)

nodes capacitance to V_{DD} , which in turn make both NMOS transistors M16 and M17 of the inverters on and therefore Di' nodes discharge to ground. Sequentially, PMOS transistors of M10, M11, M14 and M15 turn on and charge Out nodes and Sw nodes to V_{DD} while both NMOS transistors M12 and M13 are off.

During evaluation (decision-making) phase ($clk=V_{DD}$), each Di node capacitance is discharging from V_{DD} to ground in a different rate proportional to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between $Di+$ and $Di-$ nodes. Once either of Di node voltages drops down below around $V_{DD}-|V_{tp}|$, the additional inverter pairs M18/M16 and M19/M17 invert each Di node signal into the regenerated (amplified) Di' node signal. Then the regenerated and different phased Di' node voltages are relayed to the output-latch stage by M10 and M11. As the regenerated each Di' node voltage is rising from 0V to V_{DD} with a different time interval (or a phase difference which increases with the increasing input voltage difference ΔV_{in}), M12 and M13 turn on one after another and the output latch starts to regenerate the small voltage difference transmitted from Di' nodes into a full-scale digital level: $Out+$ node will output logic high (V_{DD}) if the voltage difference at Di' nodes $\Delta Di'(t)$ is negative ($Di+'(t) < Di-'(t)$) and output logic low (0V) in the case it is positive. Once either of Out node voltages drops below around $V_{DD}-|V_{tp}|$, this positive feedback becomes stronger because either PMOS transistor M8 or M9 will turn on. M14 and M15 are used to reset Sw nodes to V_{DD} in order to avoid the voltage mismatch between Sw nodes during pre-charge phase.

In summary, the two additional inverters inserted between Di and Di' nodes have enabled the proposed comparator to have both less input-referred latch offset voltage by amplifying (regenerating) weakened Di node signals to Di' node signals with the time differences and a complementary version of the output-latch stage which can drive higher load current.

4. COMPARISON WITH PREVIOUS WORKS

To compare the performances of Comparator 1, 2 and the

proposed one, each circuit was designed using 90nm PTM technology with $V_{DD}=1\text{V}$ and simulated with HSPICE. The operating conditions were the same as the previous part ($V_{DD}=1\text{V}$, $f_{clk}=3\text{GHz}$, $C_{load}=7\text{fF}$, $\text{Temp.}=25^\circ\text{C}$ and $V_{com}=0.7\text{V}$). In order to compare their relative speeds and input-referred latch offset voltages, each circuit was designed to have the same C_{Di}/I_1 (Di nodes capacitance/drain current of M1) ratio at the same area. In addition, transconductance of M2 and M3 of each comparator was kept constant by sizing the widths of M2 and M3 to have $1.2\mu\text{m}$. After setting the widths of the mismatch critical transistors to have relatively large size ($>1\mu\text{m}$), the rest sizes of transistors are optimized for high speed, low offset and less power consumption.

Figure 4 shows the simulated delay (ps) of each Comparator versus input voltage difference (V) with different load capacitance of 7fF and 10fF. The absolute delay was measured between the 30% of the rising clk edge to 70% of the rising output edge for the comparator 1 and 2 and to 30% of the falling output edge for the proposed comparator. Even with the additional inverter delays formed from transistor M16-19, the proposed comparator outputs faster decision over the comparator 1 when

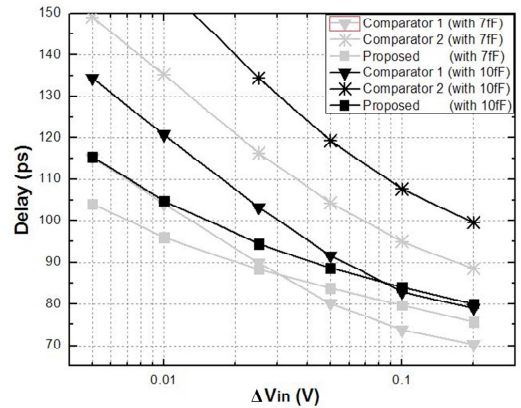


Figure 4 Simulated delay (ps) versus $\Delta V_{in}=|V_{in+}-V_{in-}|$ (V) with different load capacitances of 7fF and 10fF ($V_{DD}=1\text{V}$).

TABLE I PERFORMANCE COMPARISON

	Number of Transistors	Σ Width(μm)	[Delay(ps)/log(ΔV_{in})]	Resulting V_{os} (with $\Delta V_{th}=30\text{mV}$)	Energy/Decision	Setup + Hold time
Comparator 1 [3]	14	13.65 μm	$\sim 39.3\text{ps/decade}$	14.2mV	45.258fJ	18ps [3]
Comparator 2 [4]	15	13.68 μm	$\sim 39.7\text{ps/decade}$	4.5mV	36.555fJ	-
Proposed Comparator	19	13.56 μm	$\sim 17.2\text{ps/decade}$	3.4mV	37.597fJ	-

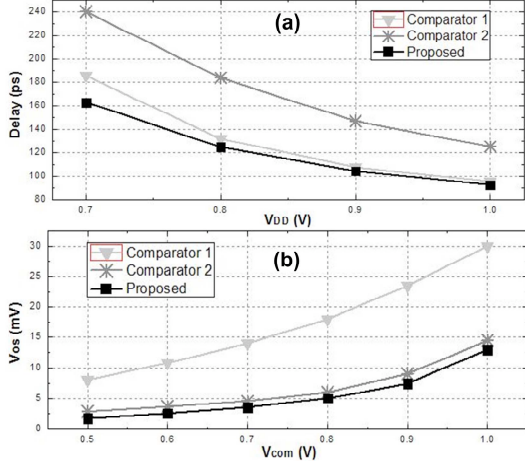


Figure 5 (a) Simulated delays (ps) with different V_{DD} ($\Delta V_{in}=20\text{mV}$, $V_{com}=V_{DD}-0.1\text{V}$ and $C_{load}=7\text{fF}$) (b) Simulated V_{OS} with different V_{com} under intentional V_{th} mismatch (30mV) condition ($V_{DD}=1\text{V}$ and $C_{load}=7\text{fF}$).

the ΔV_{in} is less than around 30mV with 7fF capacitance load and less than around 90mV with 10fF capacitance load since the delay of the proposed comparator is less sensitive to the reduction of ΔV_{in} which is around 17.2ps/decade. As the size of the load gets larger, the proposed comparator shows better overall speed over the comparator 1 since the proposed comparator can drive more current than the comparator 1 and 2 with the same area. As shown in Figure 5 (a), with lowering supply voltage (V_{DD}), the delay of the proposed comparator increases slower than that of comparator 1 and comparator 2.

In order to compare the relative input-referred latch offset voltage of each comparator, the intentional threshold voltage (V_{th}) mismatch of 30mV was added to the mismatch critical PMOS regenerative pair (M8 and M9) of the comparator 1 and 2 and NMOS regenerative pair (M6 and M7) of proposed one while all other conditions are kept constant. The sixth column in Table I shows the resulting input-referred latch offset voltage (V_{OS}) with 7fF capacitance load, $V_{com}=0.7\text{V}$ and $V_{DD}=1\text{V}$. The simulated result shows that the resulting V_{OS} of the proposed one is 3.2mV which is less than 4.7mV of the comparator 2 and even much less than 14.3mV of the comparator 1. In addition, Figure 5 (b) shows the simulated V_{OS} dependencies on each comparator with different V_{com} . With increase of V_{com} from 0.5V to $V_{DD}=1\text{V}$, the V_{OS} of the proposed comparator and the comparator 2 increases only around 10mV while the comparator 1 increases around 23mV.

The performance of each comparator is summarized in Table I. The second and third columns show the number of transistors and total channel widths of the transistors, which can be considered as approximate measures of circuit complexity and chip area. The fourth column is the delays (ps) per the input voltage differences (log(ΔV_{in}) or decade) of each comparator. The sixth and last column in Table I shows that the proposed comparator consumes even less power than the comparator 1 without setup and hold time while presenting more stable delay/log(ΔV_{in}) and even less input-referred latch offset voltage at the same area.

5. CONCLUSION

In this paper, we presents a new dynamic latched comparator which has low input-referred latch offset voltage and high output load drivability over the conventional double-tail dynamic latched comparator. It shows up to 25% less input-referred latch offset voltage and 44% less sensitivity of the delay versus the input voltage difference (delay/log(ΔV_{in})), which is about 17.2ps/decade, than the conventional double-tail latched comparator at approximately the same area and power consumption.

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