

Performance Assessment of Analog Circuits with Carbon Nanotube FET (CNFET)

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ABSTRACT

Carbon Nanotube FET technology is a new promising technology for high speed digital applications. This paper investigates optimizing analog circuits architecture to take advantage of this technology in mixed mode ICs. It was found through simulations that the optimum topology for high-bandwidth analog circuits is obtained by using an architecture which avoids loading by the high CNFET gate capacitance in the main signal path at high impedance points. Low junction capacitances of CNFET and high transconductance (g_m) compared to silicon MOSFET indicates that high gain-bandwidth can be obtained by using CNFET. Simulations indicate low voltage operation (0.5 V) is possible using CNFET technology and also high temperature operation (> 200 C) is possible. Monte-Carlo simulations indicate that device matching of important CNFET parameters such as nanotube diameter, channel length, source/drain doping are important to get consistent results.

Categories and Subject Descriptors

B.7.1 [Types and Design Styles]: Advanced technologies, Algorithms implemented in hardware, Gate arrays, Input/output circuits, Memory technologies Microprocessors and microcomputers, Standard cells, VLSI (very large scale integration)

General Terms

Measurement, Documentation, Performance, Design, Economics, Reliability, Experimentation, Standardization, Theory, Verification.

Keywords

Analog, Circuits, Carbon Nanotube, FET, Differential-Amplifier, CNFET, Low Power, High Speed, High Performance.

1. INTRODUCTION

As predicted by Moore's law, CMOS manufacturing technology has continued to scale to ever-smaller dimensions now reaching 32 nm [1]. At these dimensions several issues such as source to drain tunneling, device mismatch, random dopant fluctuations, mobility degradation, etc. that impact its cost, reliability and performance making further scaling almost impossible. Carbon

nanotube field-effect transistor (CNFET) is a promising technology that may allow for shrinking process to continue [2-3]. CNFET is similar to a conventional MOSFET except that its semiconducting channel is made up of carbon nanotubes (CNT) as shown in Fig. 1.

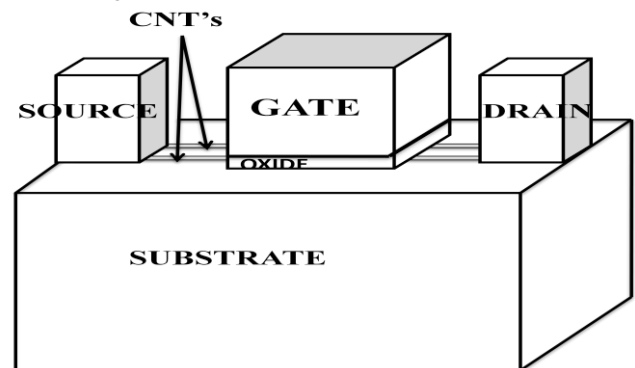


Fig. 1: Carbon NANOFET with multiple nanotubes.

Most attractive feature of CNTs is their near ballistic transport due to a limited carrier-phonon interaction because of larger mean free paths of acoustic phonons [4-5]. CNFET shows higher electron mobility of the order of 10^4 – 10^5 cm^2/Vs compared with 10^3 cm^2/Vs for bulk silicon and higher current densities, roughly three orders of magnitude greater than that reported for silicon nanowire. Analog devices require linearity, and it has been demonstrated that CNFETs have the potential to provide linearity well beyond what is possible with silicon or III-V semiconductors [6].

The differential amplifier is the basic building block in analog circuits. This paper provides the simulation and analysis of carbon nanotube FETs in differential amp/opamp circuits to point at the optimum topology when CNFETs are used with special emphasis on low-power applications. Some of the components of analog/rf systems were published [6-10], but to our knowledge this is the first attempt at optimization of CNFET opamp circuit topology based on process parameter variations.

2. CNFET DIFFERENTIAL AMPLIFIER DESIGN

The commonly used CMOS Differential Amplifier (Fig. 2) at 32 nm was optimized for area, power and performance and then extended it to the CNFET design with similar geometry as CMOS. The initial design parameters of CNFET topology was set to their most practical values and then optimized. It was found that the gain of the topology using CNFET was higher than that of CMOS which can be expected due to higher transconductance and output impedance, but the bandwidth of CNFET was lower.

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Analytical results show that with diameter increase, all circuit performance parameters suffer with the exception of some improvement in bandwidth and transient performance. Diameter D_{CNT} is the main parameter that affects the on-current proportionally (and hence transconductance) in a CNFET apart from barrier height at the S/D contact (E_{f0}), chirality (n_1, n_2) and oxide thickness, due to which Gain and CMRR changes. The change is appreciable when random values are used for different transistors in the topology simulated using Monte-Carlo simulations. The power consumption of the amplifier increases due to smaller band gap as CNTs become more conducting thereby, enhancing the current drive. Bandwidth improves with an increase in diameter due to smaller effective pitch which strongly affects the outer fringe and C_{gc} capacitances. It is primarily due to enhanced screening between adjacent channels. We conclude that Differential Amplifier could be designed for low power-low bandwidth and high power-high bandwidth applications on the basis of the selection of diameter.

3. CNFET SIMULATION RESULTS

CNFET differential amplifier (Fig. 3) was found to operate at supply voltages as low as 0.5V with very low total DC current consumption (5uA) and low power (2.5uW) making it an attractive technology for low power/micro-power analog circuits. Variation of characteristics with supply voltage variation is shown in Fig. 4. For each supply voltage, the design parameters can be adjusted to get the optimized gain, bandwidth, power trade-off. Keeping the supply voltage at 0.75 V, the differential amplifier was functional with a common-mode voltage in the range of 0.15 V to 0.45 V.

Gain (dB) and BW (MHz) vs Supply Voltage

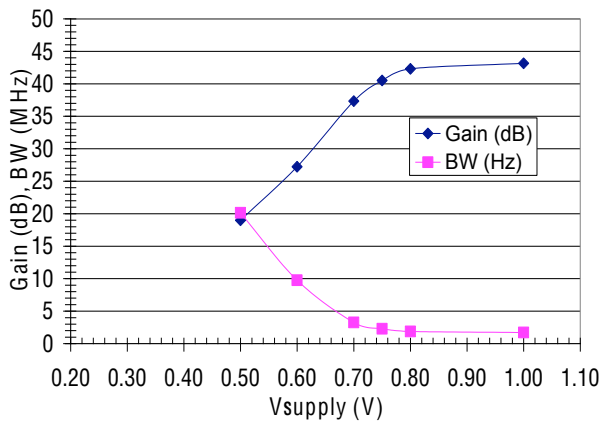


Fig. 4: Variation of Gain and Bandwidth with Supply Voltage.

CNFET differential amplifier has been simulated to work well at high temperatures as high as 200 C as shown in Fig 5. This is because of reduced scattering of carriers in CNFET compared to silicon where the scattering is increased with temperature.

Monte-Carlo simulations of CNFET topology was done to look at the effects of process variations (Fig. 6). With random variation between transistors, the circuit parameters was found to be highly dependent on the nanotube diameter, channel length and source/drain doping.

Gain (dB), BW (MHz) vs Temperature

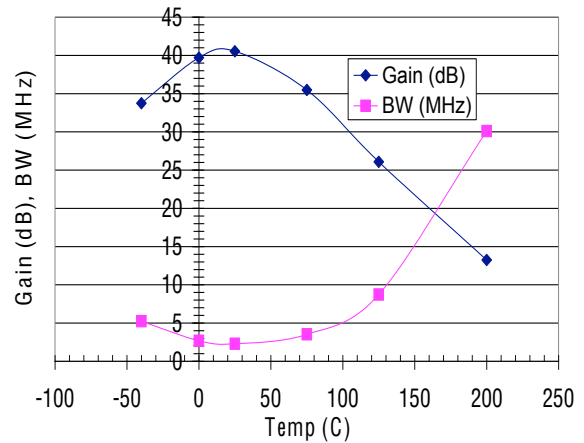


Fig. 5: Variation of Gain and Bandwidth with Temperature for a Supply Voltage of 0.75V.

The Monte-Carlo simulations indicate that matching techniques should be used in CNFETs similar to CMOS such as common centroid geometry, dummy devices at the ends etc. The median parameter values are gain of 40 dB, bandwidth of 1 MHz, unity gain frequency of 25 MHz, PSRR of -160 dB for differential output and -60 dB for common-mode output, output impedance of 47 Mega-ohm, output noise of 900nV/sqrt(Hz) (Fig. 7). These circuit parameters can be expected to get better as the technology parameters improve.

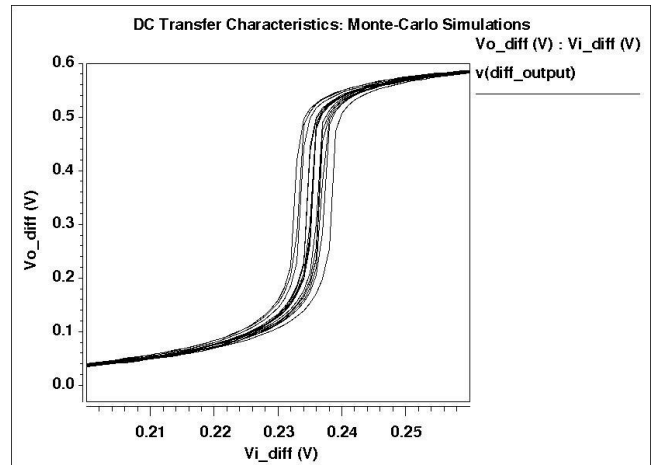


Fig. 6: Monte-Carlo Simulation with random variation of parameters to obtain DC Transfer characteristics (Output Differential Voltage vs Input Differential Voltage).

Among the device parameters, the nanotube diameter had the biggest influence for random variations between transistors. However, when the parameters were varied identically for different transistors in our topology, there was minimal variation in circuit parameters indicating that CNFET technology is feasible for producing analog circuits when layout matching techniques are employed and the process variations are reduced. The change of gain and BW with nanotube diameter when it is varied identically for different transistors is shown in Fig. 8.

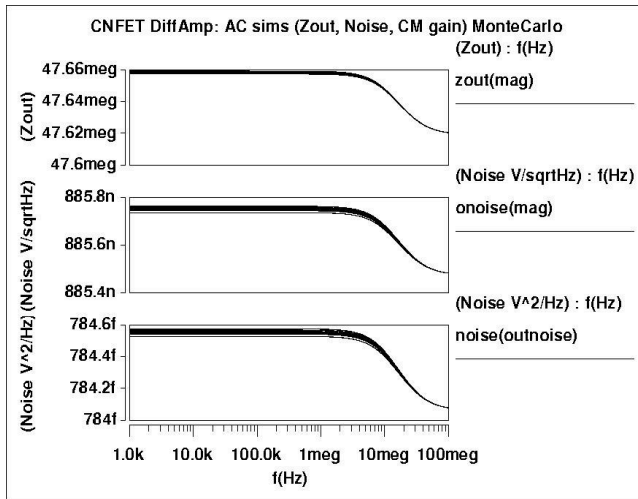


Fig. 7: Monte-Carlo Simulation with random variation of parameters to obtain Output Impedance and Noise variation.

It was seen from Fig. 8 that if high bandwidth is desired, the carbon nanotube diameter should be small (~1 nm) while making necessary trade-offs in gain and power. For high gain in the range of 40 dB, the diameter should be in the range of 1.5 nm while achieving low power (2.5-5 μ W) at the expense of bandwidth (~2 MHz). Increase in diameter leads to decrease in band-gap energy and threshold voltage. By carefully choosing the diameter for a particular application optimum trade-off between gain, bandwidth and power can be achieved. In deciding the broad range of possible applications.

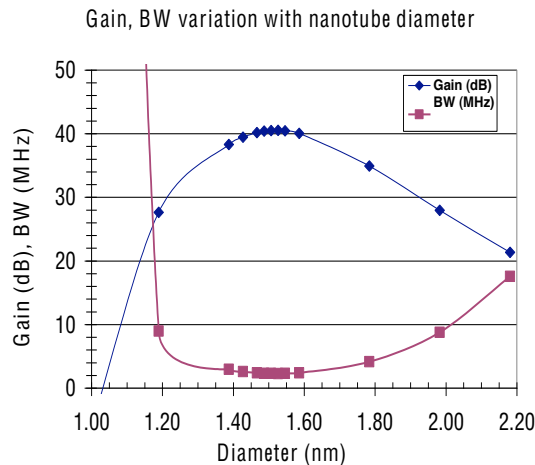


Fig. 8: Variation of Gain and BW with uniform variation of carbon nanotube diameter for all CNFET in the circuit.

4. CONCLUSIONS

This work explores basic building block of analog circuits, the differential amplifier using newly emerging CNFET technology. An advantage found for CNFETs is that it can be operated with supply voltages lower than 0.5 V leading to lower power dissipation and compatibility to digital logic supply voltages. Another advantage found for CNFETs was good high temperature operation. Circuit characterization was also performed using variations of process conditions. The carbon nanotube diameter

plays an important role and has to be optimized for each application requirements.

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