

# A Highly-Stable Nanometer Memory for Low-Power Design

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## Abstract

A nine transistor (9T) cell at a 32nm feature size in CMOS is proposed to accomplish improvements in stability as well as power dissipation compared with previous designs for low-power memory operation. Initially, this paper shows that the proposed 9T SRAM cell can be used for robust, high-density design. Then, an optimum sizing is found for this 9T cell by considering stability, energy consumption, and performance. A write bitline balancing scheme is proposed to further reduce the power consumption of the SRAM cell. The impact of process variations is investigated in detail, and the power reduction of the 9T SRAM cell is verified under parameter variations.

## 1. Introduction

As the era of nanoscale devices is becoming a reality, many features of such small devices (inclusive of performance) are starting to deteriorate: leakage has increased, gain has decreased, and sensitivity to unavoidable small fluctuations in the manufacturing process has dramatically risen. Power and energy have become the key limitations on many new designs. With the advent of microprocessors and systems on chips (SoCs), the design of power efficient SRAM structures has become highly desirable. One of the most effective approaches to meet this objective is to design SRAM cells whose operation is ultra-low power. A decrease in supply voltage reduces quadratically the dynamic power and linearly to the first order leakage power. However, with an aggressive scaling in technology, substantial problems have already been encountered when the conventional six transistors (6T) SRAM cell configuration is utilized at an ultra-low power supply; this cell shows poor stability at very small feature sizes. Moreover, the read static noise margin is small for robust operation at a feature size of 32nm. SRAM cell configurations with more than 6 transistors to reduce leakage power and improve stability have been proposed in [1] [2]. An 8T cell can be found in [1]; this

cell employs two more transistors to access the read bitline. Two additional transistors (thus yielding a 10T cell design) are employed in [2] to reduce the leakage current. A 9T SRAM cell is proposed in [3] with further leakage power and area reductions.

In this paper, transistor sizing of the 9T SRAM cell for high data stability and good write-ability is first investigated. Then, an innovative precharging and bitline balancing scheme for the write operation in the 9T SRAM cell is also proposed for maximum static power saving in an SRAM array. Finally, the impact of process, voltage, and temperature (PVT) variations on the cell's power delay product is analyzed to show that the 9T SRAM cell achieves significant power reduction in the presence of PVT variations.

## 2. Optimal sizing for 9T SRAM cell

### 2.1. Proposed 9T SRAM cell

In the conventional 6T SRAM cell, the stored data is disturbed by the voltage separation between the cross-coupled inverters and the access transistors during a read operation, thus causing a low read Static Noise Margin (SNM). A 9T structure has been proposed in [3] to improve the SNM by separating the read access structures of the original 6T cell, thus making the read SNM equal to the hold SNM. Fig. 1 shows the proposed 9T SRAM cell. Similarly to the 8T cell of [1], the configurations from MN1 to MN4 and from MP5 to MP6 are unchanged (same as the one in the 6T SRAM cell). The read SNM margin is

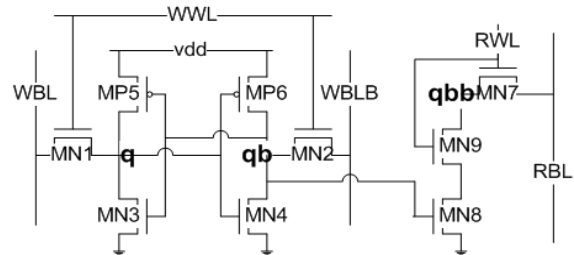
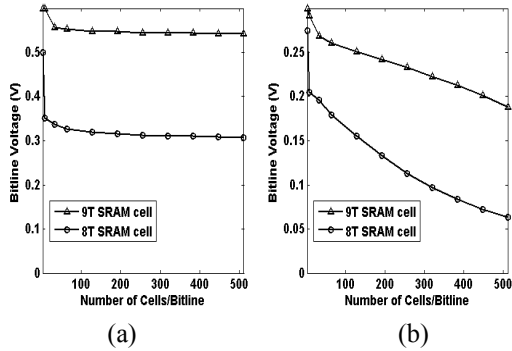


Figure 1. 9T SRAM cell in [3]



**Figure 2. Bitline voltage of 8T and 9T cell arrays with a) power supply voltage = 0.6V; b) power supply voltage = 0.3V**

maintained by retaining the write access circuit and adding a read buffer to the conventional 6T configuration. For the 8T cell in [1], the bitline leakage problem has been observed on the read bitline; this may cause a data correctness problem during a read operation, i.e. the bitline must be kept high but it may drop to a low level due to a bitline leakage for the other unaccessed cells. This problem limits the 8T cell to high-density applications. In the 9T cell, by adding a NMOS transistor (MN9) between MN7 and MN8, the bitline leakage is significantly reduced by the so-called stack effect. The reduced bitline leakage makes it possible to have more SRAM cells on a bitline that can be implemented in high-density SRAM designs. Fig. 2 shows the worst case bitline voltage of the 9T and 8T cells at different power supply voltages. Simulation results have shown that by employing the proposed 9T cell in a 512-row cell array, the voltage drop at the read bitline due to the leakage current is still sufficiently small to retain data correctness on the bitline, i.e. it is above the flip point of the output buffer (about half of the value of the supply voltage).

## 2.2. Data stability and write-ability

### 2.2.1. Static noise margin and write-ability.

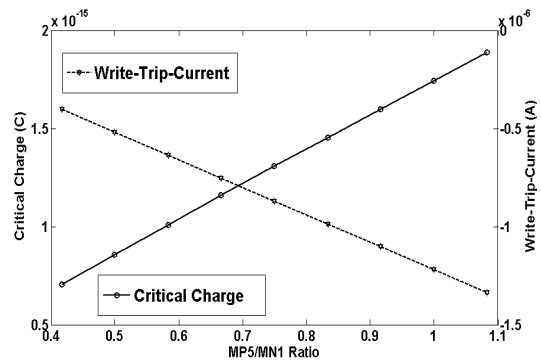
Robustness imposes a sizing constraint to the 6T SRAM cell, i.e. the pull down to the pass gate transistor ratio must be greater than 1.2 to avoid the read-upset problem [4]. However, in the 9T SRAM cell the read and write operation is separated so the transistor ratio between MN3 and MN1 can be decreased. The SNM measured by the opening in the butterfly plot is usually used as metric for SRAM stability [5]. Alternatively, the N-curve of the SRAM cell that generates statistical information can be used to define the stability [6]; the N-curve can be extracted by reading the input current at the internal storage node when sweeping the storage node voltage from 0V to

**Table 1. Noise Margin Comparison**

| SRAM cell                   | SNM   | SVNM  | SINM    |
|-----------------------------|-------|-------|---------|
| 6T SRAM cell (MN3/MN1=1.33) | 80mV  | 180mV | 25.40uA |
| 9T SRAM cell (MN3/MN1=1.00) | 270mV | 260mV | 26.68uA |

$V_{dd}$ . Two metrics for the SRAM cell static noise margin, the static voltage noise margin (SVNM) and the static current noise margin (SINM), can be found on the N-curve [6]. Table 1 shows the noise margin comparison between a 6T SRAM cell with MN3/MN1=1.33 and a 9T SRAM cell with MN3/MN1=1 measured at a supply voltage of 0.6V. Therefore, a MN3 to MN1 ratio of 1 is selected for highly stable 9T SRAM cell.

The SRAM N-curve can also be used as an alternative for assessing the write-ability of the cell, because it provides a measure for the write operation [6]. The write-trip current (WTI) specifies the amount of current required for writing. This is the current margin of the cell when its content changes. The smaller the absolute value of WTI is, the easier to write the SRAM cell. Fig. 3 shows that the absolute value of WTI decreases as the pull up transistor MP5 decreases, i.e. it is easier to write a “0” into the SRAM cell with smaller pull up transistors. A good write-ability of the SRAM cell ensures the write drivers and access transistors to overpower the load inside the cell. To increase the write-ability, the pull up transistors should be sized as small as possible. However, a good write-ability means that the data-holding ability of the SRAM cell degrades (possibly leading to soft errors), and this may make SRAM cells rather unstable at a low power supply. Therefore, the dynamic stability analysis described in the following section is used to find the optimum pull up transistor sizing for both good write-ability and resilience to soft errors.



**Figure 3. Write-trip current and critical charge of the 9T SRAM cell**

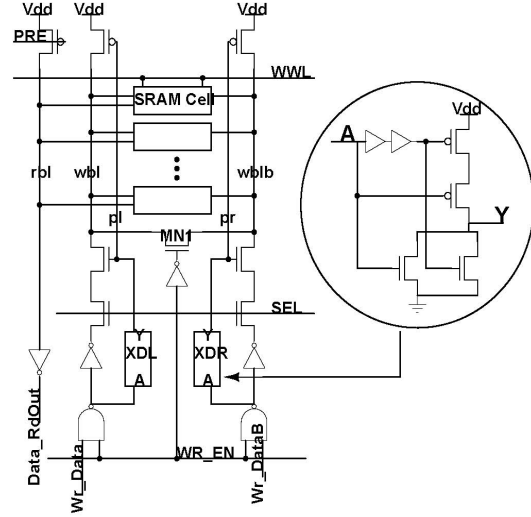
**2.3.2. Dynamic stability.** The robustness of SRAMs against soft errors can be assessed by considering its critical charge,  $Q_{crit}$  [7].  $Q_{crit}$  is the minimum charge that needs to be deposited at the sensitive node of an SRAM cell to flip the stored bit. It exhibits an exponential relationship with the soft error rate. Therefore,  $Q_{crit}$  should be as high as possible to limit the soft error rate.

To determine the critical charge for a SRAM cell, a current generator is applied by HSPICE to the storage node of the SRAM cell (“q” and “qb” in Fig. 1) as equivalent to transient noise when the cell is holding data. Since the pull up PMOS transistor MP5 is significantly weaker than the driver NMOS MN3 due to a lower W/L ratio and mobility, the node storing a “1” is weaker and hence more susceptible to soft errors than the node storing a “0”. Therefore, a current generator is applied to the node storing a “1” to determine the critical charge  $Q_{crit}$ . The minimum total charge  $Q_{crit}$  can be found by finding the integrated current applied to the node storing a “1” to flip the cell. Fig. 3 shows the critical charge of the 9T SRAM cell with different MP5/MN1 ratio. The SRAM cell tolerance to soft errors is enhanced by increasing the pull up transistor size. It is important to find an optimum pull up transistor size due to the conflicting constraint between write-ability and dynamic stability of the cell. Fig. 3 shows that a MP5/MN1 ratio of around 0.7 keeps a relatively high critical charge as well as a low absolute value of WTL.

Therefore, for the proposed 9T SRAM cell at 32nm feature size described previously, the transistor size ratios of the pull up PMOS, the pull down NMOS, and the access transistor have been found for low-power, best static and dynamic stability, and write-ability; in this case, power, stability, and performance of the proposed 9T SRAM cell are optimized when MP5/MN1 = 0.67 and MN3/MN1 = 1.00.

### 3. Write bitline balancing circuitry for standby power reduction

In a conventional 6T SRAM design, both bitlines must be restored to  $V_{dd}$  following a write operation to ensure a successful read operation. The write amplifier circuitry in [4] ensures that the selected bitline is back to a “high” value by generating a negative pulse to precharge the selected bitline high after driving the bitline low to write “0” into the SRAM cell. Therefore, both bitlines (WBL and WBLB in Fig. 1) will be restored to a “high” state after a write operation. When the SRAM cell stores a “0”, the voltage difference between the drain and source of MN1 is  $V_{dd}$ , i.e. a large subthreshold current from WBL to ground will be present when the SRAM cell is in a standby mode.



**Figure 4. Proposed write bit line balancing circuitry**

A novel write bitline balancing circuitry is shown in Fig. 4 to reduce the subthreshold current from WBL to ground. When the WR\_EN signal is enabled, the NMOS transistor MN1 is turned off, and a negative pulse is generated to precharge the bitline that is going to be in the “high” state for a fast write. After the write operation, the WR\_EN signal is removed from the column and MN1 is turned on to balance the voltage at both bitlines to half the value of  $V_{dd}$ . Therefore, the sub-threshold current from WBL to ground decreases exponentially due to the reduced  $V_{ds}$  of the access transistor. Furthermore, for the write amplifier circuitry in [4], the bitline voltage drops in the standby mode due to the leakage of the SRAM cell and will increase the write delay. By employing the proposed write circuitry, the bitline leakage problem can be eliminated.

A 1x128 SRAM cell array operating at a power supply voltage of 0.6V is used to compare the power dissipation on 6T, 8T in [1] and 9T cell arrays in standby mode. As shown in table 2, the 9T SRAM achieves a significant power reduction compared with 6T and 8T designs, at three different process corners.

### 4. Impact of parameter variations

PVT variations are posing a major challenge to

**Table 2. Power dissipation comparison**

| SRAM cell          | <i>SS Corner</i> | <i>TT Corner</i> | <i>FF Corner</i> |
|--------------------|------------------|------------------|------------------|
| 6T SRAM cell array | 220.54nW         | 832nW            | 3.92uW           |
| 8T SRAM cell array | 318.72nW         | 946nW            | 4.05uW           |
| 9T SRAM cell array | 176.26nW         | 547nW            | 2.81uW           |

nanoscale integrated circuits design. Fig. 5 shows the static power and write delay product of the 9T SRAM cell using the write circuitry in Fig. 4 and a conventional 6T SRAM cell design in [4]. Simulation results show that the 9T SRAM cell has a reduced power delay product as well as smaller sensitivity due to power and temperature variations. Meanwhile, technology scaling beyond 90nm is causing higher values in device parameter variations. A Monte Carlo analysis has also been performed to a 1x128 SRAM cell array to examine the impact of geometric variation on the power delay product of the individual SRAM cell. The arithmetic mean of the power delay product of the 9T SRAM cell and the 6T SRAM cell have been found to be  $2.95e-19$  J and  $4.44e-19$  J, respectively. Fig. 6 shows the distribution of the power delay product with transistor geometry variations. All power delay product results are normalized to the arithmetic mean of the power delay product of the 9T SRAM cell. Fig. 6 shows that the power delay product of a 9T SRAM cell is lower than a 6T SRAM cell even when process variations are taken into consideration. As shown in Fig. 6, the power delay product variance of the 9T SRAM cell is also lower compared to that of the 6T SRAM cell. The scheme to lower the bitline voltage

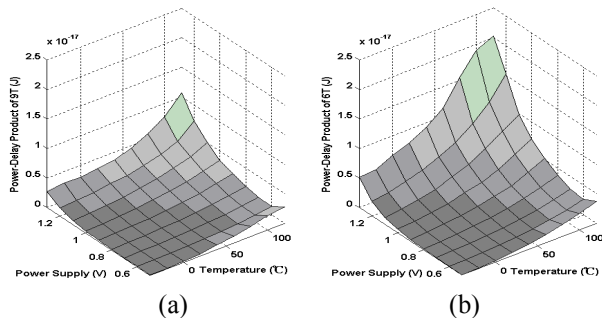
during standby mode mitigates the impact of process variations on power consumption.

## 5. Conclusion

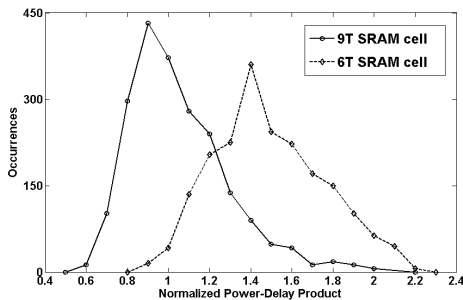
This paper has presented a new design method for the optimal sizing of a 9T SRAM cell by examining the N-curve and dynamic stability of the SRAM cell. Along with transistor sizing scaling, an innovative bitline balancing scheme has been proposed to reduce the leakage current. Simulation results have shown that this write scheme for a 9T SRAM cell-based array achieves a substantial reduction in power consumption at a typical process corner compared with a conventional 6T SRAM cell based array; it has also been shown that this cell is very stable and therefore resilient to soft errors. The impact of parameter variations on the power delay product has been analyzed; also in this case, simulation results show that the 9T SRAM cell offers superior performance in the presence of PVT variations.

## References

- [1] L.Chang et al., "Stable SRAM Cell Design for the 32 nm Node and Beyond", *VLSI Technology, 2005 Symposium on*, June 2005, pp. 128-129.
- [2] B.H. Calhoun and A.P. Chandrakasan, "A 256-kb 65-nm Sub-threshold SRAM Design for Ultra-Low-Voltage Operation", *Solid-State Circuits, IEEE Journal of, Volume 42, Issue 3*, March 2007, pp. 680-688.
- [3] S. Lin, Y-B. Kim, F. Lombardi, "A Low Leakage 9T SRAM Cell for Ultra-Low Power Operation", *ACM Great Lakes Symposium on VLSI 2008*, May 2008, pp. 123-126.
- [4] A. Chandrakasan, W.J. Bowhill, F. Fox, "Design of High-Performance Microprocessor Circuits", IEEE Press, 2000.
- [5] E. Seevinck, F.J. List, J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells", *Solid-State Circuits, IEEE Journal of Volume 22, Issue 5*, Oct 1987, pp. 748-754.
- [6] E. Grossar, M. Stucchi, K. Maex, W. Dehaene, "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies", *Solid-State Circuits, IEEE Journal of, Volume 41, Issue 11*, Nov 2006, pp. 2577-2588.
- [7] S. M. Jahinuzzaman, M. Sharifkhani, M. Sachdev, "Investigation of Process Impact on Soft Error Susceptibility of Nanometric SRAMs Using a Compact Critical Charge Model", *Quality Electronic Design, 2008. 9th International Symposium on*, March 2008, pp. 207-212.
- [8] Berkeley Predictive Technology Model website, <http://www.eas.asu.edu/~ptm/>.



**Figure 5. Power-delay product of the SRAM cell arrays at different temperatures and power supplies a) 9T; b) 6T**



**Figure 6. 6T and 9T SRAM power-delay product distributions due to process variations**