

Fault Tolerant Clockless Wave Pipeline Design *

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T. Feng, B.Jin, *J.Wang and N.Park †

Department of Computer Science
Department of Electrical and Computer Engineering
Oklahoma State University, Stillwater, OK 74078-1053
npark@cs.okstate.edu

Y.B. Kim and F. Lombardi

Department of Electrical and Computer Engineering
Northeastern University, Boston, MA 02115
lombardi@ece.neu.edu

Abstract

This paper presents a fault tolerant design technique for the clockless wave pipeline. The specific architectural model investigated in this paper is the two-phase clockless asynchronous wave pipeline [10] which is ideally supposed to yield the theoretical maximum of performance. Request signal is the most critical component for the clockless-induced control of the wave pipelined processing of data. In practice, the request signal is very sensitive and vulnerable to electronic crosstalk noise, and this problem has become extremely stringent for the ultra-high density integrated circuits today. Electronic noise may devastate the operational confidence level of the clockless wave pipeline. In this context, this paper characterizes the yield and reliability properties of the two-phase clockless asynchronous pipeline. Based on the yield characterization, a simple yet effective fault tolerance architecture and algorithm is proposed on the request signal lines as the most critical component for high confidence clockless asynchronous wave pipeline processing. A reliability model is developed to evaluate the effect of the request signal crosstalk noise, referred to as glitch. An example experiment and simulation is shown to demonstrate the efficiency and effectiveness of the proposed technique.

1: Introduction

Wave pipeline is a pipeline processing technique that can increase the throughput without internal storage spaces and power proposed by Cotton in 1969[4]. Multiple data waves can propagate through the wave pipeline from the PI(Primary Input) to the PO(Primary Output) simultaneously without internal latching. It can achieve the theoretical maximum performance, and draws lots of attentions in the industry nowadays.

Assurance and optimization of yield and reliability is a key to the success of clockless asynchronous wave pipeline technique. Ideally, all path delays from PI to PO are to be equally or

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N.Park is the contact author

near-equally balanced. However, equal-balancing of path-delays is hard to be realized even with help of extensive tuning due to various fabrication and runtime variations such as power consumption, thermal distribution and design errors to mention a few. In addition, clock skews due to the variations in the rise/fall time, and setup and hold time of the storage elements, clock frequency is limited within an increase only by a factor of 2 to 3 even by using the best available design method [5].

Wave pipeline is developed in both synchronous and asynchronous ways. Synchronous wave pipeline uses clock signal to control the synchronous movement of the data bits. It has been successfully implemented as modules in several commercial processors such as floating point unit in IBM 360/91 and external caches in HP PA8000. Asynchronous wave pipeline (clockless wave pipeline(CWP) is used interchangeably in this paper) uses request and acknowledgement signals, or only request signal instead of clock to serve as the reference. CWP is relatively more difficult to deploy than synchronous wave pipeline due to its explorativeness and a few technological hurdles as mentioned before. Clockless wave pipelined circuit has only been experimented in non-commercial sectors such as the two-phase CWP with request signal only as reported in [6] and [10]. The specific architectural model investigated in this paper is the two-phase clockless asynchronous wave pipeline [10] which is ideally supposed to yield the theoretical maximum of performance.

It requires new methods to model and analyze wave pipelined circuit analysis because of high operating speed, narrow range of frequencies, starting/stopping mechanism vacancy, and feedback loops. In [14], testing of synchronous wave pipeline circuits has been proposed in which it was reported that any testing scheme for wave pipelined circuits has to address the faulty conditions for the wave pipelined nature as well as the traditional fault condition. An off-line test pattern-generation was also proposed. In [11], an on-line detection of delay faults in CMOS synchronous wave pipelined circuit was proposed. Another testing circuit for delay fault was devised in [7], in which the proposed testing circuit can be used to monitor the outputs of circuits that are either general, or designed to be self-checking with respect to steady-state errors. Fault tolerance in wave pipeline has not yet been adequately addressed and researched in as an integrated method. In this context, this paper will address and propose a novel fault tolerance technique with focus on the crosstalk noise in request signal lines in CWP.

The fault models for asynchronous wave pipeline has been established and proposed in [15]. The fault models were based on the target architecture of the two-phase asynchronous wave-pipelines. According to the previous result, the correct operation of asynchronous wave pipeline depends on the proper association between the request signals and data waves. In order to manipulate the propagation behavior of data waves, the request signal was assumed to be fault free. However, in practice, request signal is highly sensitive and vulnerable to electronic crosstalk noise (referred to as *glitch*). The current growing trends of VLSI technology is the smaller device geometries, millions of closely spaced interconnections, and higher switching speeds. Therefore, electronic crosstalk noise are very likely to occur, and it appears to be a major problem in the development of next generation high speed integrated circuits [12][1][8] [9]. In general, the request signals are exposed to various electrical and environmental factors such as voltage, temperature, humidity, etc. Crosstalk noises on request signal could be permanent, transient, or intermittent. Any type of crosstalk noise on the request signal propagating through switches, is deleterious, and it may cause serious improper operation between the switches and data waves eventually to yield a faulty output.

The objective of this paper is to characterize the yield and reliability properties of the two-phase clockless asynchronous pipeline. Based on the yield characterization, a simple yet effective fault tolerance architecture and algorithm is to be developed for the request signal lines as the most critical component for high confidence clockless asynchronous wave pipeline processing. A

reliability model will be developed to evaluate the effect of the request signal crosstalk noise.

The following section presents the review and preliminaries of the two-phase asynchronous wave pipeline which is the base architecture of the fault tolerant technique proposed in this paper. Section 3. gives a scrutiny and manifest illumination on the possible consequences resulted from the combinations of different type of switches and crosstalk noises. Section 4. describes the details of the proposed approach and its implementation, and Section 5. proposes the modeling and analysis method to evaluate the experimental results in Section 4. Section 6. shows the experimental simulation and the results. Finally, Section 7. concludes this paper.

2: Preliminaries and Review

In conventional pipeline, there are registers or latches between any two stages, and there is only one data wave active in any stage at any time. The clock cycle time is determined by the maximum stage path delay, i.e., $T_{ck} \geq D_{max}$. Wave pipeline remove all of the internal registers or latches and let multiple data waves propagate through the circuit at the same time, thus the throughput is enhanced greatly. The clock cycle time of wave pipeline with clock is determined not by the maximum path delay but the difference between the maximum path delay and minimum path delay, and its clock cycle is

$$\frac{T_{max}}{N} < T_{ck} < \frac{T_{min}}{N} \quad (1)$$

where N is the number of waves in the circuit(degree of the wave pipeline).

CWP is an asynchronous circuit. A *two-phase asynchronous wave pipeline* is developed by Hauck [10] as shown in Fig 1, which has a two-phase operation by alternating positive and negative level-sensitive switches. Besides, it employs request signal only.

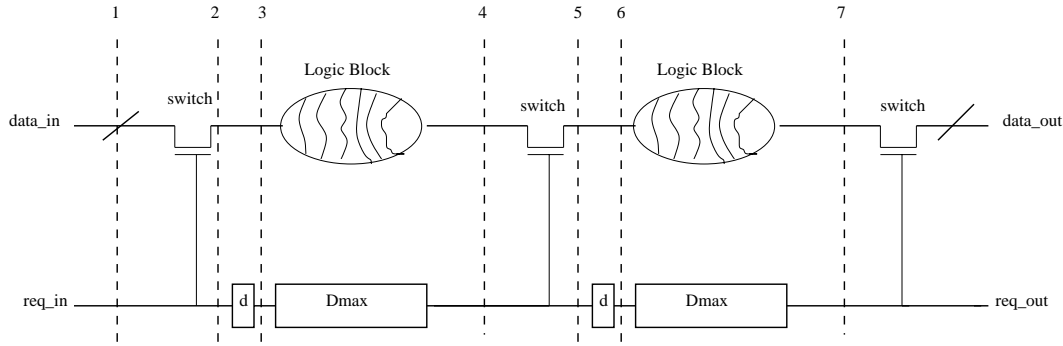


Figure 1. Two-phase asynchronous wave pipeline [10]

As shown in Fig 1[10], two types of switches, namely positive and negative switches, separate the pipelined circuit into several stages and request signal controls the switches. The pair of data waves and request signal enters the CWP at the same time, furthermore they stay coherent in the process of data wave propagation through the circuit. The switch can be opaque or transparent to the data waves. If opaque, the switch latches the data wave and if transparent, the data wave pass the switch without any latching. Specifically, N type switches (negative switches) are made to be opaque to the data waves associated with high request signal and transparent to those associated with low request signal. Vice versa, P type switches (positive switches) are made to be transparent

to the data wave associated with high request signal and opaque to the data wave associated with low request signal.

The propagation of the data wave within the pipelined circuit is intermittent. Once the data wave enters the circuit, it is assigned to a request signal in turn, high or low. By the design rules, data wave associated with high request signal can propagate through N switch directly, but has to be latched by the P switch. On the contrary, data wave associated with low request signal can waltz through P switch but has to stop and be latched by the N switch. Fig. 2 depict the situation of a data wave go through a transparent switch and Fig. 3 describe the situation where a data wave go through an opaque switch.

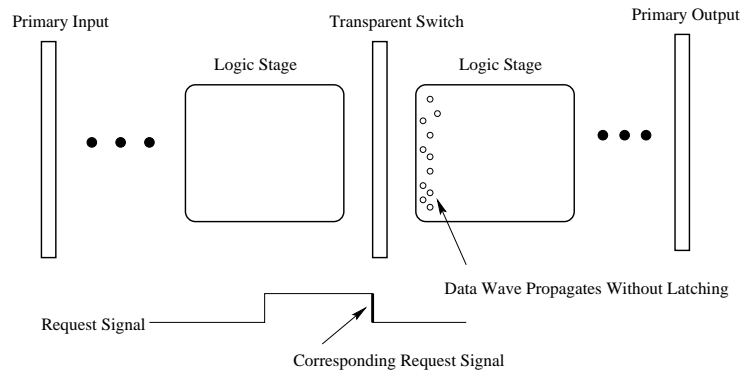


Figure 2. Transparent switch

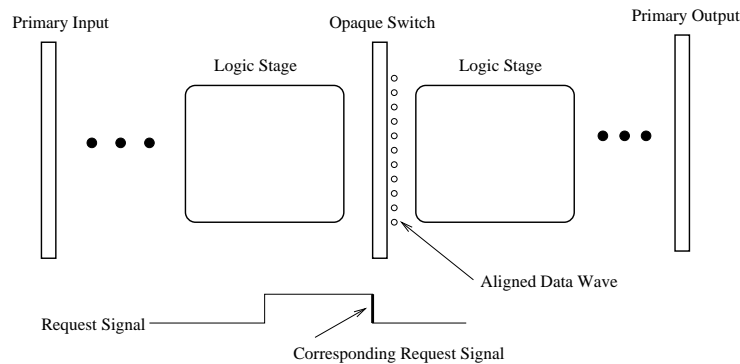


Figure 3. Opaque switch

3: Crosstalk Noise: A Glitch on Request Signal

Crosstalk noises can occur on low or high request signals, and they could effect the regular control of request signal to N or P switches. There are four possible combinations between types of switch and noise altogether. In this section, each possible combination and their effects is analyzed in-depth, thus the solution proposed later to solve this request signal introduced fault problem can be easily comprehended.

3.1 High request signal with crosstalk noise to pass N switch

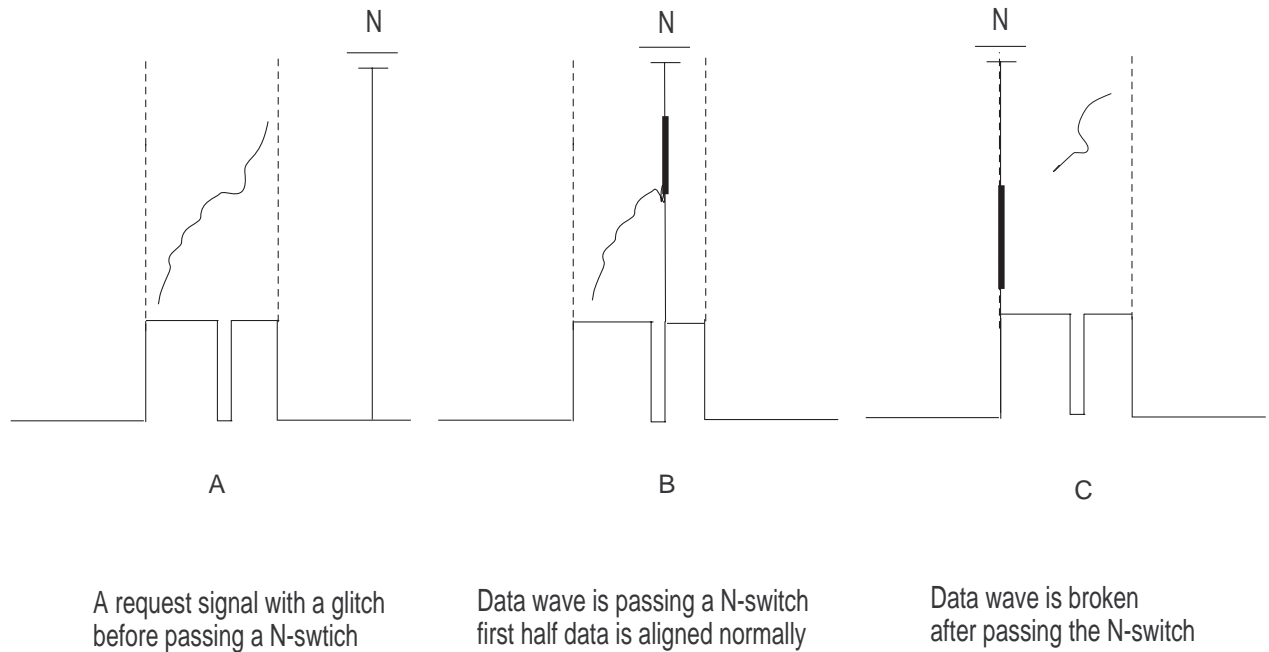


Figure 4. Crosstalk noise on high request signal with the N switch

Fig. 4 shows the instance of crosstalk noise resided high request signal and its associated data wave propagating a N switch. Part A depicts the fault-free situation before the data wave and request signal propagating through the N switch. As mentioned earlier, data wave associated with high request signal has to be latched at N switch, hence at part B in Fig. 4, part of data bits are latched as normal until the crosstalk noise reach the N switch. The crosstalk noise has the complementary electronic signal value to the regular request signal and it mislead the switch, therefore, the switch switches from opaque state to transparent state immediately. Then the latched first half bits of the data wave are permitted to start to propagate in the next stage of circuit, which is improper since the first half bits start to propagate a lot earlier than designed. At this time, these bits could invalidate the previous data wave because the present bits propagation conflicted with the design specification.

The width of crosstalk noises are very short compared with the length of request signal level, so the control signal switches back to normal request signal swiftly. The switch becomes opaque again and the remaining bits of the current data wave are latched by the opaque switch. At the end of this process, half of the data bits are propagating through the next circuit stage and half of them are latched at the current switch. There is a big gap between them and this data broken could causes fault because there may exist bits dependent in the process of bits propagation. Part C in Fig. 4 portray this situation.

Broken data wave with big gap eventually causes **Intra Wave Fault** [15] (the CWP delay fault caused by improper cover of the data wave by the associated request signal level). Fig. 5 traces the broken data wave propagation from the break point to the fault point. Site A is position where

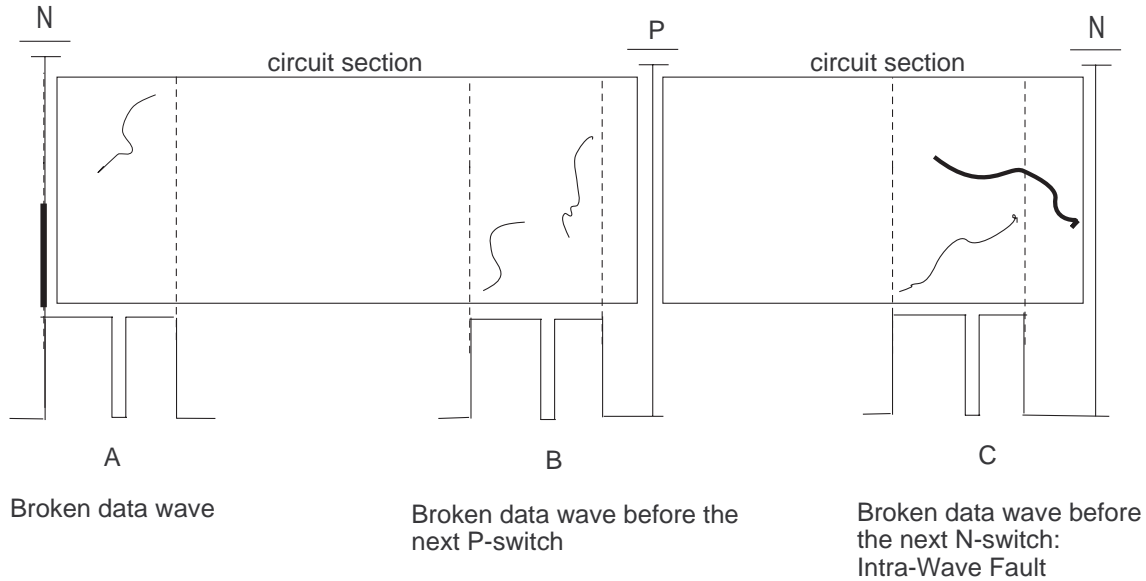


Figure 5. Broken data on N switch cause intra-wave fault

the broken data wave was generated as discussed earlier. Site B displays the situation where the broken data wave reaches the next switch: a transparent P switch. Site C portrays the intra wave fault situation, where the first half data wave propagates too far and goes beyond its limit because of the unexpected earlier startup. Thus it can not be covered by its associated request signal level properly. The more specific explanation is that the first half data wave starts to propagate earlier than designed and its propagation speed remains unchanged despite the crosstalk noise and data broken, thus it reaches the next N switch earlier than normal after propagating through two circuit sections, while in the normal case, all data bits must arrive after the arrival of the frontier of the high request signal.

3.2 High request signal with crosstalk noise to pass P switch

The second combination is the crosstalk noised resided high request signal and P switch. Fig.6 traces the propagation process. The crosstalk noise occurs at site A, before the data wave propagating through the P switch. According to the clockless wave pipelined circuit design rules, the P switch is transparent to the data waves associated with high request signals. Thus, at site B, the data wave is propagating through the P switch without being latched. Site C depicts that the P switch switches to opaque to data wave and recovers rapidly since the crosstalk noise take the control of the P switch instantaneous. The temporary opaque section results a very small section of momentary data latching as shown in the site C, and in site D, this small section of latching data wave causes the tiny data wave broken.

It is important to notice that this tiny broken data does not bring any faults. The difference between this and the situation in the first combination is that this broken is caused by temporary latching other than temporary transparent, and temporary latching does not produce data wave's earlier startup as been discussed in the previous part. Since the width of the crosstalk noise is really small, the gap between the two parts of the data wave is also too small to cause any faults, even if

bit dependence applied.

Note also if the crosstalk noises rate becomes excessive high, multiple single noises may unite into one big glitch. In that case, the temporary latching time is enlarged, and consequently the gap between the two parts of the broken data is broadened, then intra-fault could be possibly occurs. Fortunately, in reality crosstalk noise density is hardly to be so high. So, in this paper, this combination is considered to be faulty free.

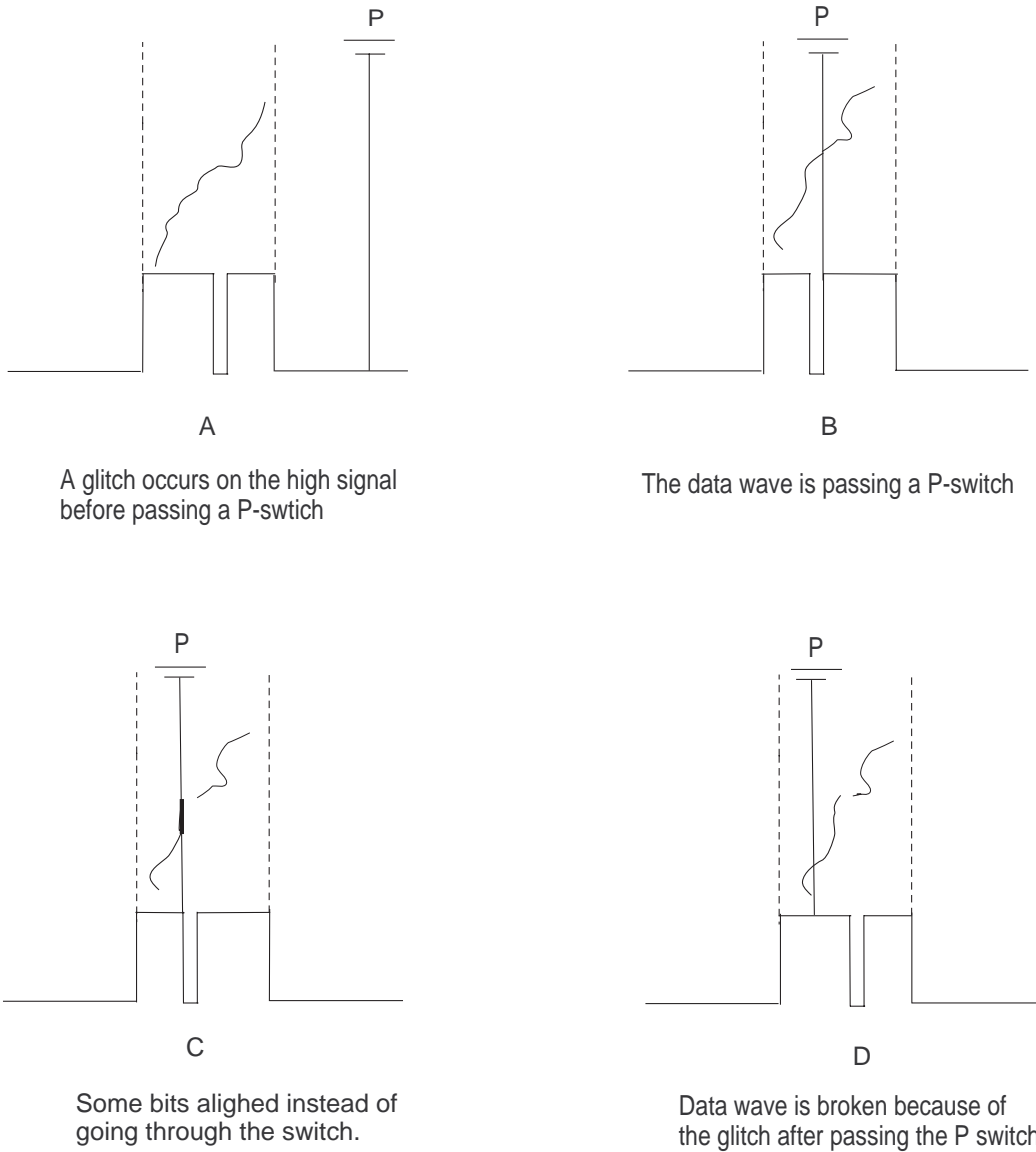


Figure 6. Crosstalk noise on high request signal with P switch

3.3 Low request signal with crosstalk noise to pass P switch

This combination can cause fault. It is very similar to the first combination. Data wave associated with low request signal is latched by the P switch, and the crosstalk noise can broken the data wave with a big gap because of temporary transparent. At the next successive P switch, intra-wave fault and bits dependent fault then occur. This combination is described in Fig. 7 and 8.

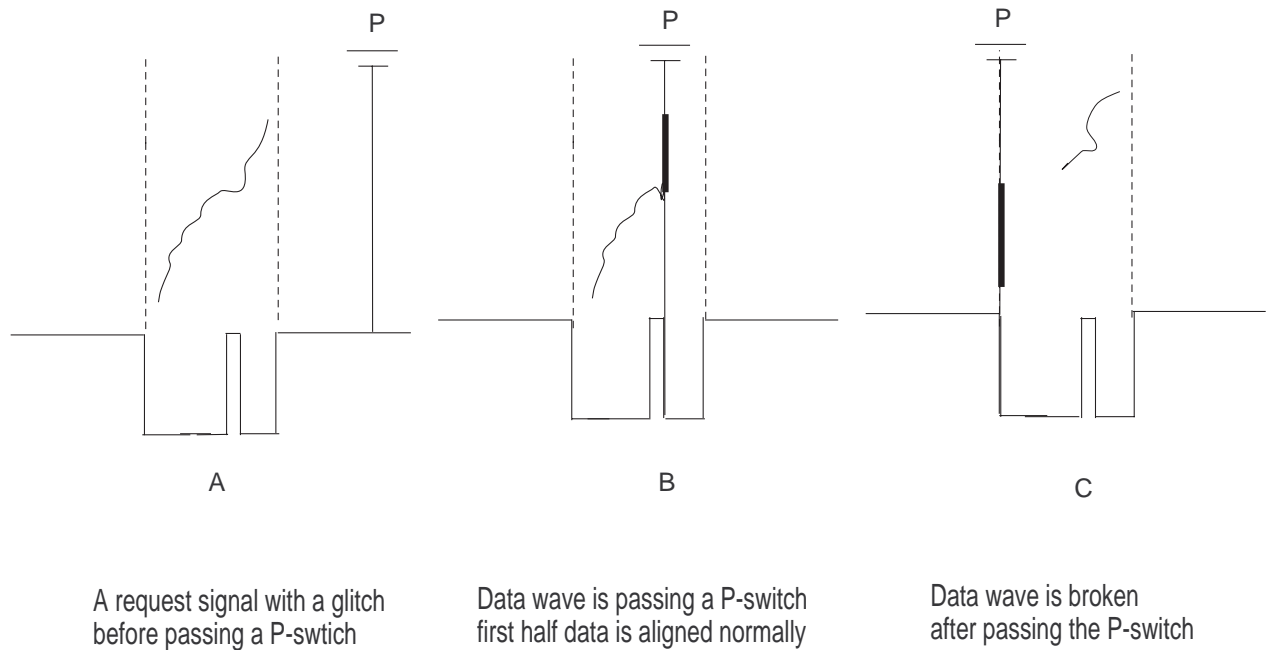


Figure 7. Crosstalk noise on low request signal with P switch

3.4 Low request signal with crosstalk noise to pass N switch

The case is similar with the second combination. Crosstalk noise on low request signal before a N switch does not cause fault since temporary latching does not produce data wave's earlier startup and the tiny data wave broken does not cause bits dependent fault unless extremely excessive crosstalk noise density. The figure depicting this situation are omitted since it is same as Fig.6 except using N switch and low request signal instead of P switch and high request signal.

Up till now, the complete four combinations of request signals and the switches are investigated carefully, two of them, which are high request signal combined with N switch, low request signal combined with P switch are suspicious to results faults in the present of crosstalk noise. The other two combinations, which are high request signal combined with P switch, low request signal combined with N switch are reluctant to generate any faults even crosstalk noises stand on the request signal. This is summarized in Table 1.

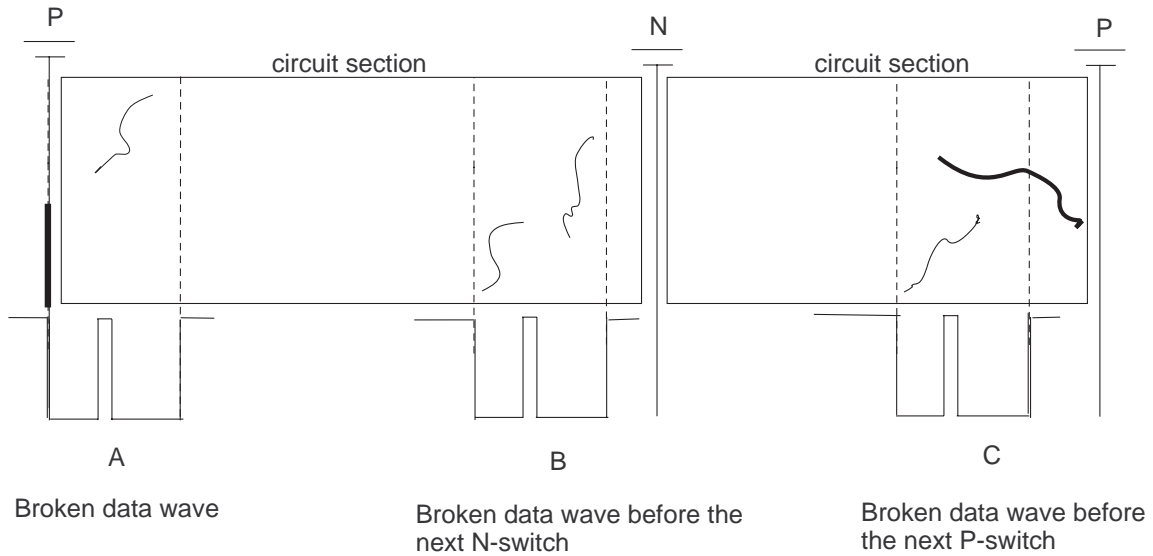


Figure 8. Broken data on P switch cause intra-wave fault

Table 1. fault cases

-	N-switch	P-switch
Crosstalk noise at high request signal	faulty	not faulty
Crosstalk noise at low request signal	not faulty	faulty

4: Proposed Fault Tolerant Request Signal Approach

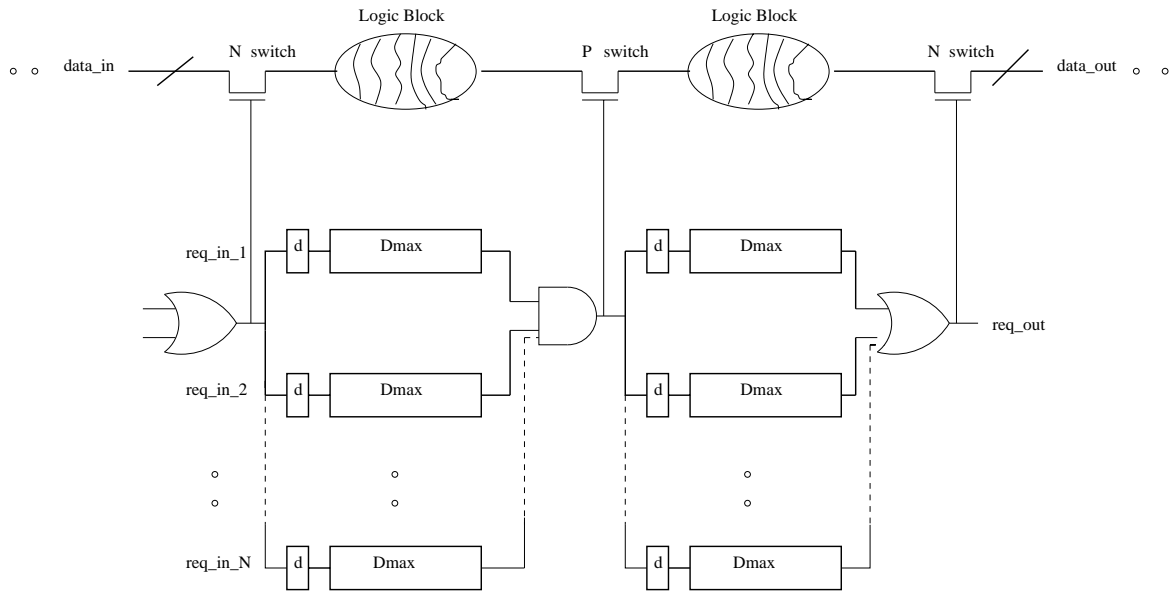


Figure 9. Modified two-phase asynchronous wave pipeline with redundant request signal lines

The fault tolerant approach to solve this crosstalk noise introduced intra-wave fault is proposed in this section. According to the discussion of the interactive behavior of the data waves and switches under the present of faulty crosstalk noise in the previous section, redundant request line are introduced into the two-phase asynchronous wave pipeline architecture to mask the occurred crosstalk noise. The modified architecture is shown in Fig.9.

AND gate can be used to mask the crosstalk noises occurred on the low request signal level and OR gate can mask crosstalk noises on high request signal level. Table 2 explains this by a simple truth table. Double request signals, signal A and B, are assumed to be employed and also crosstalk noises are assumed to occur only on request signal B. So, A is crosstalk noise free and B has noises resided on it as shown in table 2, and A and B are complementary. Clearly, after applied to the appropriate logic gate, the faulty signal B is successfully been discarded.

Note not all crosstalk noises on the request signal can be hidden by this. The only condition

Table 2. Truth Table

A (regular signal)	B (crosstalk noise signal)	A OR B	A AND B
high	low	high	X
low	high	X	low

where this fault mask technique fails is that both of the request signal A and B has crosstalk noises at the same time. In that case, another request line with accurate signal is needed to achieve a higher fault tolerance rate and more reliable system. By this means, the number of request line is expended to N so that the modified pipeline's reliability can be described and calculated theoretically in the next section.

5: Reliability Analysis

Assume λ is the rate that the crosstalk noise occurs on any request signal line from the signal entering the circuit to the signal arrives at the primary output of the circuit and assume the primary request signal line and redundant request signal lines share the same crosstalk noise rate.

5.1 Effectiveness of multiple request signal lines on reliability

After the application of the redundant request signals, the crosstalk noises are masked away except crosstalk noises occurs at every request signal at the same time. so, the final fault rate on the redundant request signal is:

$$\lambda_{total} = \left(\lambda \times \frac{l}{L}\right)^N \quad (2)$$

where l is the minimum valid crosstalk noise width, and L is the length of one request signal section.

Thus, the total reliability of the request signal module is:

$$R(t) = e^{-(\lambda \times \frac{l}{L})^N \times t} \quad (3)$$

Equation 3 is plotted in Fig. 10 with the assumption that 1, 2, 3,4 request signals lines are used and $\lambda = 0.2$, $\frac{l}{L} = 0.3$. It shows that the system reliability enhanced exponentially with number of the redundant request signal lines increase.

5.2 MTTG, λ , and L

Mean time to crosstalk noise (*MTTG*) is the expected time that a high or low signal propagate normally through the wave pipelined circuit before the first crosstalk noise occurs, which can be calculate by the follow integrations 4, where k is the *degree of wave-pipelining* [2] which represents the number of clock cycles need for a signal to propagate through the logic before being latched by the output register and kL is the total length of request signal path within the pipelined circuit.

$$MMTG = \int_0^{\infty} R(t) dt$$

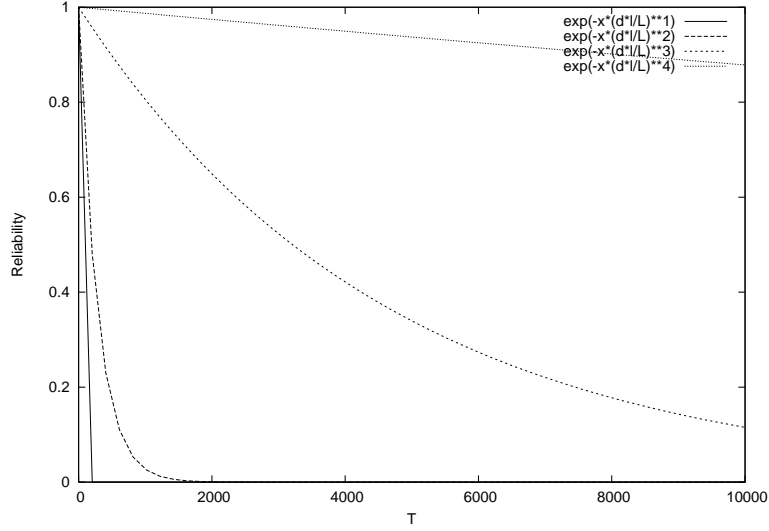


Figure 10. System reliability with 1,2,3,4 request signal lines

$$\begin{aligned}
 &= \int_0^{kL} R(t) dt \\
 &= \int_0^{kL} e^{-\lambda t} dt \\
 &= -\frac{1}{\lambda} e^{-\lambda kL} - \left(-\frac{1}{\lambda} e^{-\lambda(0)}\right) \\
 &= \frac{1}{\lambda} (1 - e^{-kL\lambda}) \tag{4}
 \end{aligned}$$

Equation 4 shown that crosstalk noise rate can influence MTTG in a great extents, the following Fig 11 is plotted based on equation 4 with the assumption of known parameter K, L, and it shows the decreasing trends of MTTG when the crosstalk noise rate increase.

The relationship between the length of the request signal level and MTTG, fault rate can be then easily get as shown in equation 5.

$$L = \frac{\ln(\lambda \times MTTG - 1)}{k\lambda} \tag{5}$$

5.3 Reliability of the redundant request signal in MTTG

The reliability of a single request signal at the time t is:

$$R(t) = e^{-\lambda t} [3] \tag{6}$$

so, at the time point MTTG, the reliability of a single request signal is :

$$\begin{aligned}
 R(MTTG) &= R\left(\frac{1}{\lambda}(1 - e^{-kL\lambda})\right) \\
 &= e^{-\lambda\left(\frac{1}{\lambda}(1 - e^{-kL\lambda})\right)} \\
 &= e^{(e^{-\lambda kL} - 1)} \tag{7}
 \end{aligned}$$

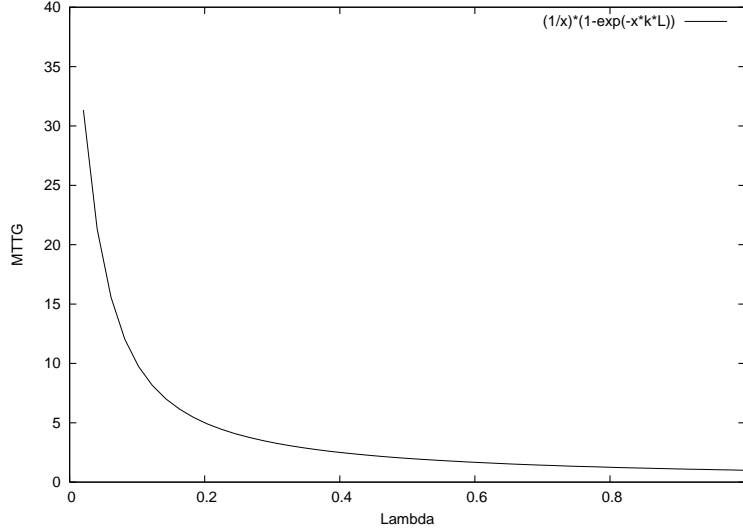


Figure 11.

The reliability of the request signal part of the whole circuit with N request signal lines is:

$$R_{total} = \sum_{i=1}^{N-1} \times N \times R^{N-i} \times (1 - R)^i \times (1 - P) \quad (8)$$

where $P = \lambda^N$.

The reliability of the whole request signal part at time point MTTG can be obtained by combining equation 7 and 8 and displays as follows.

$$\begin{aligned} R(MTTG) &= \sum_{i=1}^{N-1} \times N \times R^{N-i} \times (1 - R)^i \times (1 - P) \\ &= \sum_{i=1}^{N-1} \times N \times (e^{(e^{-\lambda k L} - 1)})^{N-i} \times (1 - (e^{(e^{-\lambda k L} - 1)}))^i \times (1 - \lambda^N) \end{aligned} \quad (9)$$

6: Experimental Results

The circuit implementation is conducted using Cadence to verify the proposed fault tolerant technique. Two request signal lines with crosstalk noises are filtered by AND gate and OR gate respectively. They are then extracted and simulated using Spectre. The designed circuit is shown in Fig.12.

In Fig.13, *input1* and *input2* are the signals of the two request signal lines and crosstalk noises reside on them. The out signal shows that noises resided on the low request signal are successfully masked away by the AND gate. Although the noise density on the high request signal level double, as discussed in section 3, noises on the high request signal level for a P switch is harmless until the crosstalk noise density goes extremely high and in reality, that is hardly occur. Meanwhile the crosstalk noises accumulation can not happen since all the noises resided on high request signal

level, including the original noises and the AND gate introduced noises, will be discarded by the OR gate in the next successive N switch as shown in Fig.14. So there is no other faulty risk introduced by this technique.

Fig.14 demonstrate the OR gate masks the crosstalk noise resided on high request signal. Equivalently, *input1* and *input2* are the two request signals with noises resided on and out is the signal filtered by the OR gate, where the noises on the high request signal are hidden away by the OR gate. Noise density on the low request signal also doubles after OR gate, but normally they will be casted away by AND gate in the next successive P switch.

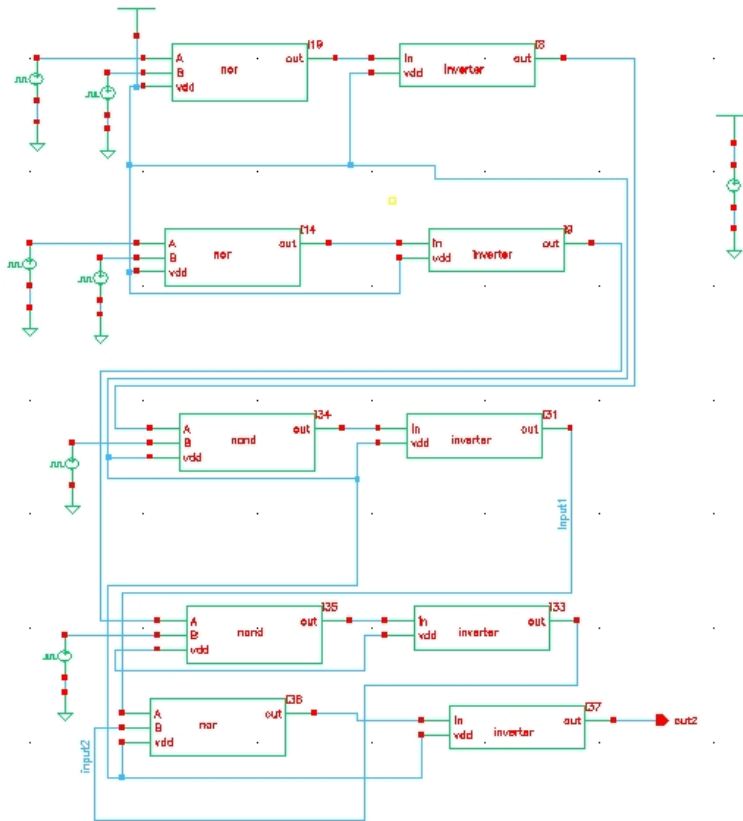


Figure 12. Circuit implementation of the fault tolerant technique

7: Conclusions

This paper has presented a fault tolerant design technique for the clockless wave pipeline with emphasis on the glitch on the request signals. A redundant request signal approach has been experimented and demonstrated a significant reliability enhancement for clockless asynchronous wave pipeline processing with high confidence.

Request signal is the most critical component for the clockless-induced control of the wave pipelined processing of data. In practice, the request signal is very sensitive and vulnerable to electronic crosstalk noise, and this problem has become extremely stringent for the ultra-high density integrated circuits today. Electronic noise may devastate the operational confidence level

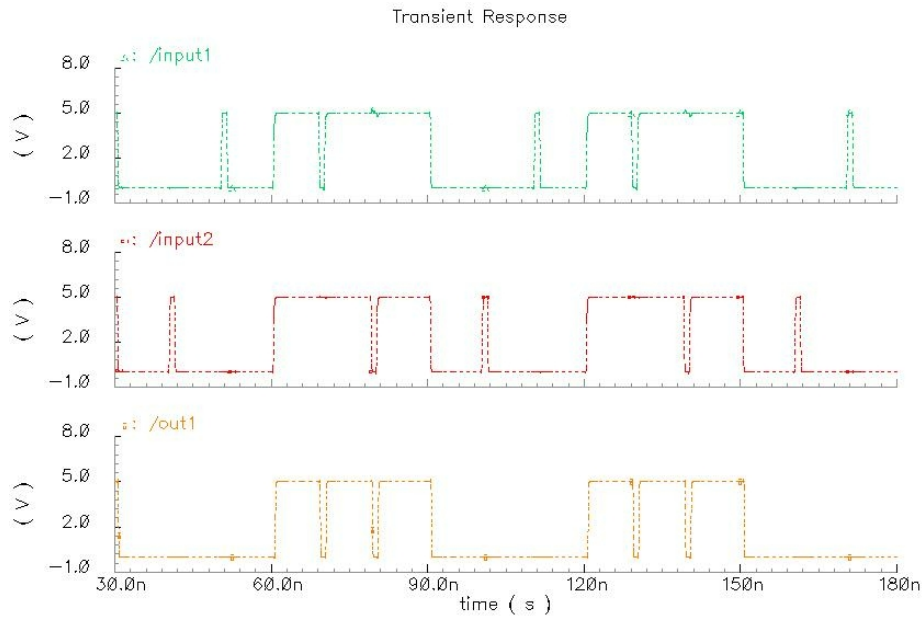


Figure 13. Simulation of crosstalk noise on low request signal masked by AND gate on P switch

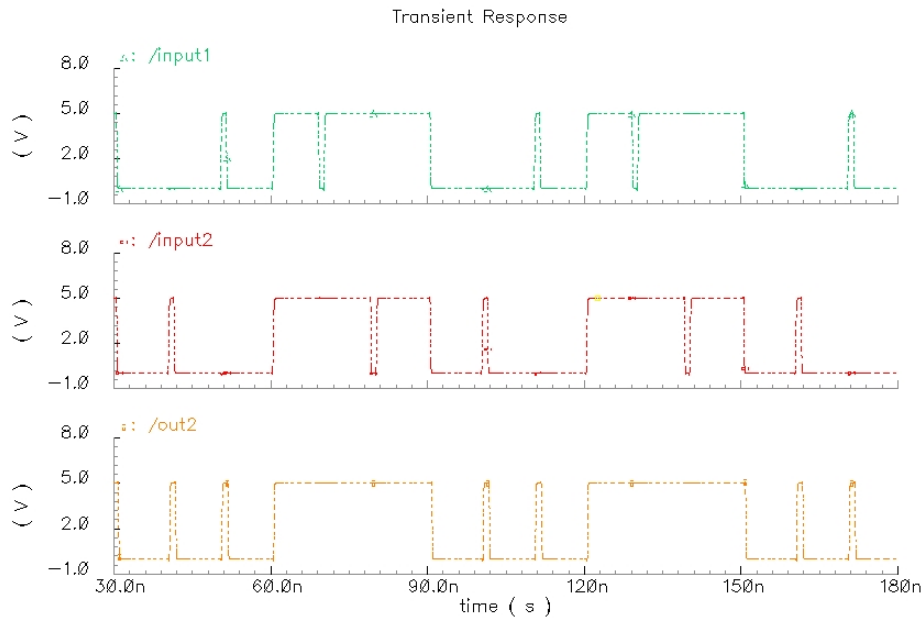


Figure 14. Simulation of crosstalk noise on high request signal masked by OR gate on N switch

of the clockless wave pipeline. In this context, this paper characterizes the yield and reliability properties of the two-phase clockless asynchronous pipeline. Based on the yield characterization, a simple yet effective fault tolerance architecture and algorithm is proposed on the request signal lines as the most critical component for high confidence clockless asynchronous wave pipeline processing. A reliability model is developed to evaluate the effect of the request signal crosstalk noise, referred to as *glitch*. An example experiment and simulation is shown to demonstrate the efficiency and effectiveness of the proposed technique.

It was demonstrated that low level crosstalk noises on a high request signal line may cause a broken datawave (i.e. intra-wave fault on N switches) while no fault on P switches. On the other hand, high signal crosstalk noises on a low request signal line may result in a broken datawave (i.e. intra-wave fault on P switches) while no fault on N switches. Based on this principle, an AND gate was used to mask the high level crosstalk noises on low request signal to a P switch; and an OR gate was used to mask the low level crosstalk noises on high request signal to an N switch. This simple yet effective approach can mask all the crosstalk noises on request signal lines except for that every redundant request signal line is impaired by crosstalk noise at the same time. It has been demonstrated that the reliability of the clockless asynchronous wave pipeline is increased exponentially as more redundant request signal lines are incorporated. Also, the reliability with respect to MTTG (Mean Time To Glitch), λ (glitch rate), and L (request signal level length) have been provided. Finally, an example experiment has been conducted to verify the efficiency and effectiveness of the theoretical fault tolerant request signal design.

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