

ENVIRONMENTAL BASED CHARACTERIZATION OF SoC FOR STRATIFIED TESTING

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Abstract – This paper proposes a novel environmental-based method for evaluating the good yield rate (GYR) of Systems-on-Chip (SoC) during fabrication. Testing and yield evaluation at high confidence are two of the most critical issues for the technological success of SoC. Since a SoC is designed and assembled using deeply embedded Intellectual Property (IP) cores on a single chip, then at fabrication, it is not possible to rely on conventional testing and yield evaluation methods because there is no a-priori information or data available on the yield of the fabricated IPs due to the different integration processes of the cores. This is radically different from previous technologies in which the known-good-yield of ASIC or MCM chips for example is extracted from physical-level information. The proposed method relies on different aspects of fabrication (which are quantified by the so-called Environmental Parameters (EP)). EPs which could be highly correlated to the yield, are analyzed using a comprehensive statistical method to improve the accuracy of the estimated yield of the SoC as well as for directing the test process. Numerical simulation results are provided to show that the proposed method significantly improves the confidence interval of the estimated yield when compared to conventional random testing.

I. INTRODUCTION

The rapid advances in technology for manufacturing complex integrated circuits have been made possible by the high density integration of a large number of components and devices; today, a complete system can be integrated and assembled on a single chip (SoC). Due to density and complexity, conventional fabrication methods are facing tremendous challenges when manufacturing SoCs. The miniaturized size and light weight as well as performance benefits (such as power consumption, high speed and thermal distribution) have made

SoC a rapidly expanding market with great potential.

However, SoC manufacturing is encountering major hurdles as related to achieving an acceptable yield at high confidence level with an efficient testing technique. For SoC, conventional testing methods are impractical and costly; methods based on Very Large Scale Integration (VLSI) technology for implementing ASIC (Application-Specific IC) and MCM (Multichip Module) are not effective because they may not capture the new processes involved in SoC manufacturing.

An SoC is assembled by using Intellectual Property (IP) cores as components. As IP cores are deeply embedded in a single chip, it is not readily possible to rely on conventional testing and yield evaluation methods. There is no a-priori information or data available on the yield of the components. Moreover, wafer or chip level information has limited relevance due to the disparate integration processes of the IP cores and the lack of known physical-level yield. This is substantially different from custom optimized ASIC with a well-exercised yield, or MCM with known-good-yield. Since there is no significant information available during the integration and test of the embedded IP cores, past work on correlation between fabrication and related features (such as yield and fault rate), is not applicable.

In this paper, the proposed method relies on a set of fea-

tures which experimentally appear in the fabrication process and directly affect the yield and test quality. These features are extracted and quantified; they are referred in this paper as the *Environmental Parameters* (EPs). EPs can be also highly correlated and through an extensive statistical analysis, they can be used to derive a stratified-based test process and assess the yield of the SoC. In this paper, an accurate GYR (i.e. Good Yield Rate as confidence level of estimated yield) is established by using a novel method in which highly correlated EPs are categorized at different levels through a characterization of different environmental parameters and a statistical analysis of their interactions. This process also identifies the stratification criteria for selecting (or sampling) the chips (as components of the SoC) and testing them by providing statistical information on whether or not an EP has a significant impact on the GYR. Within this approach, this is possible because SoCs from the same wafer are fabricated under an homogeneous environment, i.e. no significant variations occur within a wafer. Therefore, sampling is conducted at SoC-level and EPs are used to guide through a novel characterization process; this process effectively relies on a statistical test hypothesis technique which in this paper exploits the so-called Analysis of Variance (ANOVA) method. Different measures such as the level in EPs for a given SoC fabrication condition, or the stratification variables for sampling-based testing to estimate the GYR are utilized. Having identified a proper stratification structure, a post-stratified sampling-based test process is conducted to estimate the unbiased estimator of GYR by using a *ratio estimation* technique. Hence, a further objective of this paper is to propose a new SoC-specific test method to enhance the confidence level of the estimated GYR with high accuracy and ensuring the efficient testing of the SoC as final product of the assembly of the IP cores.

This paper is organized as follows. In section 2, literature related to SoC testing is reviewed; previous works are also introduced. The basic principles and procedure of the proposed method are described in Chapter 3. The performance of the proposed stratified sampling-based method in comparison with a random sampling-based test method is presented in Section 4. In the final section, discussion and conclusion are presented.

II. REVIEW AND PRELIMINARIES

For MCM technology, discrete VLSI chips of different types are mounted on a wafer substrate (such as global power, clock, and distribution networks). In MCM, the chips of the same type are assumed to constitute a *stratum* [1]. Chips of the same type are procured from the same manufacturer with a uniform KGY (i.e. a low variance in their KGY). A heterogeneity in KGY (i.e. high variance in KGY) between chips in different strata is assumed as different manufacturers can be involved. This is referred as *stratification*. In [3], a *stratified test* method has been proposed for testing Multi-Chip Module (MCM) systems. Its advantages are the improvement in qual-

ity level and cost-effectiveness. This approach referred to as the Lowest Yield-Stratum First-Testing (LYSFT) considers the unevenness of Known-Good-Yield (KGY) of stratification as a criterion for testing the chips on a MCM for quality enhancement [3] - [8].

There have been extensive studies reported on statistical approaches for testing ICs. Sequential statistical analysis has been employed as a standard vehicle to manipulate the correlation among Defect Level (DL), yield, random test length, and detection probability. Instead of using deterministic DL analysis, a sequential statistical analysis directly examines the random behavior of test vectors and results in an elegant derivation of the DL. The DL derived by using this method can be then used to find the average confidence in the probability of fault-free chips, which in turn is represented by the yield and the coverage [9] - [14]. The DL obtained through random testing can be evaluated by a probability distribution rather than a value as pointed out in [9]. The probability density function of a DL can be approximated by using the standard normal distribution; the confidence degree on the defect level can thus be derived. It has been shown that the high confidence degree of a specific DL can be achieved using large sample chips [15].

A detailed study on design quality has been conducted in [16]; design quality is considered from an architectural level to include test coverage for those cases in which design quality has a significant impacts on the quality of the final product; in particular, it has been reported that testability requirements at system level though functional and structural test reuse make possible to monitor and improve test effectiveness after the physical layout implementation [16]. The proposed ET is featured with the following components: 1. To identify EP levels highly co-related with Good Yield Rate (GYR) by using experimental design and test technique; 2. To conduct stratified sampling-based testing with respect to the focused EP levels as its stratification criteria without additional chips to test; 3. To estimate GYR with ratio estimation.

In this context, using an SoC, it is possible to integrate the many digital and analog functions needed for consumer electronic products (such as home appliances and advanced mobile devices) on a single Very Large Scale Integrated (VLSI) chip. A SoC can accommodate complex functions usually associated with today's systems. However, it is difficult to test and assure the quality of a SoC using conventional VLSI test methodologies due to the high density and complexity at deep sub-micron scale.

III. PROPOSED METHOD

The procedure of the proposed method to estimate the GYR, is shown in Figure 1; it consists of different steps as outlined next in more detail. The proposed method has the following unique features as corresponding to each of these steps:

- Through an environmental-based method to identify the EPs and their levels which could be correlated with the Good Yield Rate (GYR).
- Through a statistical analysis to establish the acceptance test of the EPs and outcome with respect to the correlation with the GYR.
- To identify the stratification conditions for sampling-based testing of the SoCs.
- To estimate with high accuracy the GYR through a ratio procedure.

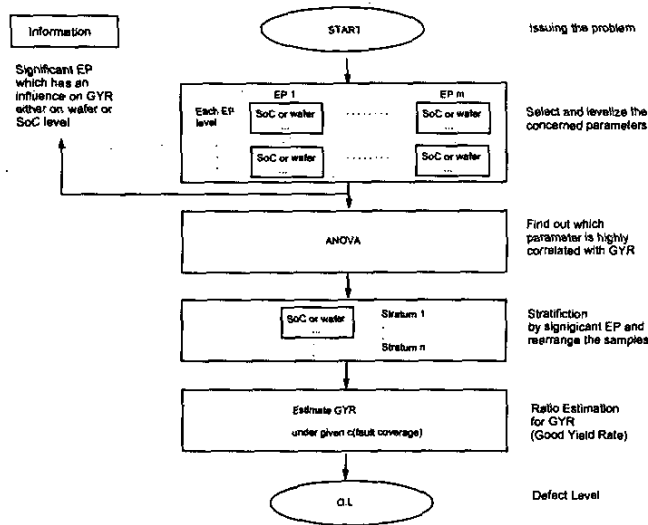


Fig. 1. Proposed environmental-based method

A. Environmental Characterization

The environmental characterization of an SoC is dependent on many parameters, referred to as EPs (environmental parameters). An EP can be identified at physical level (such as temperature or pressure) as well as at technology level (line width, power consumption for example). The interaction among EPs can affect different measures (such as GYR) during the fabrication of a SoC.

A *two-way classification* method is proposed for identifying the Environmental Parameters (EPs) which can be highly correlated with the GYR. This can be extended to a *multi-way classification* without loss of generality [17]. Hereafter, for sake of simplicity only a two-way classification process is presented.

Each *level* represents a range of values for EP in the environmental characterization. For instance, suppose two EPs are selected, i.e. the temperature (denoted by $A = \{A_i\}$, $i=1, \dots, p$) and the pressure (denoted by $B = \{B_j\}$, $j=1, \dots, q$). So, there are $p \times q$ so-called *treatments* (i.e. each treatment is a coparameter of A_i and B_j). Within each treatment a set of SoCs is

sampled, i.e. y_{ijk} represents the sample SoCs within the range of the i th level of A , the j th level of B ; and the r th sample in the ij th treatment, where $1 \leq i \leq p, 1 \leq j \leq q$. A *sample treatment table* can be generated accordingly (an example is omitted due to space limit).

For example, let the levels of each EP be given as follows:

- Levels of A (temperature): $A_1(100^\circ\text{C}), A_2(105^\circ\text{C}), A_3(110^\circ\text{C}), \dots, A_p$
- Levels of B (pressure): $B_1(100\text{N/m}^2), B_2(105\text{N/m}^2), B_3(110\text{N/m}^2), \dots, B_q$

The theoretical model of a two-way classification method (as used in the proposed approach) can be expressed within a statistical framework as follows.

Let Y_{ijk} be the observed GYR of the tested SoC sample within the i th level of A , the j th level of B , and the r th sample of SoC in the ij th treatment with $1 \leq i \leq p, 1 \leq j \leq q, 1 \leq k \leq r$; hence,

$$Y_{ijk} = \mu + \alpha_i + \beta_j + \gamma_{ij} + e_{ijk}, \quad i = 1, 2, \dots, p, j = 1, 2, \dots, q, \quad (1)$$

where

- μ is the total mean GYR from the sampled SoCs.
- α_i is the Y_{ijk} in the i th treatment of A .
- β_j is the Y_{ijk} in the j th treatment of B .
- γ_{ij} is the interaction between the i th treatment and the j th treatment.

Let e_{ijk} be the residual, i.e. the difference between the observed and estimated GYRs, this can be expressed as

$$e_{ijk} \sim N(0, \sigma^2) \quad (2)$$

B. Statistical Analysis

By using the model and the equations given previously, a statistical acceptance method such as the *F-test* can be conducted next. The *F-test* is based on a *sum of the squares* technique and is used to determine whether to accept an EP, i.e. based on the environmental characterization whether the EP is highly correlated with the GYR under a specified *significance level* (denoted by α); this is the probability of making an erroneous decision when selecting an EP (in generally, its value is rather low). To conduct the *F-test* two new expressions must be derived. The first equation is the difference (denoted by $y_{ijk} - \bar{y}_{\dots}$) between the observed GYR (y_{ijk}) and the total mean (\bar{y}_{\dots}) of the GYR from the sampled SoCs.

Therefore,

$$\begin{aligned} \sum_{i=1}^p \sum_{j=1}^q \sum_{k=1}^r (y_{ijk} - \bar{y}_{...})^2 &= qr \sum_{i=1}^p (\bar{y}_{i..} - \bar{y}_{...})^2 \quad (3) \\ + pr \sum_{j=1}^q (\bar{y}_{.j.} - \bar{y}_{...})^2 &+ r \sum_{i=1}^p \sum_{j=1}^q (y_{ij.} - \bar{y}_{i..} - \bar{y}_{.j.} \\ &+ \bar{y}_{...})^2 + \sum_{i=1}^p \sum_{j=1}^q \sum_{k=1}^r (y_{ijk} - \bar{y}_{ij.})^2 \end{aligned}$$

where

- $\sum_{i=1}^p \sum_{j=1}^q \sum_{k=1}^r (y_{ijk} - \bar{y}_{...})^2 = \text{SST}$ is the sum of the squares (it represents the variation of each sampled SoC).
- $qr \sum_{i=1}^p (\bar{y}_{i..} - \bar{y}_{...})^2 = \text{SSA}$ is the sum of the squares (it represents the variation of A).
- $pr \sum_{j=1}^q (\bar{y}_{.j.} - \bar{y}_{...})^2 = \text{SSB}$ is the sum of the squares (it represents the variation of B).
- $r \sum_{i=1}^p \sum_{j=1}^q (y_{ij.} - \bar{y}_{i..} - \bar{y}_{.j.} + \bar{y}_{...})^2 = \text{SS}(A*B)$ is the sum of the squares which represents the interaction between A and B ; this operation is denoted by $*$.
- $\sum_{i=1}^p \sum_{j=1}^q \sum_{k=1}^r (y_{ijk} - \bar{y}_{ij.})^2 = \text{SSE}$ is the sum of the squares to represent the residual, i.e. it is the probability of accepting the EP if it is highly correlated with GYR after the F-test.

A test hypothesis must be made to conduct the F-test based on the previous expressions; in this case, the hypothesis is that there exists at least a non zero EP level; otherwise, there exists a joint effect by the interaction between the two EPs. The summary of the test hypothesis is given in Table I.

The test hypothesis is based on the ANOVA of the two-way classification. The statistical parameters are shown in Table II.

In Table II, if each F -value does not satisfy the significance probability (i.e. $S\text{Prob}$), then the respective EP is rejected; moreover if the interaction between A and B (i.e. $(A*B)$) does not satisfy the significance probability (i.e. $P(F < f_3)$), then $(A*B)$ has no stochastic correlation with GYR. Using this method, the EPs and their levels which could be highly correlated to GYR, can be found together with the interactions among EPs. This information will be used to provide a better understanding of the SoC fabrication process, and establishing a criterion for stratified sampling-based testing.

C. Stratification for Sampling-based Testing

In the proposed method, *stratified sampling* is used for testing SoCs. A sampling-based testing for SoCs approach is different from a conventional method because the Good Yield Rate (GYR) is the ratio estimator under the assumption that the variance of GYRs of the sampled SoCs (denoted by S_h^2) is

homogeneous in each stratum. The variance is asymptotically given by

$$V(Y_{conv}) = \frac{N-n}{Nn} \bar{S}_h^2 \left[1 + \frac{1}{\bar{n}_h} \left(\frac{L-1}{L} \right) \right] \quad (4)$$

where

- \bar{S}_h^2 is the mean of S_h^2 ,
- N is the total number of sampled SoCs,
- $\bar{n}_h = n/L$, n is the total number of sampled SoCs, L is the total number of strata.

If \bar{n}_h is large enough, then the variance of Y_{conv} [17] is

$$V(Y_{conv}) = \frac{N-n}{Nn} \bar{S}_h^2 \quad (5)$$

Next, the sampled SoCs from the treatments in the environmental characterization are rearranged to build a new framework with the EPs which were accepted by the F-test.

D. Estimation of GYR

The true value of Y (or GYR, good yield rate) can be represented by

$$Y = \frac{\sum_h^L N_h Y_h}{N} = \frac{\sum_h^L \sum_i^{N_h} y_{hi}}{N} = \frac{A}{N} \quad (6)$$

where

- A is the number of SoCs which has been tested and diagnosed as fault free, thus contributing to the GYR.
- L is the number of strata.

For stratified sampling-based test, the unbiased estimator of Y is given by

$$\hat{y}_{st} = \frac{\sum_h^L N_h \hat{y}_h}{N} \quad (7)$$

where

$$\hat{y}_h = \frac{\sum_{i=1}^{n_h} y_{hi}}{n_h} = \frac{a_h}{n_h} \quad (8)$$

and its variance is

$$V(\hat{y}_{st}) = \frac{1}{N^2} \sum N_h^2 \frac{N_h - n_h}{N_h - 1} \frac{S_h^2}{n_h} \approx \frac{1}{N^2} \sum N_h^2 \frac{S_h^2}{n_h} \quad (9)$$

For comparison with random sampling-based test, the unbiased estimator of Y is

$$\hat{y}_r = \frac{\sum_{i=1}^n \hat{y}_i}{n} \quad (10)$$

and its variance is

$$V(\hat{y}_r) = \frac{S^2}{n} \left(\frac{N-n}{N-1} \right) \approx \frac{S^2}{n} \quad (11)$$

Using these estimators, the accuracy (denoted by \hat{y}_{st} and \hat{y}_r respectively) versus the actual value Y can be derived.

TABLE I
TEST HYPOTHESIS

EP	Hypothesis	F-test
A	$H_0 : \alpha_1 = \alpha_2 = \dots = \alpha_p = 0$	$F = \frac{MSA}{MSE}$
B	$H_0 : \beta_1 = \beta_2 = \dots = \beta_q = 0$	$F = \frac{MSB}{MSE}$
A*B	$H_0 : \gamma_{ij} = 0, i = 1, \dots, p, j = 1, \dots, q$	$F = \frac{MS(A*B)}{MSE}$

where α : confidence level

TABLE II
ANOVA RESULTS FOR THE TWO-WAY CLASSIFICATION

EP	SS	d. f.	MS	F value	SProb.
A	SSA	p-1	MSA=SSA/(p-1)	f1=MSA/MSE	P(F >= f1)
B	SSB	q-1	MSB=SSB/(q-1)	f2=MSB/MSE	P(F >= f2)
(A*B)	SS(A*B)	(p-1)(q-1)	MS(A*B)=SS(A*B)/(p-1)(q-1)	f3=MS(A*B)/MSE	P(F >= f3)
Resid.	SSE	pq(r-1)	MSE=SSE/pq(r-1)		
Total	SST	pqr-1			

where SS is the sum of the squares, MS is the mean square, d.f. is the degree of freedom, F-value is the the F-test for the hypothesis

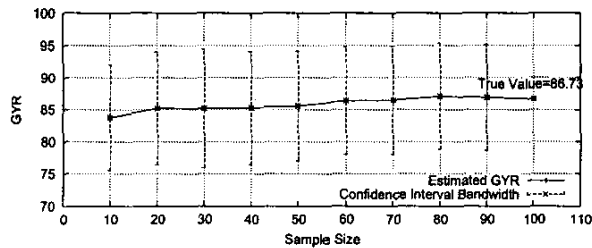


Fig. 2. Confidence interval of random testing

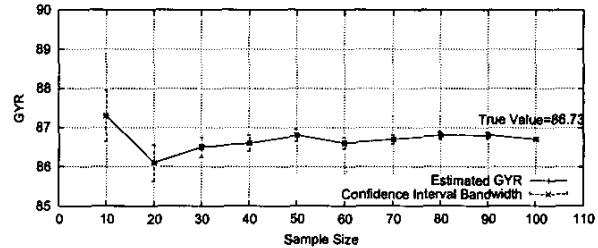


Fig. 3. Confidence interval of proposed testing

IV. SIMULATION RESULTS

In the analysis it is assumed that the sampled SoCs are manufactured in a fabrication environment as described previously and the value corresponding to the observed Y of an SoC is randomly generated for the EPs. The total number of SoCs to be tested is fixed to 100. In the simulation, the actual value of Y (i.e. GYR) is assumed to be 86.7. After having found the highly correlated EPs and their levels, then the observed Y 's of the sampled SoCs can be rearranged into strata as follows.

The Y 's for the proposed method and random sampling-based testing can be calculated using the sample SoC variance for various sizes as shown in Table III.

The numerical simulation model and the steps for the proposed test method can be described as follows.

1. Random generation of GYR samples.
2. Stratification of the GYR samples.
3. GYR estimator (y_r) and confidence interval (S_{y_r}) of random testing.

4. The GYR estimator (y_e) and the confidence interval (S_{y_e}) of the proposed method.

The GYR estimators and confidence intervals of random testing (the proposed method) for different sample sizes ($n = 10, 20, \dots, 100$) are shown in the first and second (third and fourth) columns of Table III, respectively.

Comparison is made with respect to the confidence interval of the two testing methods (proposed and random testing) and is shown in Figures 2 and 3 with respect to the true value of Y (i.e. GYR) on the vertical axis. Figures 2 and 3, show that there is a significant increase in accuracy compared with random sampling-based testing; and also it is evident that there is less disagreement between the true value of Y and the value as estimated by the proposed method. Such disagreement is higher when the value of Y found by random sampling testing is utilized. This indicates that the proposed method improves both the accuracy of Y and its confidence level.

TABLE III
ACCURACY COMPARISON FOR PROPOSED METHOD VERSUS RANDOM SAMPLING-BASED TESTING

Sample size	GYR estimator (y_r) of random testing	Confidence interval (S_{y_r}) of random testing	GYR estimator (y_e) of stratified testing	Confidence interval (S_{y_e}) of stratified testing
10	83.8	8.24	87.3	0.66
20	85.2	8.80	86.1	0.46
30	85.2	9.25	86.5	0.26
40	85.3	8.87	86.6	0.21
50	85.6	8.58	86.8	0.16
60	86.4	8.40	86.6	0.14
70	86.5	8.47	86.7	0.12
80	87.1	8.28	86.8	0.10
90	86.9	8.24	86.8	0.09
100	86.7	-	86.7	-

V. DISCUSSION AND CONCLUSIONS

This paper has proposed a novel environmental-based method for evaluating the good yield rate (GYR) of Systems-on-Chip (SoC) during fabrication. Testing and yield evaluation at high confidence are two of the most critical issues for the technological success of SoC. The main novelty of the proposed method is twofold: to provide a better understanding for the integration and fabrication of SoCs and their yield with high confidence level; to propose an efficient test approach and accurate method for calculating the Good Yield Rate (GYR). Initially, the proposed method identified and selected a set of EPs that are highly correlated with GYR, using a multi-way classification technique. Next, it built a stratified sampling-based testing framework in which the EPs are divided into levels as test criterion. Finally, an unbiased estimator was derived for the GYR with minimum variance as solution to yield evaluation for SoC fabrication. Numerical simulation results have been provided. As an example, a numerical experiment was given to show that the proposed method significantly improves the confidence interval of the estimated yield when compared to conventional random testing.

References

- [1] C. M. Habiger and R. M. Lea, "Cost and Delivery Benefits of Fault-tolerant Multi-chip Modules for Massively Parallel Computing," *Proc. IEEE Int. Workshop on DFT in VLSI Systems*, Venice, Italy, Oct. 1993
- [2] Y. Zorian, "A Structured Testability Approach for Multi-Chip Modules Based on BIST and Boundary-Scan," *IEEE Trans. Compon. Pkg. Mfg. Tech. -Part B*, Vol. 17, No. 3, pp.283-290, Aug. 1994
- [3] N. Park, and F. Lombardi, *Analysis of Stratified Testing for Multichip Module Systems*, IEEE Trans. on Reliability, Vol.51, No.1, Mar., 2002
- [4] J. K. Hagge, and R. J. Wagner, *High-Yield Assembly of Multichip Modules Through Known-good IC's and Effective Test Strategies*, Proc. Of the IEEE, Vol. 80, No. 12, pp. 1965-1994, Dec. 1992.
- [5] C. M. Habiger and R. M. Lea, *Cost and Delivery Benefits of Fault-tolerant Multi-chip Modules for Massively Parallel Computing*, Proc. IEEE Int. Workshop on DFT in VLSI Systems, Venice, Italy, Oct. 1993.
- [6] M. S. Abadir, A. R. Parikh, et al., *Analyzing Multichip Module Testing Strategies*, Proc. IEEE Design and Test of Computers, Vol. 11, No. 1, No. 1, pp. 40-52, 1994.
- [7] M. Iubaszewski, M. Marzouki, and M.H. Touati, *A Pragmatic Test and Diagnosis Methodology for Partially Testable MCMs*, Proc. IEEE MCMC, pp. 108-113, Mar. 1994.
- [8] D. P. Siewiorek, and R. S. Swqz, *Reliable Computer System, Design and Evaluation*, Second Edition, Digital Press, 1992.
- [9] W. -B. Jone, *Defect Level Estimation of Circuit Testing Using Sequential Statistical Analysis*, IEEE trans. On Computer-Aided Design of Integrated Circuits and System, Vol. 12, Issue 2, pp. 336-348, Feb. 1993
- [10] R. L. Wadsack, *Fault coverage in digital integrated circuits*, Bell Syst. Tech. J., vol. 57, pp. 1475-1488, May-June 1978.
- [11] T. W. Williams, and N. C. Brown, *Defect level as a function of fault coverage*, IEEE Trans. Computers, vol. C-30, pp. 987-988, Dec. 1981.
- [12] T. W. Williams, *Test length in a self-testing environment*, IEEE Design & Test, vol. 2, pp. 59-63, Apr. 1985.
- [13] E. J. McCluskey and F. Buelow, *IC quality and test transparency*, IEEE Trans. And Electron., pp. 197-202, May 1989.
- [14] D. R. Tryon, *Self-testing with correlated faults*, Proc. ACM/IEEE Design Automation Conf., June 1986, pp. 374-377, 1986
- [15] P. Gondalia, A. Gutjahr, and W. -B. Jone, *Realization high measure of confidence for defect level analysis of random testing*, IEEE Test Conference, 1993. Proceedings., International pp. 478-487, 17-21 Oct. 1993.
- [16] O. P. Dias, M. B. Santos, J. P. Teixeira, J. Semiao, and I. M. Teixeira, *Quality of Electronic Design: from Architectural Level to Test Coverage*, IEEE Quality Electronic Design, 2000. ISQED 2000 Proceedings., 2000 First International Symposium pp. 197-202, 20-22 March 2000.
- [17] R.G.D. Steel, J. H. Torrie, and D. A. David, *Principles and Procedures of Statistics*, McGraw Hill College Div. 1996.
- [18] T. Yamane, *Elementary Sampling Theory*, Prentice-Hall, Englewood Cliffs, N.J.,1967
- [19] M. H. Hansen, W. N. Hurwitz, and W. G. Madow, *Sample Survey Methods and Theory* John Wiley and Sons, New York, Vols. 1 and 2. 1953.
- [20] W. G. Cochran, *Sampling Techniques* John Wiley and Sons, New York, 1977.

options on processor core Apr.-May 2001.
and Systems, Vol. 20, Issue 3, pp. 426-439, Mar. 2001.