

DESIGN OF ENHANCED DIFFERENTIAL CASCODE VOLTAGE SWITCH LOGIC (EDCVSL) CIRCUITS FOR HIGH FAN-IN GATE

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ABSTRACT

In this paper, a new logic-style, Enhanced Differential Cascode Voltage Switch Logic (EDCVSL) is presented for high performance and low power VLSI. EDCVSL simplifies the logic tree of DCVSL, and dramatically reduces the number of interconnects by eliminating the complementary inputs maintaining the feature of DCVSL. Simulation results of EDCVSL show less power consumption compared to the traditional DCVSL architecture while EDCVSL keeps DCVSL advantages.

1. INTRODUCTION

This paper will describe a new logic family which can substantially reduce area and increase speed of CMOS circuits. A large number of CMOS differential logic families have been introduced for low-power and high-performance systems applications [1][2][3][4][5]. Differential Cascade Voltage Switch Logic (DCVSL) is one of those. DCVSL has several advantages over the conditional CMOS static logic. First, DCVSL does not need a complementary pull-up network, thus the parasitic capacitances at the output node is reduced, which produces a faster response. Secondly, in contrast to pseudo-NMOS, its output voltages can swing from rail to rail and there is no direct current path between V_{DD} and ground in steady states. Finally it generates both true and complementary outputs, and an inverting stage can be eliminated and its performance is further improved[3]. However, these advantages are achieved at the expense of the extra area and complexity associated with dual logic networks including complementary signals.

In this paper, we propose Enhanced Differential Cascode Voltage Switch Logic (EDCVSL) that does not require complementary inputs. The proposed EDCVSL dramatically reduce the number of interconnects and simplify logic tree complexity while it reduces dynamic power and enhances the performance utilizing the dynamic current operation.

This paper is organized as follows. The second section gives an overview of the DCVSL circuitry. The proposed

EDCVSL circuitry is introduced in Section III. Section IV illustrates the implementation issues of EDCVSL and shows the comparison of simulation results to traditional DCVSL.

2. DCVSL OVERVIEW

The static version of Differential Cascode Voltage Switch Logic (DCVSL) is depicted in Fig.1(a). It is a differential style of logic that provides the complementary outputs with true and complementary inputs to the gate. When the inputs switch, nodes OUT and OUTB are pulled either high or low. This static version slowly transits and highly consumes current since the PMOS pull-ups fight the NMOS pull-down trees during the switching period.

To increase the performance and reduce the power consumption, many clocked versions of the DCVSL gate have been introduced. One of them is shown in Fig.1(b). Two complementary NMOS switch structures are constructed and connected to the cross-coupled PMOS pull-up transistors. OUT and OUTB are first precharged by setting CLK low. Once CLK goes high, NMOS logic tree determines the true output and its complement when the input signals are asserted, and either side is pulled down. The positive feedback applied to the PMOS pull-ups (M3 and M4) causes the gate to switch. The performance of the dynamic DCVSL gate is improved with the additional accelerating circuitry, M5 and M6.

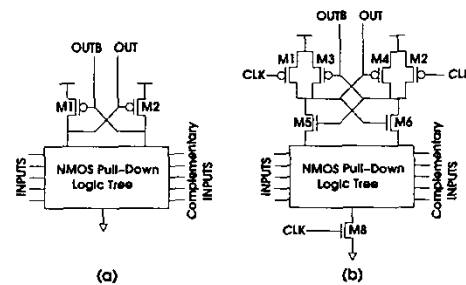


Fig. 1. DCVSL: (a)Static version, and (b)Dynamic version.

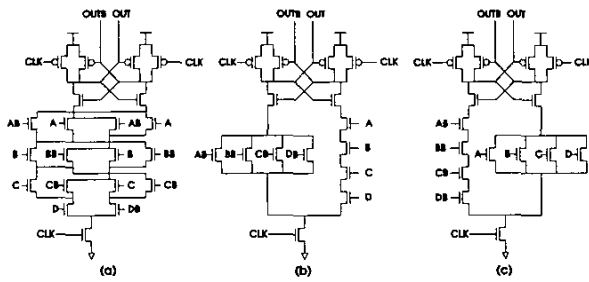


Fig. 2. 4-input DCVSL examples: (a)XOR-XNOR, (b)AND-NAND, and (c)OR-NOR.

The implementation of CMOS random logic with DCVSL has many advantages over the traditional static CMOS logic approach. First of all, DCVSL has the speed advantage of domino circuit. The reduction of the parasitic capacitances at the output nodes provides a faster response while static power consumption is eliminated. Second, this logic style allows both inverting and non-inverting logic gate implementation, making it a complete logic family while standard domino logic cannot implement inverting logic gates[2]. Third, DCVSL saves area by sharing the common transistors in the logic network for both of the outputs when a complex logic gate is designed. Several techniques have been proposed to minimize DCVSL trees such as an algebraic technique[6], an approach utilizing the Karnaugh map[3], and a modified method of the Quine-McCluskey method[3]. 4-input XOR circuit shows the shared logic tree in Fig.2(a) as an example.

On the other hand, these advantages are achieved at the expense of the extra routing, active area, and complexity associated with double-rail logic including complementary signals. Furthermore, if the true and complementary outputs have to be implemented using dual networks for primary gates such as NAND gate or NOR gate as shown in Fig.2(b) and (c), DCVSL cannot share logic tree transistors. Therefore, it is hard to implemented very high fan-in primary gates efficiently since a tall logic tree stack is required to produce dual outputs.

3. ENHANCED DIFFERENTIAL CASCODE VOLTAGE SWITCH LOGIC

In order to improve the DCVSL circuits, a couple of new versions of DCVSL has been studied. The first and the second versions of new DCVSL proposed in this paper are called EDCVSL Type I, and EDCVSL Type II, respectively. First, EDCVSL Type I schematic is shown in Fig.3. The operation of the EDCVSL is described as follows. During the low phase of the clock (CLK), the precharge transistors, M1 and M2 are turned ON to charge the output nodes to V_{DD} . Since the low phase CLK turns OFF M5 and M6, the DC

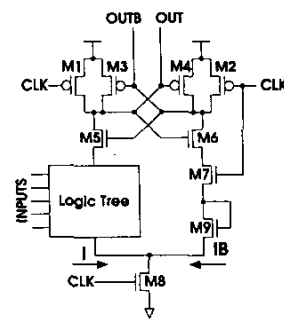


Fig. 3. Proposed EDCVSL Type I structure.

path from outputs to GND is eliminated. During the evaluation phase, the precharge transistors M1, and M2 are turned OFF, while transistor M7 and M8 are switched ON creating a current path from two precharged output nodes to GND through an EDCVSL logic tree depending on the input condition, and a diode (M9) works as a dynamic current source to limit the amount of charge transferred from one output node. Whichever the weaker current path, either the logic tree path or the diode path, is disconnected by the feedback of its complementary transistor (M5 or M6). The transistors M3 and M4 speed up the evaluation and maintain the logic levels. When the diode path is activated (OUTB is low), this diode raises the logic low level higher, but less than PMOS threshold voltage.

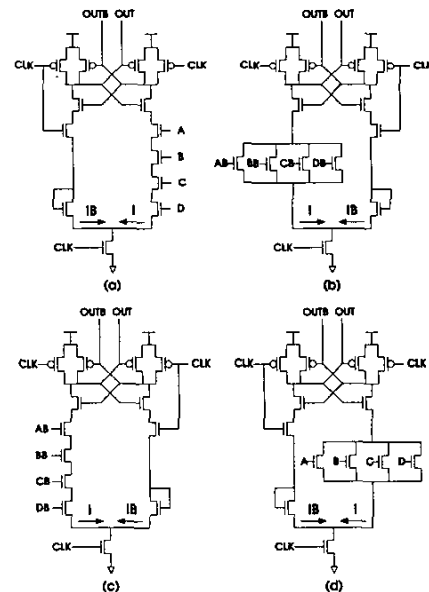


Fig. 4. 4-input gates of Type I: (a) AND-NAND series type, (b) AND-NAND parallel type, (c) OR-NOR series type, and (d) OR-NOR parallel type.

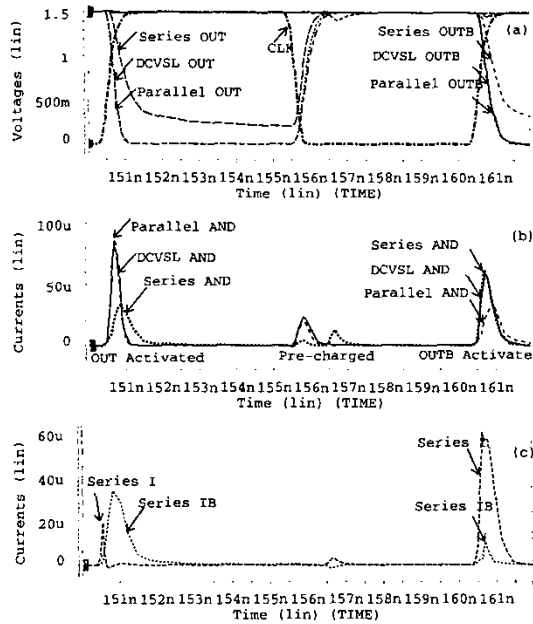


Fig. 5. Simulation results for EDCVSL Type I (Fig.5(a) and (b)) and conventional DCVSL (Fig.2(b)) 4-input AND-NAND gates: a) Voltage transient curves, b) Switching current curves, and c) I and IB path current curves in Fig.5a.

The current 'I' denotes the current activated by the EDCVSL logic tree, while the current 'IB' indicates the current provided by the transistor M9. When the input combination of EDCVSL logic tree provides any current path to GND, it supplies the larger current compared to that of the self-biasing current source (M9). When 'IB' is greater than 'I', in other words there is no DC current path to GND in the logic tree, OUTB voltage begins to fall faster than OUT voltage. Fig.4 shows the examples of the implementation of 4-input AND-NAND and OR-NOR gates.

Fig.5 shows the simulation results of Fig.4(a) AND-NAND EDVSL gate implementation using the true input signals (series logic structure) and (b) AND-NAND EDCVSL gate implementation using the complementary input signal (parallel logic structure). As shown in Fig.5(a), either OUT or OUTB has a slow transition than the other transition. Furthermore, it has a voltage drop due to a diode connection. Thus, it is clear that this scheme has asymmetric feature where one output is faster, the other is slower with much less power consumption due to small amount of current flow as shown in Fig.5(c). However, Fig.5.(b) demonstrates that ED-

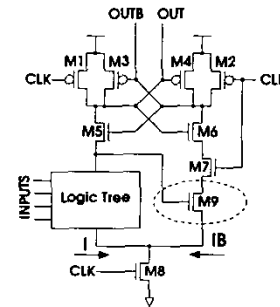


Fig. 6. Proposed EDCVSL Type II structure.

CVSL of Fig.4(a), series structure gate, requires less current flow compared with other styles such as traditional DCVSL (Fig.2(b)) or parallel EDCVSL (Fig.4(b)). In order to avoid this asymmetric problem, EDCVSL Type II is presented as shown in Fig.6. The transistor M9 is controlled by the intermediate output (the source node of M5) of the other rail which keeps "High" level when there is no DC current path in the logic tree, or "Low" level when any current path in the tree exists during the evaluation period. The simulation results are illustrated in Fig.7, where all the output signals are switching at very high speed.

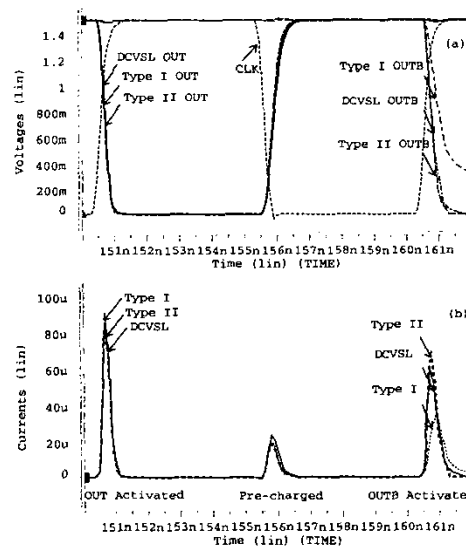


Fig. 7. Simulation results for DCVSL (Fig.2(b)), Type I (Fig.5(b)), and Type II: a) Voltage transient curves, and b) Switching current curves.

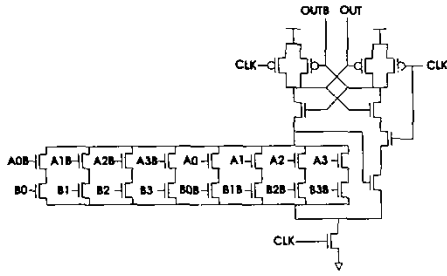


Fig. 8. Proposed EDCVSL Type II 4-bit comparator structure: Inputs A[3:0] and B[3:0].

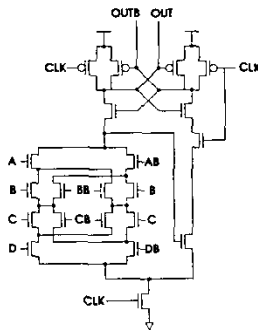


Fig. 9. Proposed EDCVSL Type II 4-input XOR-XNOR structure.

In addition, the outstanding advantage in both of the cases is that the proposed EDVSL gates reduce the number of interconnects and simplify logic tree eliminating the complementary input signals.

Since the charge-sharing of EDCVSL logic tree is proportional to the tree depth or width, the charge-sharing is not a significant problem at the output if the parallel structure is used for the evaluation logic tree. The proposed EDVSL can utilize only the parallel structure for the evaluation while the conventional DCVSL always requires both parallel and series structure. For example, the proposed EDVSL needs only one logic tree, parallel or series for 4-input AND-NAND as shown in Fig.4(a) and (b). Designers can select one of dual implementations to avoid any severe charge-sharing problem.

As shown in Fig.5, this style is very attractive when an encoding logic function is implemented. A 4-bit comparator circuit is shown in Fig.8 as an example. For any function with multi true outputs, such as 4-input XOR-XNOR, this merit is alleviated as shown in Fig.9, but EDCVSL still requires less transistor count compared to the conventional DCVSL logic tree in Fig.2(a).

Table 1. Comparison Results: EDCVSL Type I vs. DCVSL with Fan-out 4

	T(OUT)	T(OUTB)	I	EDP
Series AND	3.014	0.886	0.704	1.372
Parallel AND	0.892	1.977	0.999	1.433
Series OR	0.883	3.885	0.701	1.670
Parallel OR	1.867	0.988	0.991	1.414
EDCVSL XOR	1.064	2.061	0.941	1.470

Table 2. Comparison Results: EDCVSL Type II vs. DCVSL with Fan-out 4

	T(OUT)	T(OUTB)	I	EDP
Series AND	1.337	0.935	0.846	0.961
Parallel AND	0.882	0.876	0.974	0.857
Series OR	0.933	1.483	0.839	1.013
Parallel OR	0.909	1.003	0.960	0.918
EDCVSL XOR	1.088	0.929	1.040	1.048

4. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

To evaluate the performance of EDCVSL logic style, simple 4-input logic gates such as AND-NAND, OR-NOR, and XOR-XNOR were implemented with DCVSL, and EDCVSL using 1.5V 0.18 μm CMOS technology. All the transistors for the logic gates were optimized. And the simulations were performed at 100 MHz frequency. Delay and average current were measured at the typical corner. Table 1 and 2 shows the comparison results for EDCVSL Type I and II in terms of average current and Energy-Delay-Product (EDP), respectively. Both of the output was assumed to have fan-out 4 including local wire capacitance. All the results in these tables are normalized with respect to DCVSL results to simplify the comparison.

Since the current through the diode diminishes slowly, the particular high-to-low transition time becomes slow compared to the time of the other side. Therefore, EDP of Type I is not improved as much as Type II gate. The Type II improves the unbalanced delays of the Type I, and maintains the EDP of the conventional DCVSL while the complementary interconnects are eliminated. And the graphs in Fig.10 show the propagation delay and average current for five different AND-NAND gates as a function of output loads ranging from fan-out 1 to fan-out 5. The delay and EDP of the proposed EDVSL Type II gate are superior to those of the conventional DCVSL because the EDVSL reduces the circuit area and eliminates the interconnects for complementary signals in most of the cases.

5. CONCLUSIONS

In this paper, a new logic-style, EDCVSL is introduced for high performance and low power VLSI design. EDCVSL eliminates the complementary input signals, reduces the interconnects of the signals, and simplifies its logic structure. It was verified that EDCVSL Type II has less power consumption while it provides the higher performance compared to traditional DCVSL architecture.

6. REFERENCES

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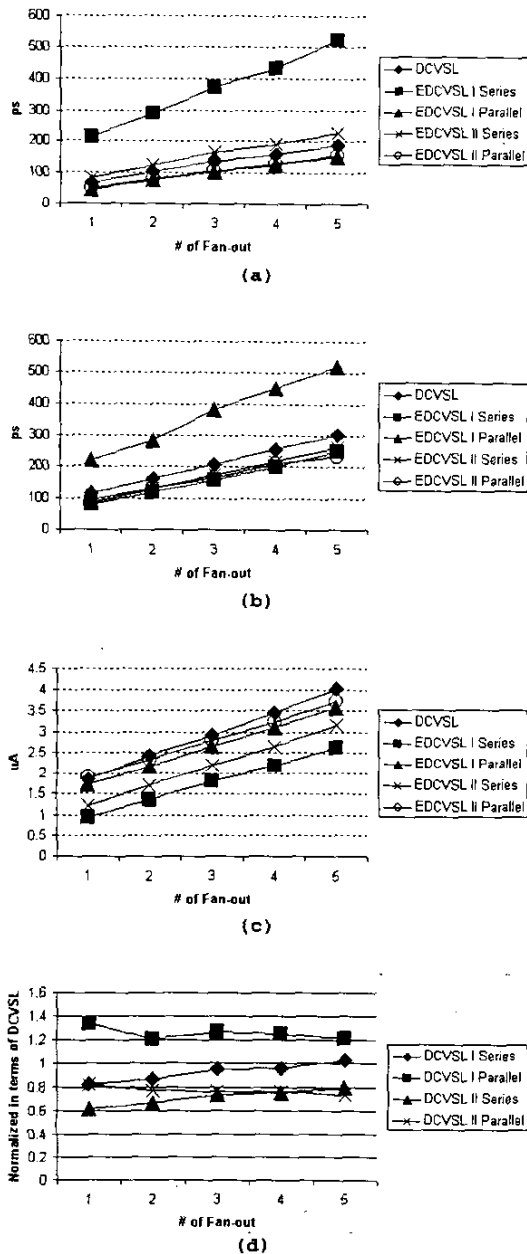


Fig. 10. The characteristic variations of DCVSL, EDCVSL I series & parallel, and EDCVSL II series & parallel with respect to fan-out: a) OUT transient delay, b) OUTB transient delay, c) Average current and d) normalized EDP in terms of DCVSL.