

Power Supply Network Aware Timing Analysis Using S-parameter In Nanometer Digital Circuits

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Abstract

This paper describes a novel technique to analyze the effects of supply voltage noise on circuit delay for nanometer VLSI circuits. Scattering parameters are used to analyze the power supply noise and to reduce runtime and memory usage. The interconnections of the power grid are modeled by RLC passive elements, constant voltage and time-varying current sources. A fast and accurate MOS modeling method for static timing analyzer is proposed based on the power grid analysis. MOS is modeled in three different regions during transition, and the maximum delay is formulated as a constrained non-linear optimization problem by considering the power supply noise (inclusive of the IR-drop and the Ldi/dt drop). The proposed technique has been applied to ISCAS85 benchmark circuits redesigned in 45nm technology. The results are compared to Hspice; they show that the error is within 5% of the Hspice simulation results.

Index Terms

IR-Drop, Ldi/dt, Power Supply Network, Power Supply Variation, Timing Variation, Cell Characterization.

I. INTRODUCTION

In Very-Deep-Submicron (VDSM) technology, the on-chip power-ground voltage variation significantly increases due to the IR-drop and the Ldi/dt noise. Reduction of the voltage drop in the power grid is a primary design challenge. The large current consumption across long power lines with parasitic impedance

causes low and/or unstable voltage levels on the grid. This affects performance and can cause circuit failure due to the increased delay as result of the lowered supply. The voltage drop also causes a smaller effective threshold voltage (resulting in an increased sensitivity to noise)[1][2].

With the aggressive scaling of VLSI circuits, the analysis of power grids has become a necessary step in VLSI design. However, a detailed analysis of the power grid is computationally intensive due to the distributed and dispersive nature of the grid. A large number of internal nodes or RLC elements in a power grid usually overwhelms a circuit simulator. Furthermore, a power grid suffers from Ldi/dt noise as VLSI systems go beyond several GHz and power supply currents increase; this requires special techniques such as on-chip decoupling capacitors or regulators to provide a stable supply voltage. To implement an efficient and accurate modeling and simulation method, a distributed RLC network and frequency-dependent parameters are required for the power grid. The scattering parameter(S-parameter) is a promising alternative to overcome the above issues and to satisfy requirements because it is well suited for characterizing and modeling power networks at high frequency [3]-[6]. The sensitivity of the supply voltage variation to the supply current is developed at the block level based on the model. In this paper, a S-parameter based macromodel for the power grid is proposed. At transistor-level, the sensitivity of voltage variations to the block currents is established based on the model.

The results of the power grid analysis must be also utilized in the timing analysis for accuracy. Gates with different voltage levels that communicate with each other across the chip, can propagate erroneous data, thus causing a malfunction. Gate delays increase non-linearly as the voltage at a logic gate decreases. The increase in gate delay due to the voltage drop on the datapath can ultimately lead to setup time error. Moreover, the supply voltage drop on the buffers and inverter cells of the clock path may cause the clock signal arrival time to be different thus resulting in a clock skew and hold time error. Due to the voltage drop and related signal-integrity effects, traditional timing analysis methods often provide inaccurate results. Timing analysis in nanometer technology requires a comprehensive design flow that accounts for the interactions between power supply noise and signal-integrity timing effects using both accurate parasitic data and detailed models. For example, conventional timing analysis methods assume global supply voltage drops in the range of 2 to 5%; they then re-run the delay calculation to determine the IR-drop effects in a design. However, this approach applies the same supply voltage to all gates in the design and typically provides rather pessimistic results. The IR drop on timing has a nonlinear effect with supply voltage.

Therefore, the use of static timing analysis with a simple linear derated supply voltage cannot correctly identify the setup and hold-time errors caused by IR drop related factors [7]-[10]. In this paper, a new fast

and accurate MOS modeling method for a static timing analyzer is proposed. For fast timing analysis, the modeling method uses the non-linear MOS model, and the circuit maximum delay is formulated as a constrained non-linear optimization problem by considering the power supply noise (including IR-drop and Ldi/dt drop).

II. CHARACTERIZING AND MODELING FOR POWER GRID

Power-ground distribution has been a challenge for high speed VLSI design because 10% supply voltage variation may cause more than 10% timing uncertainty. Voltage drop has two aspects. The first is often referred to as the DC IR drop; this is a result of the power lines' resistance and the current drawn from the power and ground grids. A large current can cause transistors to see lower voltage levels than intended. If the wire resistance is too high or the current is larger than predicted, an unacceptable voltage drop may occur. Circuit design in the nano scale is extremely susceptible to the voltage drop because power and ground wire resistivities increase with decreasing geometries and the overall power supply voltage decreases. This results in poor performance and increased noise susceptibility. This problem cannot be entirely solved by raising the value of Vdd because the power supply voltage level is different from point to point.

The voltage drop can also be transient due to fluctuations in local or global current demand and the capacitive (and inductive, if the frequency is sufficiently high) nature of the loads. In a synchronous chip, a system-wide clock may typically switch thousands of transistors at the same time causing current surges that further reduce the supply seen by the gates. This phenomenon is called Simultaneous Switching Noise(SSN). On/Off-chip decoupling capacitors are typically used to smoothen these transients [1][2].

The power grid is typically implemented using the top two metal layers. Grid lines on the same layer are in parallel, while grid lines on the two different layers are orthogonal. The end nodes of grid lines on each layer are connected via metal contacts. One end of the contact is connected to the current source that represents the logic block.

The supply voltage on this node provides the current to the logic blocks. A simple RLC distributed wire model is commonly used to model a grid structure. The whole grid structure is composed of grid elements; each grid element is a segment of a wire connecting two nodes. A RLC model is established for each grid element. Figure 1(a) shows the basic model of the power supply network that consists of the VDD and GND grids. Each grid is effectively a large mesh structure shown in Figure 1(b). The edges of the grids are connected to time-varying current sources. Modeling of the time-varying power supply voltage and current calculation of logic blocks are very difficult and time consuming due to the

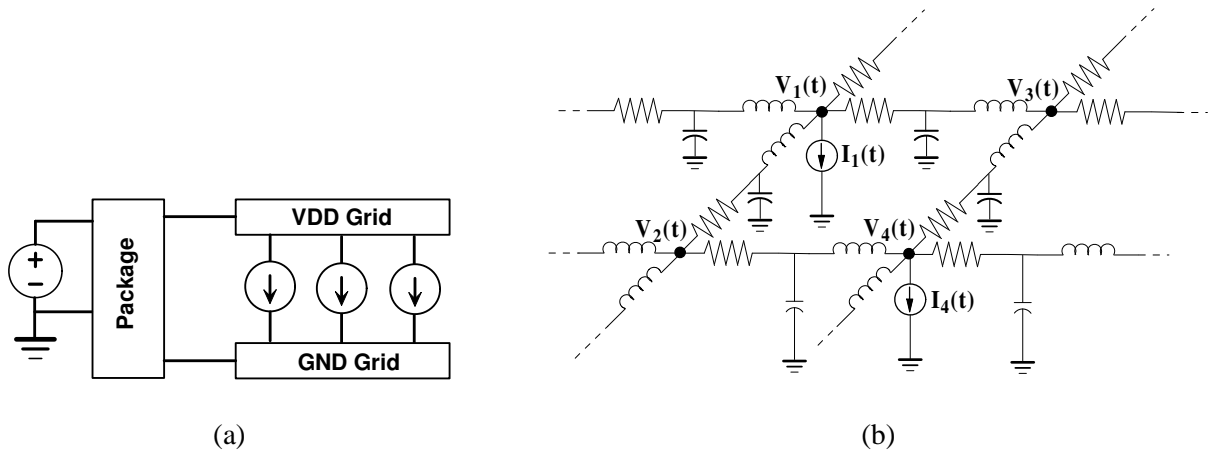


Fig. 1. Traditional power grid model, (a) Power supply network, (b) VDD/GND grid model

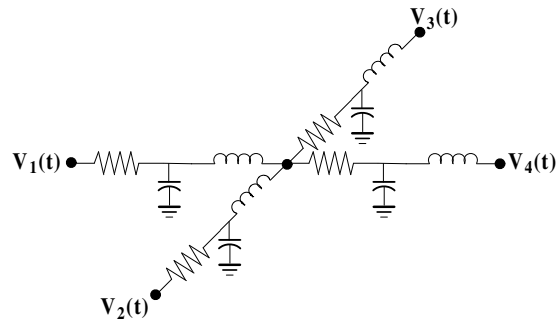


Fig. 2. A representative node in the power grid

many simultaneous switching logic blocks and the parasitic elements. For an efficient analysis and fast simulation of the power grid, this paper proposes a signal flow graph using S-parameter analysis.

In Figure 2, the grid model has 4-port inputs and 4-port outputs and can be characterized by a 4×4 scattering matrix as follows (all ports can be used as both input and output)

$$\begin{pmatrix} port1 \\ port2 \\ port3 \\ port4 \end{pmatrix} = \begin{bmatrix} s_{11} & s_{12} & s_{13} & s_{14} \\ s_{21} & s_{22} & s_{23} & s_{24} \\ s_{31} & s_{32} & s_{33} & s_{34} \\ s_{41} & s_{42} & s_{43} & s_{44} \end{bmatrix} \times \begin{pmatrix} port1 \\ port2 \\ port3 \\ port4 \end{pmatrix} \quad (1)$$

Scattering parameters are a powerful method to describe and model the interconnection network. They

can be measured at high frequency and exist for all distributed-lumped circuit elements, including open and short circuits. Moreover, the parameters describe transmission lines that are critical for interconnect analysis in high speed design. A scattering matrix is employed to relate the outgoing waves to the incoming waves of a multi-port circuit [12]. Each S-parameter can be obtained from the measured S-parameter in Hspice, or the calculated S-parameter from the Z-parameter of a single interconnection model [11]. For an N-port component, the S-parameter matrix can be defined as

$$S_{ji}(s) = \left. \frac{b_j}{a_i} \right|_{a_k=0, k \neq i} \quad i, j = 1, 2, \dots, n \quad (2)$$

where s is the complex frequency, a_i and b_j are the incoming voltage wave at port i and the outgoing wave at port j , respectively.

Based on the basic grid element and a single interconnection model, the total power grid is partitioned as shown in Figure 3, in which each Power Network(PN) is the basic model for the power grid of Figure 2. On the assumption that PN1 and PN2 are connected to logic blocks as output loads, then all the S-parameters of other PNs are calculated using signal flow graphs [13]. By considering PN1 and PN2, the calculated S-parameters of other PNs are effective the S-parameters for the whole power network. Once the effective S-parameters are calculated, Hspice can easily simulate PN1 and PN2 and measure the voltage drops at each logic block because other PNs are considered as a large block (as simplified by the S-parameters).

The so-called Mason's signal flow graph can be applied to the S-parameter networks. Assume that the network has two ports, then the graph is shown in Figure 4, where Γ_S and Γ_L are the source and load reflection coefficients. Using this graph, the transmittance of the network is calculated and it is given by

$$\frac{b_1}{a_1} = \frac{1}{\Delta}(P_1\Delta_1 + P_2\Delta_2) = \frac{S_{11}(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L}{(1 - S_{22}\Gamma_L)} \quad (3)$$

where a_1 is the source node and b_1 is the sink node, the loop transmittance(L_1) = $S_{22}\Gamma_L$ and $\Delta = 1 - L_1 = 1 - S_{22}\Gamma_L$. The path transmittances is given by $P_1 = S_{11}$ and $P_2 = S_{21}\Gamma_L S_{12}$. If Δ_i is the value of Δ for the portion of the graph not incident on the i th forward path(P_i), then $\Delta_1 = 1 - S_{22}\Gamma_L$ and $\Delta_2 = 1$.

Few rules can be used to simplify the graph.

- The serial paths in the graph are represented by multiplying the weight of the paths.
- The branches joining common nodes are represented by adding the weight of the branches.

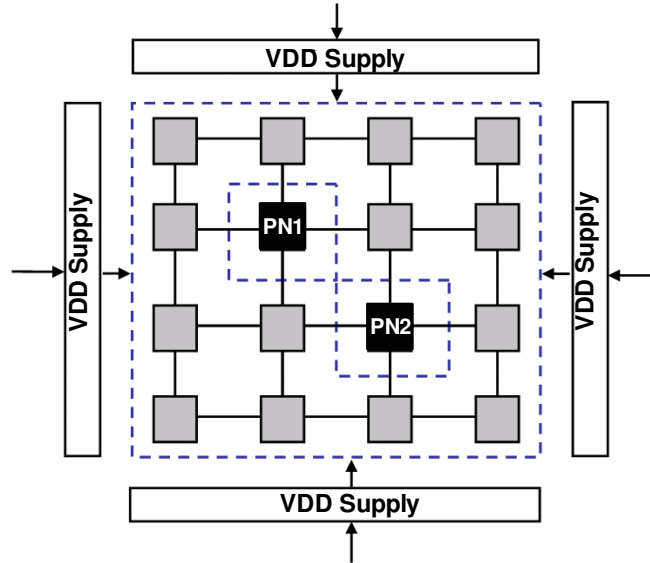


Fig. 3. Partition method for the power grid

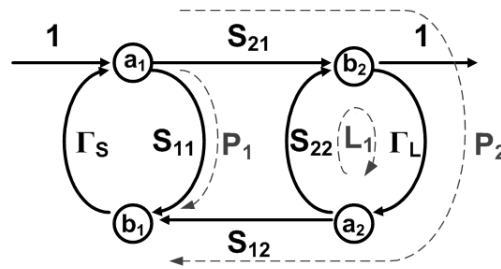


Fig. 4. Mason's signal flow graph of a two port network

- The loop can be removed by dividing the weight of every other edge entering the node by $\{1 - (\text{the weight of the loop})\}$.

The proposed simulator consists of interface programs to Matlab, Hspice, and C as shown in Figure 5. The S-parameters from the four port RLC model are extracted by Hspice, and the extracted S-parameters are added to the lookup table in Matlab. Once the lookup table is generated, the whole signal flow graph based on the output load locations is generated. Except for the power networks connected to any active circuit, the macro power network (that contains the power network under consideration and every neighboring power networks) is generated in Matlab. Finally, Hspice simulates the macro-networks that

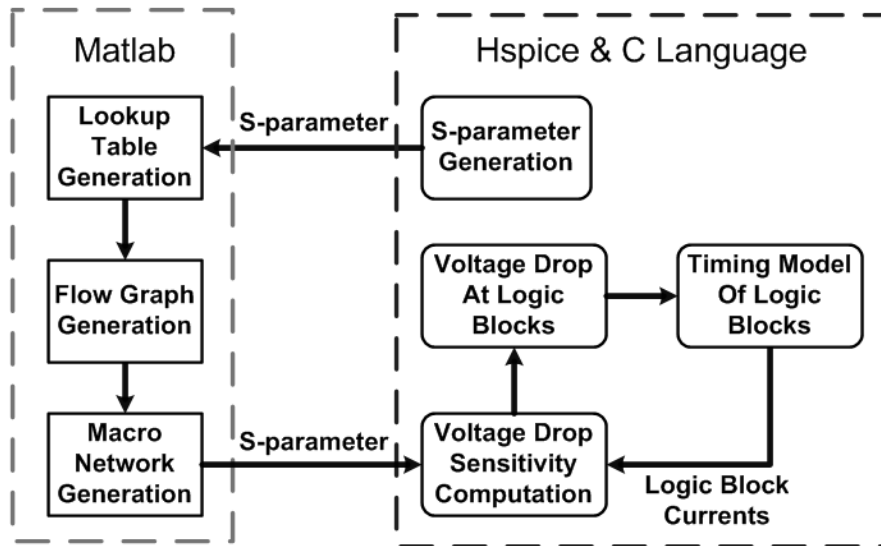


Fig. 5. Block diagram of the proposed simulation method for the power grid

contain the power networks and circuit blocks; it also calculates the voltage drop at the logic blocks by considering the gate currents obtained from the timing models developed in the following section. If only the voltage drop is calculated, the logic block currents are changed based on the calculated voltage drop within the local and global current constraints. The above final procedure is repeated until the worst-case delay is found.

III. GATE DELAY MODEL FOR VOLTAGE VARIATION

In this section, a gate delay model is developed by considering power supply variations obtained from simulation to investigate its impact on gate delay. Figure 6 shows an inverter with modeling parameters; the input is assumed to rise from V_{IL} to V_{IH} . The output of the inverter falls from V_{DD} to V_{SS} . Consider the variation range of the power supply voltage. For the circuit to function properly, the transistors must be able to turn OFF; this sets the upper limit on the supply voltage variation. It is necessary that $|V_{SS} - V_{IL}| < V_{tn}$ and $|V_{IH} - V_{DD}| < |V_{tp}|$. In the worst case, if the opposite variations for (V_{SS}, V_{IL}) and (V_{IH}, V_{DD}) are considered, then

$$|\Delta V_{SS}| + |\Delta V_{IL}| < V_{tn} \Rightarrow \text{roughly, } |\Delta V_{SS}| < \frac{V_{tn}}{2} \quad (4)$$

$$|\Delta V_{DD}| + |\Delta V_{IH}| < V_{tp} \Rightarrow \text{roughly, } |\Delta V_{DD}| < \frac{V_{tp}}{2} \quad (5)$$

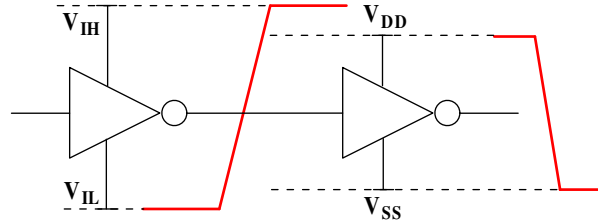


Fig. 6. Inverter with modeling parameters

Equations (4) and (5) set the limit of the tolerable supply voltage variation. In this paper, for simulation 45nm CMOS technology is used with a 1.0V supply voltage.

To develop a timing analysis in the presence of power supply and ground voltage variations, an accurate delay model that dependent on these voltage variations is required beforehand. A traditional delay model utilizes two dimensional tables with entries representing delay and transition times for a specified input transition time. In addition for aggressive scaled devices, the gate delay depends on the input (high and low levels) the power supply and ground of the gate, its output load as well as the input slope [7]-[10]. It is rather complex to develop a timing model considering all these parameters. For simplification in this paper, a non-linear MOSFET model is developed for the three different timing regions during a gate transition.

Digital gate circuits are reduced to a single NMOS transition and a capacitor; the following differential equation describes the charging events [14].

$$C_{Load} \frac{dV_{out}(t)}{dt} = I_{out}(t) \quad (6)$$

However, it is too complicated to derive the current equation of a non-linear device. In Figure 7, the output current waveform is divided into three different timing windows. In region 1, the output current starts to flow through the MOSFET device and increases suddenly. In region 2, a high current flows because both th NMOS and PMOS are turned on and there is little current increase. In region 3, the output current decreases suddenly because the output capacitor is fully charged and finally the current stops flowing. In these three regions, the output current can be modeled as follows.

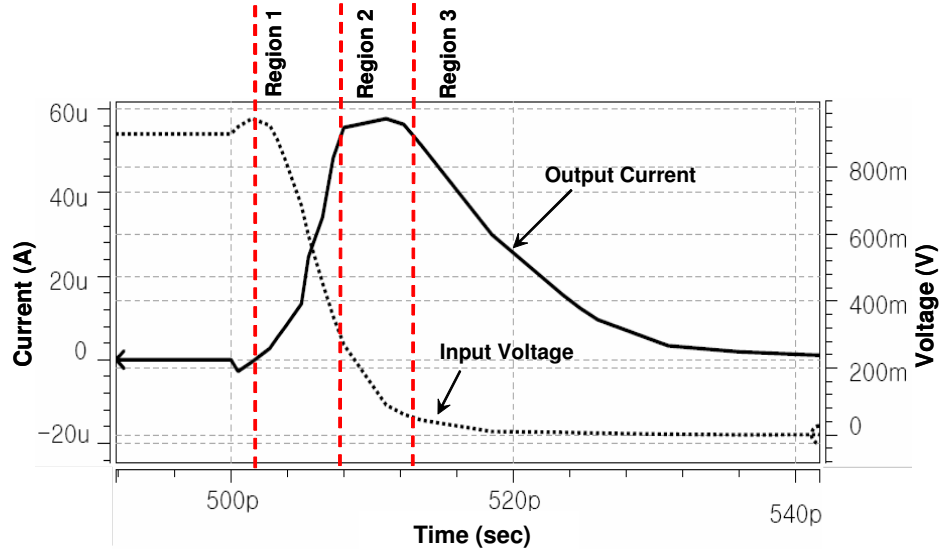


Fig. 7. Current waveform of inverter

Region 1:

$$I_{out}(t) = \frac{V_{IN}(t/T_{IN}) - V_{TH}}{R_M} \quad (7)$$

Region 2:

$$I_{out}(t) = \frac{V_{IN} - V_{TH}}{R_M} \quad (8)$$

Region 3:

$$I_{out}(t) = \frac{V_{OUT}(t)}{R_F} \quad (9)$$

where T_{IN} is the transition time of the input signal, and R_M and R_F are the effective resistances of the MOSFET. V_{IN} , V_{OUT} , and the effective resistances depend on the power supply noise.

From equation (6) with (7), (8), and (9), the output voltage(V_{OUT}) is calculated.

Region 1:

$$V_{out}(t) = V_{dd} - V_{IN} \frac{(t - t_v)^2}{2R_M C_L T_{IN}} \quad (10)$$

Region 2:

$$V_{out}(t) = V_{dd} - \frac{(V_{IN} - V_{TH})(2t - T_{IN}(1 + V_{TH}/V_{dd}))}{2R_M C_L T_{IN}} \quad (11)$$

Region 3:

$$V_{out}(t) = \left[V_{dd} - \frac{(V_{IN} - V_{TH})(2t - T_{IN}(1 + V_{TH}/V_{dd}))}{2R_M C_L} \right] \exp\left(\frac{t_s - t}{R_F C_L}\right) \quad (12)$$

where t_v is the rising time to the threshold voltage and is given by $t_v = T_{IN} \times V_{TH}/V_{dd}$, t_s is the time boundary of region 2 and region 3.

From equations (10), (11), and (12), the signal delay is calculated as follows.

$$0 < T_d < T_{IN}$$

$$T_d = t_v + \sqrt{2R_M C_L T_{IN} \Delta V_{OUT}} \quad (13)$$

$$T_{IN} < T_d < t_s$$

$$T_d = \frac{T_{IN}(1 + V_{TH}/V_{dd})}{2} + \frac{R_M C_L \Delta V_{OUT}}{1 - V_{TH}/V_{dd}} \quad (14)$$

$$t_s < T_d$$

$$T_d = t_s + R_F C_L \ln\left(\frac{R_M C_L - (1 - V_{TH}/V_{dd})(2t_s - T_{IN}(1 + V_{TH}/V_{dd}))}{2R_M C_L(1 - \Delta V_{OUT})}\right) \quad (15)$$

These delay equations reduce the static timing analysis, and its accuracy is within 5% error comparing to Hspice simulation result. The effective resistances must be generated in advance depending on the input transition time, the output load; resistance values are saved in a two-dimensional table. Delay is estimated using a bilinear interpolation based on the table. For the voltage variation, the sensitivity of the effective resistance to supply voltage is calculated at the same time. Using sensitivity, the effective resistance is updated according to the voltage variation to provide a more accurate timing delay. For complex gate circuits, the timing delay calculation through stages is the same as for the inverter.

Based on the delay model, the propagation delay is estimated with a small error. For signal propagation an output waveform is generated using an input waveform; the input is linear and generates linear output waveform as shown in Figure 8. the input transition time(T_{IN}) is approximated from equation (11) as follows.

$$T_{IN} = \frac{V_{dd} R_M C_L}{(V_{IN} - V_{TH})} \quad (16)$$

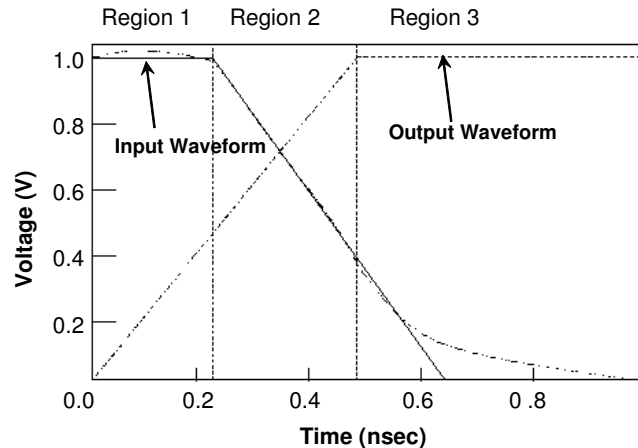


Fig. 8. Approximation of output response

Using both the signal equation and the input transition time, the propagation from the primary inputs to the primary outputs is obtained.

IV. COMBINING THE POWER GRID MODEL AND THE GATE DELAY MODEL

For calculating an accurate propagation delay for the MOSFET circuits, the sensitivity of voltage variations to the block current must be investigated at gate level in the block. Therefore, the simplified linear model of the power supply network is considered as a linear system with time-varying currents as inputs and time-varying voltage as outputs; this is shown in Figure 9(a). If the power grid is a network with two port S-parameters, the transfer function ($H(S)$) is derived from Mason's signal flow graph as shown in Figure 9(b); this is given by

$$H(S) = \frac{\frac{a_2}{B_s} + \frac{b_2}{B_s}}{\frac{a_1}{B_s} + \frac{b_1}{B_s}} = \frac{S_{21}(1 + S_0)}{1 + S_{11} + S_0(S_{12}S_{21} - S_{11}S_{22} - S_{22})} \quad (17)$$

where S_0 is the S-parameter of the output load.

As shown in Figure 10, the $H(s)$ function can be generated by the method presented in Section II. After obtaining the voltage drop at the supply points (as a linear function of the block current), the

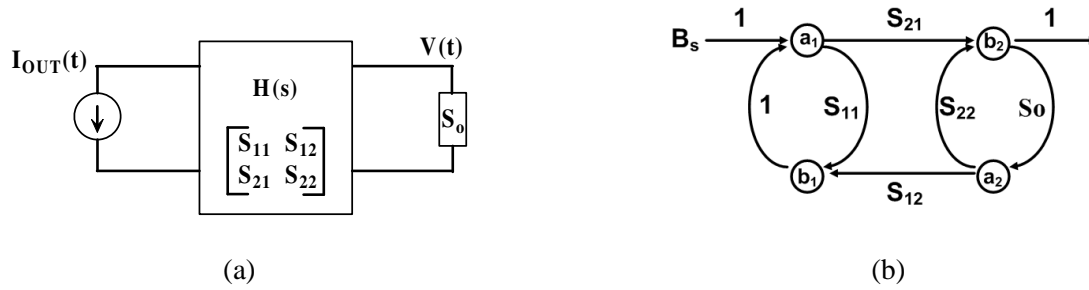


Fig. 9. Power grid model as a linear system, (a) A two port network, (b) Mason's signal flow graph

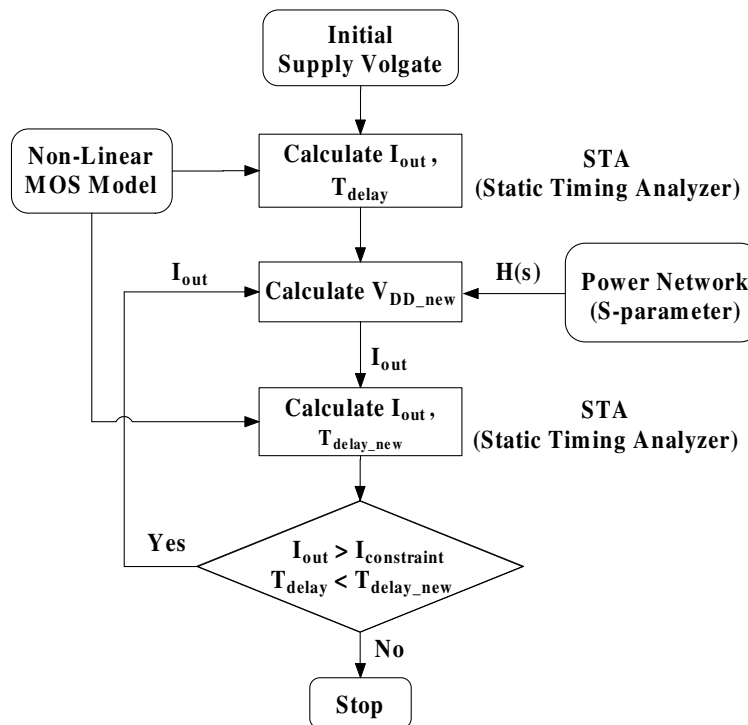


Fig. 10. Overall flow of the proposed method

current of the logic blocks is updated using equations (7), (8), and (9). After finding the new value of the current, the voltage drop at the supply point is updated by the $H(s)$ function. The procedure is repeated until the local and global constraints of the block currents are satisfied, and the final voltage drop and current value are obtained. The propagation delay is estimated by utilizing the proposed timing analysis method and the final supply voltage.

V. EXPERIMENTAL RESULTS

The proposed S-parameter based simulator for clock grid and timing analysis has been implemented in Matlab and C; the simulation was run on a 500MHz UltraSPARC-IIe with 500Mbyte memory. The proposed procedure has been evaluated using the ISCAS85 benchmark circuits. Each benchmark circuit has been redesigned in a 45nm CMOS technology and the look-up table has been generated for random input variables. The variables have been generated 50 times by Monte Carlo simulation in Hspice to obtain the average delay for the voltage variations. The primary inputs are characterized by a Gaussian distribution.

In [11], the wire capacitance is the average of all the interlayer capacitances while the wire resistance is the sheet resistance times the ratio of its length and width. Table I shows the computational time for the power grids (wire width = $0.045\mu m$) with 1320 to 27055 nodes using Hspice and the proposed method. The (simulated) execution time of the proposed method is faster than Hspice by a factor of at least 12 folds.

TABLE I
EXPERIMENTAL RESULTS FOR SIMULATION TIME

# of Grid Nodes	# of Blocks	CPU time (sec):Hspice	CPU time (sec):Proposed Method
1320	12	87.34	5.03
3772	12	200.45	5.12
5832	12	750.94	12.34
10073	20	2707.68	20.63
27055	20	2810.24	225.63

Table II shows the summary of the propagation delay performed with a power grid simulation to consider supply voltage variation. The eighth column is the error between the Monte Carlo simulation and the proposed approach. The delay is estimated at a confidence level of 97% for the Monte Carlo simulation; the accuracy of the proposed method is within a 5% difference compared with Hspice (Monte Carlo simulation). In addition, the simulation time of the proposed method is faster than the Monte Carlo simulation by at least a factor of 1000.

VI. CONCLUSION

This paper has proposed a novel technique for analyzing the effect of supply voltage noise on the delay of nanometer VLSI circuits. The proposed method considers both the IR and Ldi/dt drops in the power

TABLE II
EXPERIMENTAL RESULTS FOR PROPAGATION DELAY

Circuit	# of gates	# of Grid Nodes	Monte Carlo Simulation		Proposed Method		error(%)
			CPU time (sec)	Delay (psec)	CPU time (sec)	Delay (psec)	
C432	160	652	7451.23	162	10.04	164	1.22
C499	202	652	10121.45	132	13.32	138	4.30
C880	383	1320	22450.34	185	31.43	180	2.70
C1355	546	1320	22012.67	199	50.31	209	4.80
C2670	1193	1320	4915.98	312	400.64	320	2.50
C3540	1669	5832	6454.12	425	600.74	435	2.30
C5315	2307	5832	8312.87	300	800.14	316	3.40

supply network by modeling the logic block with a time varying current source. This new model and the corresponding analysis and methodology for power grid use scattering parameters to reduce the simulation runtime and memory utilization. Along with the power grid analysis, a method for logic propagation delay has been presented; it uses different MOS models for the three regions of signal transition. Based on the MOS model, the circuit maximum delay is formulated as a constrained non-linear optimization problem by considering the power supply noise (including the IR-drop and Ldi/dt drop). The proposed technique has been applied to the ISCAS85 benchmark circuits redesigned in 45nm technology. Its results are compared to Hspice. They show that the error is within 5% compared with the Hspice simulation results. The proposed methodology can be used in power distribution design and power supply aware timing analysis for nanometer VLSI circuits.

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Yong-Bin Kim was born in Seoul, South Korea in 1960. He received the B.S. degree in Electrical Engineering from Sogang University in Seoul, South Korea in 1982, the M.S. degree and PH.D both in Computer Engineering from New Jersey Institute of Technology and Colorado State University in 1989 and 1996, respectively. From 1982 to 1987, Dr. Kim was with Electronics and Telecommunications Research Institute in South Korea as a Member of technical Staff. From 1990 to 1993 he was with Intel Corp. as a Senior Design Engineer, and involved in micro-controller chip design and Intel P6 microprocessor chip design. From 1993 to 1996 he was with Hewlett Packard Co., Fort Collins, Colorado as a Member of Technical Staff, and involved in HP PA-8000 RISC microprocessor chip design. From 1996 to 1998 he was with Sun Microsystems, Palo Alto, California as an individual contributor, and involved in 1.5GHz Ultra Sparc5 CPU chip design. From 1998 to 2000, he was an assistant professor in the Dept. of Electrical Engineering of University of Utah. He is currently Zraket Endowed Professor in the Department of Electrical and Computer Engineering at Northeastern University. His research focuses on low power analog circuit design, high speed low power VLSI circuit design and methodology.



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