

A Digital-Trim Controlled On-Chip RC Oscillator

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Abstract – In this paper, a high-accuracy RC Oscillator (OSC) circuit is demonstrated using trimming control. The OSC uses a 7-bit binary-weighted resistor array as the trimming object. Using a $0.5\ \mu\text{m}$ CMOS process, the final output frequency can be achieved within $\pm 0.5\%$ error while the original OSC without trimming has as much as $\pm 40\%$ output variation due to process variations. Temperature variation and power supply variation are also considered and resolved. Detailed circuit design and SPICE simulation results are presented. The final die size of the test chip is $130\ \mu\text{m} \times 145\ \mu\text{m}$ excluding bonding pad.

I. Introduction

High-accuracy internal clock is very important for synchronization among the independent cells in VLSI circuits. Many oscillator circuits have been studied and published so far. The most common one is the crystal oscillator. However, crystal can not be built in a tiny chip and its usage is much limited by its size. Many other RC circuits, like canonic RC-active frequency oscillator^[1], Novel RC Oscillator^[2], and single-resistance-controlled oscillator,^{[3][4]} need an op-amp to stabilize the oscillating frequency. However, building a high gain op-amp is complicated and expensive. Moreover, there exists the problem of inaccurate op-amp input offset, which also needs to be compensated.

The trimmed OSC circuitry presented in this paper is inexpensive and reduced the degree of design difficulty. The system block diagram is shown in Fig. 1. By trimming the resistor array in the RC oscillator, the frequency errors caused by the process variations can be compensated efficiently and accurately.

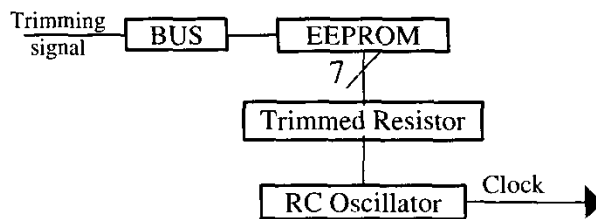


Fig. 1 System Block Diagram

The 7-bit digital trimming control signals are imported through a bus and then written to an EEPROM that finally provides the trimming signals.

The basic RC-Oscillator circuitry design and the simulation results are described in Section II. The trimming resistor array design methodology is explained in Section III while the design issues related with temperature variation are given in Section IV. Section V illustrates the final simulation results and die photo. The application with EEPROM is briefly introduced in Section VI. Finally the conclusion is given in Section VII.

II. Basic RC OSC Circuitry Design

The basic RC OSC circuit is divided into two parts, a current generator and a wave generator as shown in Fig. 2. The current generator is a kind of current mirror whose current is controlled by a resistor. The wave generator uses a switch to control the charging and discharging function of the capacitance to generate a triangular wave (as in Fig. 3). Then the triangular curve is reshaped to spike by the inverters which feed to the input of DFF (D flip-flop). Finally the wave (Vout) from DFF will be the rectangular waveform with half frequency of the triangular waveform. The final output frequency of the OSC is 2MHz according to the design specification. The design details are explained step by step as following.

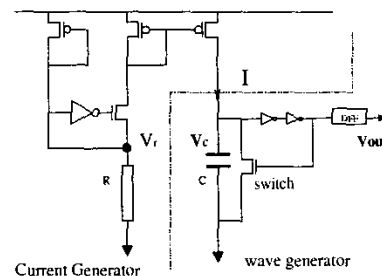


Fig. 2 Basic RC Oscillator

For the wave generator part, with the assumption of constant current into the capacitor, the voltage of the capacitor, V_c , will increase in proportional to the current. That is:

$$\Delta V_c = \frac{I \times \Delta t}{C} \quad (1)$$

Meanwhile the voltage of the capacitor, ΔV_c , is also controlled by the logical threshold voltage of the inverter which will turn on the low-impedance NMOS switch to quickly discharge the capacitor to zero voltage. The discharging time is so small that it can be ignored comparing to the charging time. At last a triangular voltage waveform (as in Fig. 3) will be generated for the capacitor and the period time for one cycle of charging and discharging will be:

$$T_c = \Delta t = \frac{C \times \Delta V_c}{I} \quad (2)$$

For the current generator part, a constant current source is built using current mirror. A feedback circuit always stabilizes the voltage above the resistor denoted as V_r . So the resistance will decide the current, that is:

$$I = \frac{V_r}{R} \quad (3)$$

Replacing the current expression into the equation (2), we get:

$$T_c = \Delta t = \frac{C \times \Delta V_c}{\frac{V_r}{R}} = RC \times \frac{\Delta V_c}{V_r} \quad (4)$$

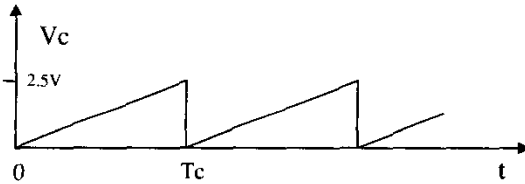


Fig. 3 Waveform Above Capacitor

The advantage of this circuit is now shown by equation (4), that is, the output clock time period is proportional to R and C . No matter where the integrated error comes from, an accurate output period/frequency can always be achieved if the resistor or capacitor can be adjusted linearly.

The important factor is that the final output clock period is two times of the T_c shown in equation (4) due to the DFF. That means period/frequency of the V_c in Fig. 3 should be $250\text{ns}/4\text{MHz}$ if 2M Hz final output frequency is the target. Since period is proportional to the product of R and C , which is convenient for calculation, period will be used instead of frequency in later calculations.

The sizes of the resistor, capacitor and transistors are calculated and the simulation result is shown in Fig. 4. The OSC output clock is shown in the first wave, the second waveform is the spike at the output of the last inverter and the last form is voltage on the capacitor, with the same shape as the one in Fig. 3.

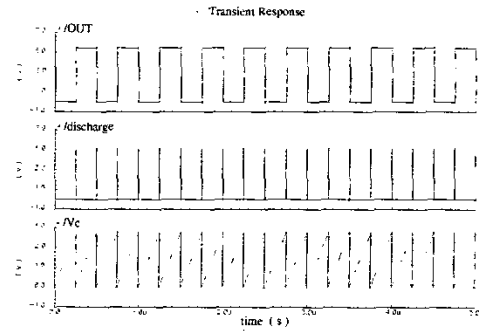


Fig. 4 Output Waveforms From Simulation

III. Trimming Resistor Array Design

Before the trimming resistor array design, the process variation needs to be defined. Using SPICE to simulate both the fastest corner and slowest corner, we got the range of process variation. The simulation result shows the variation of output period is -34% at fastest corner and 42% at the slowest corner. Hence, about $\pm 40\%$ error variation needs to be covered by the trimming design.

From the equation (4), it can be seen that controlling R or C is the key to get an accurate frequency output since ΔV_c and V_r are always near constant. Of course the high accuracy can be achieved by trimming both R and C , but it's not necessary. Due to the VLSI process, the area of a capacitor is much larger than that of a resistor, so only the resistor will be trimmed while the capacitor keeps unchanged. A binary-weighted resistor array is built for trimming. The structure is very simple as shown in Fig. 5. NMOS switches are used as the controlling bits.

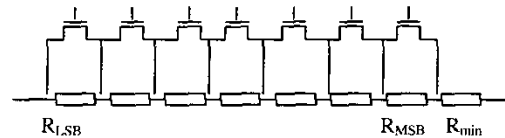


Fig. 5 Binary-Weighted Resistor Array

From the simulation results, we know the resistance variation should cover $\pm 40\%$ as shown in the following equations, where R is the theoretical value:

$$R_{\max} \cdot (1 - 40\%) \geq R = 200\text{K}\Omega \quad (5)$$

$$R_{\min} \cdot (1 + 40\%) \leq R = 200\text{K}\Omega \quad (6)$$

From equation (5) and (6), we get:

$$R_{\max} = 333.5\text{K}\Omega \quad R_{\min} = 143\text{K}\Omega$$

$$\Rightarrow \Delta R = 190.5\text{K}\Omega$$

For 7-bit resistor array:

$$R_{L\text{SB}} = 1.5\text{K}\Omega \quad R_{M\text{SB}} = 96\text{K}\Omega$$

$$R_{L\text{SB}}(1 + 40\%) / R = 1.05\%$$

Using 7-bit binary-weighted resistor array, the 1.05% LSB adjustment is enough for $\pm 0.53\%$ error trimming. In the resistance array design, we have also considered the limitation of both the transistor process in VLSI and the switch impedance.

Since the switches are working in their linear region, the impedance of the designed large NMOS switch is about $150\ \Omega$ which is small comparing with the designed resistances. For the $0.5\ \mu\text{m}$ process, the square sheet resistor value is $1\text{k}\Omega$. To minimize process variation for the resistor and get the smallest area of the layout, the resistance of LSB is best around $1\text{k}\Omega$. Combining all those factors, the LSB value of the resistor array is $1.5\text{k}\Omega$.

IV. Temperature Variations

Although we designed trimming resistor array to eliminate the process variation, temperature and voltage variations must also be considered. Without temperature compensation design, the simulation results for the circuit in Fig. 2 are shown in table 1.

V(volt)	T (°C)	Period (us)		Frequency (MHz)	
5	0	0.530	5.99%	1.887	-5.65%
5	80	0.439	-12.20%	2.278	13.90%
4.5	27	0.495	-0.99%	2.020	1.00%
5.5	27	0.503	0.50%	1.990	-0.50%

Table 1 Temperature and Voltage Variations

We can see from table 1 that the temperature variation is very large and it must be compensated for a high-accuracy oscillator. In this paper, a very simple and effective method is used.

In the CMOS $0.5\ \mu\text{m}$ process, we use poly-silicon for resistors and the resistance goes down when temperature increases. Meanwhile, the impedance of a transistor increases with increasing temperature. Hence, using a combination of the resistor and the transistor will be an effective way to eliminate the temperature variation. Also the impedance of the transistor and the resistance of the resistor are precisely picked for the best matching.

T (°C)	Period (us)		Frequency (MHz)	
0	0.5037	0.74%	1.985	-0.75%
27	0.5004	0.08%	1.999	-0.05%
40	0.4995	-0.10%	2.002	0.10%
80	0.4998	-0.04%	2.001	0.05%

Table 2 Temperature variation after compensation

Combining OSC and temperature-compensated trimming resistor array together, the whole circuitry is shown in Fig. 6. The left part of the circuit is the current mirror with the trimming resistor array while the right part is the wave shaping circuit. In the end of the resistor array, there is a transistor that is always working in the saturated region. This transistor offers temperature compensation.

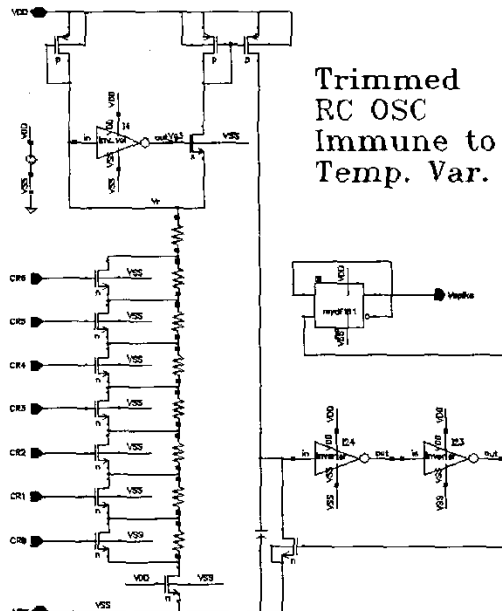


Fig. 6 Final Trimmed RC Oscillator

V. Simulation Results and Layout

Fifty-four simulations are performed to check the trimming results, half of which are for the circuit before trimming and the other half after trimming. Due to the fabrication process, there are 3 simulation corners for each transistor, resistor, and capacitor. Combining all these corners, there are totally 27 simulation corners. The simulation results are better than expected. For all the 27 corners, the output frequency can be trimmed within $\pm 0.5\%$ accuracy (Fig. 8) while it has at most $\pm 40\%$ error before trimming (Fig. 7).

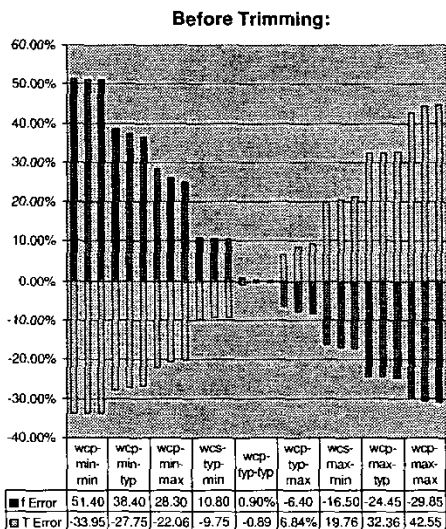


Fig. 7 Frequency Variations Before Trimming

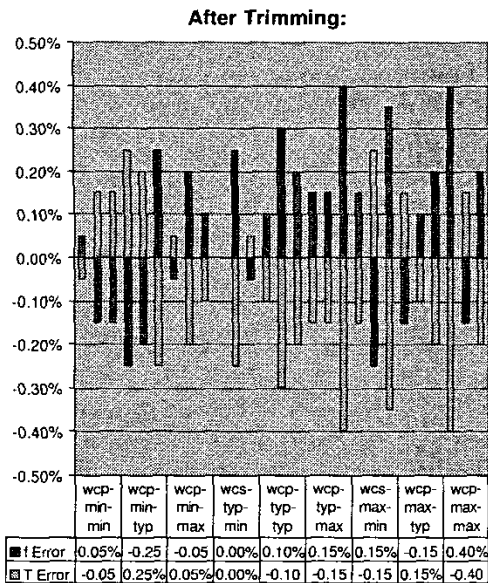


Fig. 8 Frequency Variations After Trimming

Layout of the OSC analog part is $130\ \mu\text{m} \times 145\ \mu\text{m}$ in dimension. Fig. 9 shows the final die photo with the partition explanation. The MUX array is used for testing purpose. We can separate the test of the digital circuit part with the analog circuit part by the selection bit. When SEL is asserted, the trimming signals are applied directly from the pads; On the contrary, the trimming signals are provided by an EEPROM from the digital part, which will be explained in detail at next Section.



Fig. 9 Die Photo

VI. Digital Implementation

For further application, we can use an Inter-IC (IIC) bus to import the digital controlling trimming signal. Then, the data are written into an EEPROM which will provide them to the resistor array finally. The chosen EEPROM is a Non-Volatile Latch (NVL). The verilog code of both the IIC bus and NVL were given for the simulation, so mixed signal simulation was performed.

Fig. 10 shows the mixed-simulation results. "Vout" is the final output signal while "L00" to "L06" are output digital signals from NVL. After "BURN_FINISH" is asserted, the signals are written to NVL, which means trimming signals are applied to the resistor array. We can see from the figure that the frequency of "Vout" changes immediately and is trimmed to the designed value.

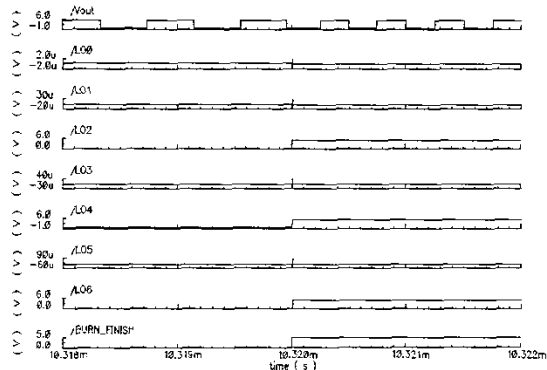


Fig. 10 Output signal with digital inputs from NVL

VII. Conclusion

An efficient and accurate RC Oscillator circuit was successfully implemented by the binary-weighted trimming resistor array using a $0.5\ \mu\text{m}$ CMOS process. The output frequency can be trimmed to be within $\pm 0.5\%$ error while the original OSC will have $\pm 40\%$ error due to process error before trimming. Also temperature compensation circuit design is successfully applied to the circuitry. The circuit is almost immune to temperature variation. Currently, the fabricated chip is being tested successfully.

VIII. References

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