A Novel Digital Controlled Technique For Operational Amplifier Compensation

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Abstract—In this paper, a method for operational amplifier compensation is described. An operational amplifier having an offset as high as $\pm 20mV$ can be compensated to have a residual offset of as low as $\pm 1mV$. The offset is achieved by trimming the currents in the active loads of the differential pair stage of the op-amp. The trimming currents are obtained by means of a series of binary weighted current sinks. The result of compensation can be observed digitally, and the trim data that is needed to switch on or off the current sinks can also be sent serially in digital format. In this paper, a chip has been designed which incorporates the afore-mentioned compensation technique, and the initial version of the chip without the digital interface logic has been fabricated using AMI $0.5\mu m$ CMOS technology.

I. INTRODUCTION

Over the past few years the demand for higher precision integrated circuits (ICs) has skyrocketed, and with the advancement in the design technology, more and more devices are getting packed on the chip. However, there still exists the problem of precision and variations of the fabrication process with the result that components differ from wafer to wafer and even from chip to chip on the same wafer. Special circuit trimming techniques including laser trimming have been incorporated to trim the die for optimum performance. The downside of this is that it is an expensive and difficult process and once trimmed, the circuit cannot be trimmed again. Other schemes of trimming require external components. This increases the cost due to pin count and more circuitry. To address the above issues, a trimming technique which is field-applicable and which can be applied more than once is proposed. In order to verify the effectiveness of the method, this technique is put to use to trim the inherent offset of an op-amp due to process dependent variations. The trimming is done via a two wire serial bus that follows the Philips I^2C protocol, and the trim data is stored in the EERAM. This will enable the op-amp to hold its trimmed state. The obvious advantage here is that the op-amp can be re-trimmed at a later time should the need arise. This paper is divided into five sections. The first section deals with the analog trim circuit and the op-amp which is to be compensated. The second section describes the data sampling block while the third section deals with the Philips I^2C interface which is used to convert the serial data into parallel format. The fourth section covers the test plan and the results obtained from simulations. The fifth section gives the chip details, and the final section discusses the possible future improvements and concludes the paper.

II. ANALOG TRIMMING CIRCUIT

The offset voltage in an op-amp is a result of the mismatch in the currents flowing in the two branches of the differential pair in the input stage. Figure 1 illustrates a simple MOS differential pair. With reference to figure 1 and assuming that the current source I_{dc} is not yet connected to either node a or node b, offset voltage is non-zero when $I_1 \neq I_2$ when $V_{inp} = V_{inm}$. $I_1 \neq I_2$ implies $I_3 \neq I_4$. The effect of this mismatch in the currents is a shift in the voltage transfer characteristic (VTC) that is equal to the offset voltage. The approach used here is to trim the currents in the active loads so as to compensate for this shift in the VTC. The trimming is implemented by connecting a current sink which sinks the current from the selected current sink stacks from either node a or node b. For example, if $I_1 > I_2$ (i.e., when the offset voltage is negative), then the current sink I_{dc} is introduced at node a to sink in the difference $(I_1 - I_2)$. This effectively results in I_3 being equal to I_4, thus, compensating for the shift in the VTC.

The following specifications were used in the design of the trimming circuit:

0-7803-7150-X/01/$10.00@2001 IEEE

1) Range to be compensated: $-20mV$ to $20mV$
2) Allowable offset after compensation: $\pm 1mV$

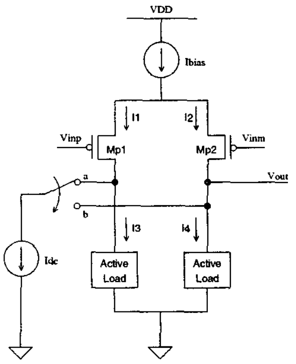


Fig. 1. Differential input stage

The trimming circuit is comprised of a stack of seven binary weighted current sinks that are switched by the binary data ($D0 - D7$) in the non-volatile memory. A wide swing cascode configuration is used to bias the current sinks. Figure 2 shows the scheme of the current sink array. Binary weightage is achieved by sizing the transistors accordingly, i.e., by having different values for the multiplication factors K and L. The stack itself is divided into two modules - the LSB stack and the MSB stack. The minimum size transistor used for the LSB stack has a $W/L = 4\ \mu m/6\mu m$. The minimum W/L used for the MSB stack is $24\ \mu m/4\mu m$.

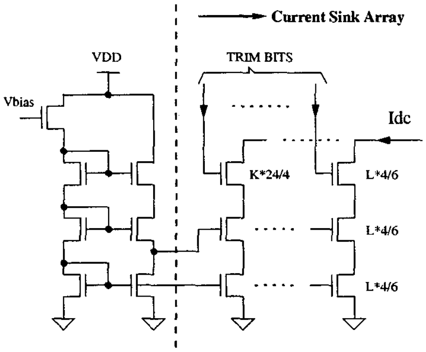


Fig. 2. Current sink stack

Table 1 gives the designed current values and the values obtained using the spice simulations.

Table 2 shows the current source outputs for different process corners. In the table, wcs is the slow corner, typ is the typical corner and wcp is the fast corner.

TABLE I

Designed current values and simulation results

D_{Bit-On}	*Designed I value, uA*	*Simulation Results, uA*	$V_{os}+$ (mV)	$V_{os}-$ (mV)
D0	0.14	0.09	0.97	-0.78
D1	0.28	0.18	1.12	-0.82
D2	0.56	0.37	1.14	-0.84
D3	1.25	1.37	1.18	-0.87
D4	2.50	2.75	3.16	-2.85
D5	5.00	5.50	7.13	-6.82
D6	8.75	9.61	11.17	-10.84
D7	sign bit	-	-	-
ALL ON	18.48	19.87	23.20	-22.00

TABLE II

Simulation results for various corners

D_{BitOn}	*wcp*, [*uA*]	*typ*, [*uA*]	*wcs*, [*uA*]
D0	0.12	0.09	0.07
D1	0.24	0.18	0.15
D2	0.48	0.37	0.30
D3	1.74	1.37	1.15
D4	3.48	2.74	2.3
D5	6.96	5.50	4.60
D6	12.19	9.62	8.05
D7	-	-	-
ALL ON	25.21	19.87	16.63

III. DATA SAMPLING BLOCK

The data sampling block interprets the op-amp output and converts it into a digital output for easier and faster interpretation. It consists of three components: a 14-bit up-down counter (or sample counter), a 14-bit down counter (or cycle counter) and a multiplexer switch which would toggle between the MSB outputs and the LSB outputs of the sample counter. This was done to reduce the output pin count.

The output of the op-amp is sampled by the up-down counter which increments its count value when the amplifier output is above the reference threshold and decrements when it is below the threshold. To avoid the situation where the sampling counter overflows, a down counter is used to limit the number of cycles (or counts) the up-down counter samples. To allow for a reasonable resolution, the two counters are 14 bits wide. Also to reduce the output pin count, 8-bit multiplexer is used to switch between 8 LSBs and the higher bits which are sent to the output of the chip.

When the local clock into the sample counter is disabled by the cycle counter, the sample counter will hold the output values to be read by the user until the arrival of the reset signal which will be pinned out and controlled by the user. When the reset signal comes in, the values held by the counter will be set to zero, and the sample counter will start counting for the number of cycles set in the cycle counter once the reset is disabled.

IV. I^2C INTERFACE

To minimize pin count, trimming is accomplished through the Philips two-wire I^2C serial bus protocol. Trim data is programmed into the I^2C and stored in the non-volatile memory cell (EERAM) as well as being connected directly to the analog circuit for test purposes. The EERAM would retain the trim information such that the I^2C would not need to be re-adjusted every time power was applied. Using EERAM greatly simplifies the trimming process and is much less expensive than laser trimming. The advantage here is that the trimming can be done in the field by the user with the minimum of equipment.

V. TEST PLAN AND SIMULATION RESULTS

The block diagram of the entire test setup including the data sampling block, I^2C and the non-volatile latch is as shown in figure 3.

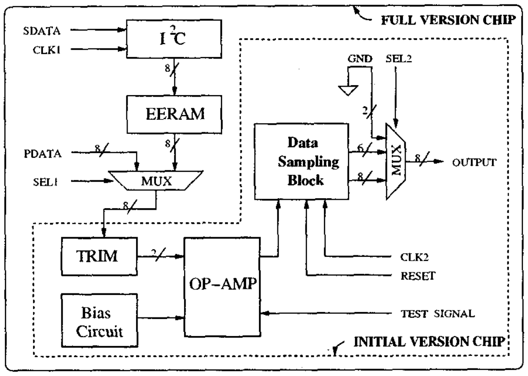
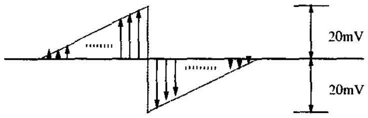


Fig. 3. Chip block diagram

The serial trim data is read into the non-volatile latch through the I^2C interface. When the chip is powered, the data is applied to the trimming circuit. A zero mean cyclic wave of frequency $1Khz$ and $40mV$ peak-to-peak is applied as the input to the op-amp which is hooked up as a comparator. The output of the op-amp is then sampled at the rate of 80 samples per cycle (of the input cyclic wave) by the up/down counter in the data sampling block which counts up during the positive cycle and counts down during the negative. For the case of positive offset voltage, the number of up counts will be greater than the down counts and vice-versa for a negative offset.

The minimum resolution (minimum offset that can be detected) of the test setup depends on the nature of input cyclic wave used. It can be a sine wave or a triangular wave or a saw-tooth wave. Figure 4 shows the saw-tooth wave with its minimum resolution of $0.5mV$, and the calculation of the offset voltage as a function of the output sample count. The saw-tooth offers the best resolution while the triangular wave has a resolution twice that of the saw-tooth due to its redundant nature. In the case of the sine wave, the resolution will be more precise for a larger offset value than a smaller offset due to the change in the gradient of the curve.


Saw-Tooth Wave Input

Input Signal Frequency -> f(in)
Sampling Frequnecy -> f(s) = 80*f(in)
Minimum Resolution -> 20mV / 40 = 0.5mV
Offset Voltage Calculation -> count / 2 * 0.5mV

Fig. 4. An example of cyclic test input

The target resolution of ±$1mV$ can be obtained by using either the triangular wave or the saw tooth wave as the input. In both cases, the counter output can easily be interpreted to calculate the offset of the op-amp and, hence, set the necessary bits for the trim circuit using table 1.

Figures 5 show the the VTC of the op-amp before and after the compensation. The offset voltage is brought down from -9.99mV to -860μV after the compensation.

VI. CHIP DETAILS

The chip is housed in a 40-pin package, and all 40 pins are used for the test chip incorporating the I^2C interface. Separate power pins are allocated for the analog and digital parts as well as for the guard rings which enclose the analog components. The layout of the chip was done using AMI $0.5\mu m$ CMOS technology and is shown in figure 6. Figure 7 is the photograph of the initial test chip which does not have the I^2C interface included.

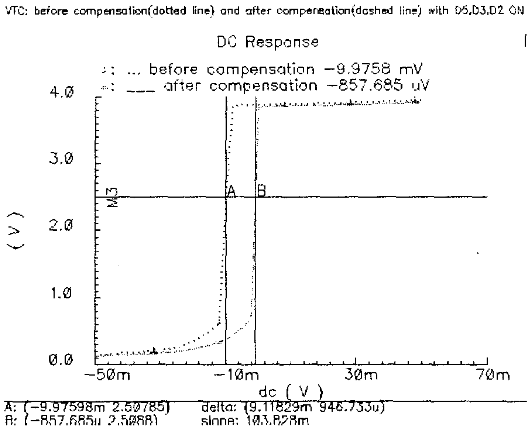


Fig. 5. VTC before and after compensation

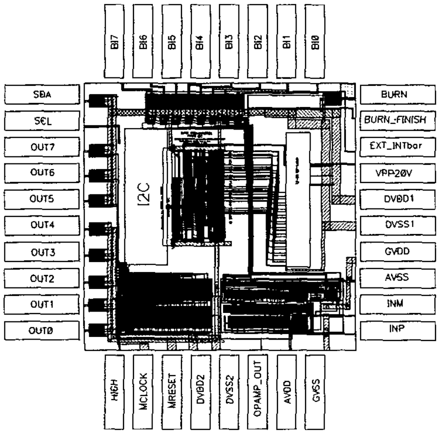


Fig. 6. Pin diagram of the chip

VII. Future Improvements and Conclusion

A. Conclusions

A trimming circuitry for the current flowing in the differential pair stage of the op-amp was designed and tested to compensate for the offset in the op-amp. This was effectively accomplished, and the trim circuitry was able to compensate a maximum offset of $\pm 20mV$ to less than $\pm 1mV$. In the full version of the test chip, the trim data for the trim circuit is taken in serially by the I^2C interface which converts it to parallel format and stores it in the EERAM. This digital data in the EERAM is used by the trim circuit to switch on the appropriate current sources.

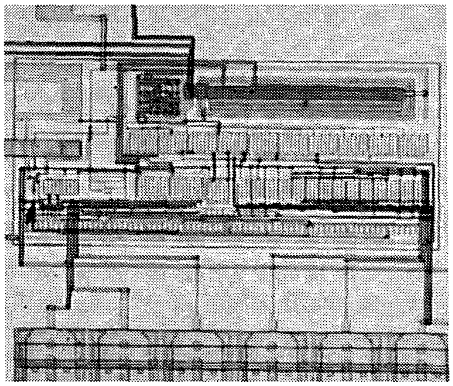


Fig. 7. Photograph of initial chip analog part

B. Future improvements

The temperature sensitivity of the compensated offset is one of the areas which needs improvement. To have an idea of how offset drifts with varying temperature the following experiment was conducted. The amplifier was compensated at room temperature (27^oC) to have a residual offset of less than 1mV and the temperature was varied from 0^oC to 100^oC. A change of approximately $75\mu V/^oC$ was observed. This can be minimized by making the trim currents the slaves of the bias current of the op-amp.

As of now there is no feedback to map the digital output to the trim circuit to automatically adjust trim data depending on the counter output. This could be another area of improvement. The I^2C is configured to handle up to 12 bits of trim data and, currently, only 8 bits are being used. The trim capabilities can be extended by 4 more bits and, thus, a wider range of offset can be compensated.

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