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Guest Editorial

Cristiana Bolchini, Yong-Bin Kim

Cristiana Bolchini
Politecnico di Milano
Dipartimento di Elettronica e Informazione
P.zza L. da Vinci, 32 – Milano – Italy
e-mail: bolchini@elet.polimi.it

Yong-Bin Kim
Department of Electrical and Computer Engineering,
Northeastern University
360 Huntington Avenue
Boston, MA 02115-5000
e-mail: ybk@ece.neu.edu

Advances in semiconductor technology allow much higher performance levels on a single chip. At the same time, the ever-shrinking device dimensions and voltages have given rise to increased problems of faults and defects. Furthermore, nanotechnology is emerging as an alternative, as lithography-based silicon VLSI technology is expected to hit its limit. However, imperfections in the fabrication process along with on-chip temperature and voltage variations result in yield-reducing defects and faults, whose density and severity grow significantly with the size and density of the chip. Therefore, a new paradigm for the development and use of defect and fault tolerant techniques at the design phase is required to complement existing efforts at the manufacturing phase. Novel techniques to address the emerging challenges and issues in the new VLSI technology era are introduced in this special issue, containing nine selected papers, whose preliminary versions were presented at the 22nd IEEE Defect and Fault Tolerance Symposium in 2007.

The nine papers of this special issue are classified into three categories, which are emerging technology, testability/test vector, and modeling.

The emerging technology category opens with a paper by M. Fukushi et al. that proposes and evaluates an efficient defect isolation framework motivated by the need to achieve scalability for extremely large scale DNA self-assembled networks. The second paper by M. Hashempour et al. investigates the characterization of the intentionally induced puncture on an erroneous DNA tile site in the grown DNA crystal as part of a healing process. The third paper, presented by X. Ma et al., investigates QCA (Quantum-Dot Cellular Automata) for testable implementations of reversible logic in array systems. The method makes fault masking possible in the presence of multiple faults. The last paper, by F. Karim et al., deals with the effects of random shift clocks and presents a model to evaluate errors in QCA.

There are three papers related to testability and test vector issues. The first paper, by W. K. Al-Assadi and S. Kakarla proposes new DFT techniques for Asynchronous NULL Convention Logic (NCL) to enhance the controllability and observability with acceptable gate overhead using an existing commercial DFT tool. The second paper by M. Favalli and M. Dalpasso analyzes the problem of bridging fault detection in the presence of parameter fluctuation and proposes a method to find the minimal set of test vectors to tackle bridge faults at low frequency. The last paper in this category is by K. Namba et al. They present a non-intrusive test compression algorithm for IP core testing using reconfigurable networks, fixing-flipping coding, and fixing-shifting-flipping coding.

Finally, there are two papers in the modeling category. The first paper by M. Valderas et al.

presents a quantized delay model to capture delays of a circuit under test in an FPGA. This new approach builds an FPGA based Single Event Transient (SET) emulator. The last paper in this category is authored by R. Ghaida and P. Zarkesh-Ha. They propose and test a layout sensitivity model to estimate electro-migration vulnerable narrow interconnects, focusing on a stochastic method of critical area analysis that consists of the modeling of the layout sensitivity to defects, defined as the ratio of critical areas to the overall layout area.

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