A Deep Sub-Micron SRAM Cell Design and Analysis Methodology

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Abstract—This paper presents a comprehensive SRAM design and diagnosis methodology including optimization paradigms on cell stability test against power supply fluctuations, SRAM access time, bit line voltage switching, and static noise margin analysis of a SRAM cell.

I. Introduction

As process technologies have been scaled down, the layout size of SRAM has greatly been reduced. On the other hand, the stability of a conventional 6-transistor SRAM cell has been worse than ever due to process variations, short channel effect, soft error rate and low supply voltage[1][2][3] against the size advantage. Therefore, memory designers have relied upon exhaustive simulations of SRAM cells to determine whether or not they would be safe as designed to reduce cell area and to enhance electrical characteristics such as stability, read/write margins, and access speed of the SRAM cell. Although the various novel architectures for SRAM cell have been presented[4][5][6][7], there are two essential aspects in the design consideration of SRAM cell: the size and the bistability of the cell that depend on each other since a larger cell area can improve the stability. Therefore, it is important to understand how to design SRAM cells with minimizing the size of SRAM cell with sufficient bistability.

In this paper, we show four test paradigms that can be used to evaluate the safety of the SRAM cell. They are SRAM cell integrity against power supply fluctuations, SRAM access time, bit line voltage switching, and static noise margin at various corners such as FFHH (fast PMOS, fast NMOS, high voltage, high temperature), FSHH, FSLL, SFHH, SFLL, SSLL and TTLH. Circuit simulations have been performed using 0.18μm and 1.5V power supply at the feasible worst case offsets such as channel length variations (worst case $\pm$2.5% variations), and channel width variations (worst case $\pm$5.0% variations).

II. Integrity against power supply variations

The integrity of a SRAM cell with regard to the power supply variations is tested observing whether the cell flips its state to its favored state due to the imbalanced geometry when unstabe word line voltage is biased.

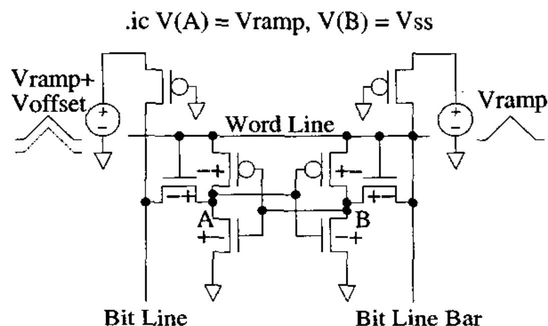

Fig. 1. SRAM Cell Ramp Test Setup.

Fig. 1 depicts the test setup, including the device geometry and voltage offsets that put an SRAM cell in the most unstable state, and the initial states are against the favored states. The '+' and '−' in the Fig. 1 represent the worst case positive and negative variations respectively. And the first sign (+ or −) represents the transistor width variation and the second sign represents the transistor length variation. Applied in this test are all predictable worst imbalances such as geometry mismatches and IR drop, to cause the cell to be an opposite status against its initial setup. This test should be executed very slowly (quasi-static, e.g., 1V/ms) from a level above the threshold voltage to a higher voltage than the desirable supply voltage under the most unstable condition. If the ramp of the supply voltage is changed too fast, the initial state can be reinforced.

As shown in Fig. 2, the passed curves keep their origin states over the range of the ramp voltages.

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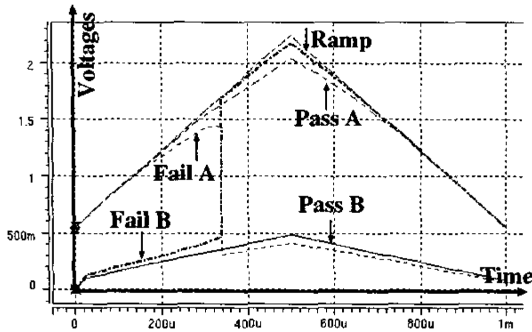

Fig. 2. Ramp Test Behavioral Curves.

On the other hand, if the cell is unstable, the states are switching during the ramp test.

TABLE I
The Results of Ramp Test Under Several Conditions.

α/β	ffhh	fshh	fsll	sfhh	sfll	ssll	ttlh
1.0/1.0	x	x	x	x	x	x	x
1.0/1.5	x	x	x	x	x	o	x
1.0/2.0	x	x	x	o	o	o	x
1.0/2.5	x	x	o	o	o	o	o
1.0/3.0	O	O	O	O	O	O	O
1.5/1.0	x	x	x	x	x	x	x
1.5/1.5	x	x	x	x	o	o	x
1.5/2.0	x	x	x	o	o	o	o
1.5/2.5	O	O	O	O	O	O	O
1.5/3.0	o	o	x	o	o	o	o
2.0/1.0	x	x	x	x	x	x	x
2.0/1.5	x	x	x	o	o	o	x
2.0/2.0	x	x	o	o	o	o	o
2.0/2.5	O	O	O	O	O	O	O
2.0/3.0	o	o	x	o	o	o	o

Table I shows the test results for various combinations of the α and β ratios (α: ratio between pull-up and access transistors, and β: ratio between drive and access transistors). This test was performed for the cases that passed at each corner for the worst case geometry mismatches and 100mV off-set voltage between word line and bit line. The 'x' represents 'failure', the 'o' stands for 'pass', and the 'O' represents the α/β ratio that passed all corners. At this step, the α ratio and β ratio ranges of the transistors are obtained to guarantee the stability for the worst feasible power supply variations.

III. Access Speed

Process technology and supply voltage scaling have improved the logic circuit delay. However, the delays of bit line and sense amplifier are not scaled at the same ratio since the offset voltage of the sense amplifier does not scale[8]. On the other hand, in order to secure a fast read speed, the voltage swing on the bit line is generated as low as possible[9].

Among the successful gate-size combinations from the first stage, the cell speed is tested by measuring the bit line current when the cell is accessed to make sure the cell speed meets the target performance. The peak read current of the cell is inversely proportional to the series resistance through the access and drive transistors in the discharge path[10]. Therefore, the pull-up transistor changes are excluded during this test. This test requests the actual bit-line load capacitance modeling, which is a key factor for SRAM performance[10]. Fig. 3 shows how to setup this test environment to minimize the read current. And Table II describes the peak currents of a cell with α=1.5 and β=2.5 (Native as a cell drawn in the layout and offset as the cell with variations).

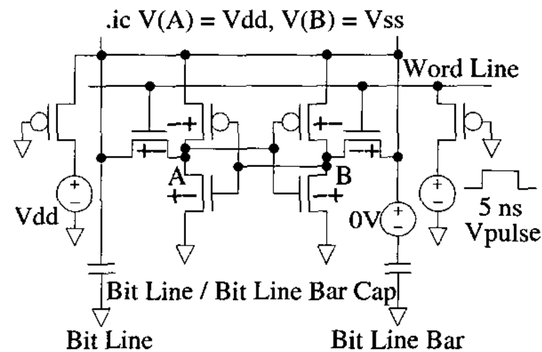

Fig. 3. SRAM Cell Read Current Measurement Setup.

TABLE II
The Results of Read Current Measurement with α=1.5, β=2.5 and bit line load=0.5pF.

Corner	Vdd(V)	T(°C)	Native(μA)	Off.(μA)
ffhh	1.65	100	101.7	99.3
fshh	1.65	100	73.6	72.1
fsll	1.35	0	48.4	47.1
sfhh	1.65	100	82.9	79.6
sfll	1.35	0	54.2	51.4
ssll	1.35	0	36.5	34.7
ttlh	1.35	100	52.7	50.6

IV. State Switching Point

The SRAM cell is normally designed to have enough noise immunity. Therefore it requests a full supply voltage swing on the bit line to override the previous cell data during write[9]. The switching

point is defined as a bit line voltage that causes the states of the node A and B to be exchanged. Fig. 4 shows how the worst offsets are applied for this test. At first, initialize the bit line and bit line bar voltages VDD, the word line voltage VSS, the node A voltage to VDD, and the node B voltage to VSS. Then observe whether the voltages of the nodes are exchannged while the bit line voltage is decreased slowly (quasi-static) to VSS with making the word line voltage VDD, as shown in Fig. 5. And Table III shows the switching points of a cell with α=1.5 and β=2.5.

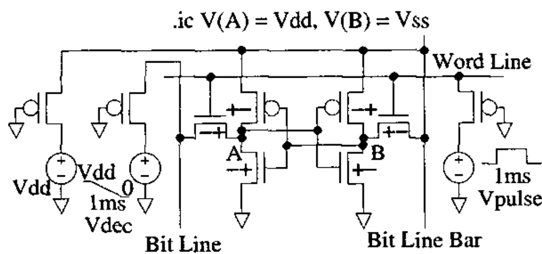

Fig. 4. SRAM Cell State Switching Point Measurement Setup.

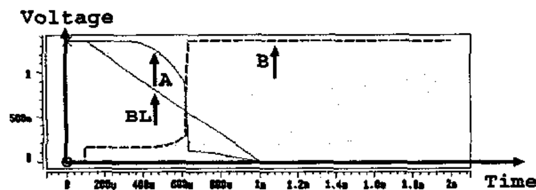

Fig. 5. The Example of Successful Switching Point Behavioral Curves.

Fig. 6 shows a failed case that does not obtain the switching point. And it is true that the larger select transistor length, the more stable against the power supply variations. However, if the select transistor length is increased beyond a certain range, the switching point is not be obtained. This switching point voltage is used to the reference to define the stable read and write voltage ranges with the static noise margin (SNM) that is tested at the next step.

V. Static Noise Margin (SNM)

It is also important to check the SNM of the cell because the deeper sub micron, the weaker immunity against noise due to the lower operating voltage. The voltage transfer functions of the two inverters in the SRAM cell strongly depend on the

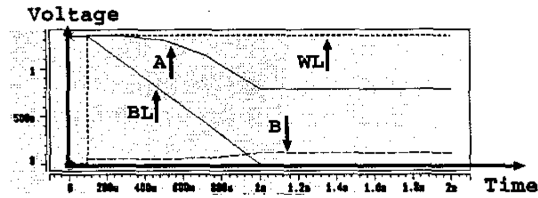

Fig. 6. The Example of Failed Switching Point Behavioral Curves.

TABLE III
The Results of Switching Point Measurement with α=1.5 and β=2.5.

Corner	Vdd(V)	T(°C)	Native(V)	Off.(V)
ffhh	1.65	100	0.983	0.900
fshh	1.65	100	0.985	0.921
fsll	1.35	0	0.746	0.716
sfhh	1.65	100	0.771	0.698
sfll	1.35	0	0.599	0.551
ssll	1.35	0	0.636	0.594
ttlh	1.35	100	0.680	0.625

static noise, which results from the geometry mismatches, non-uniform transistor degradation and threshold voltage variation[3]. And the static noise can cause the two inverter curves not to overlap at three crossing points (dark dots) in shown in Fig. 7, or unbalanced. Seevinck, et al, presented the direct measurement method of the SNM from SPICE simulation by rotating the axes of the cell voltage transfer functions by 45°[3].

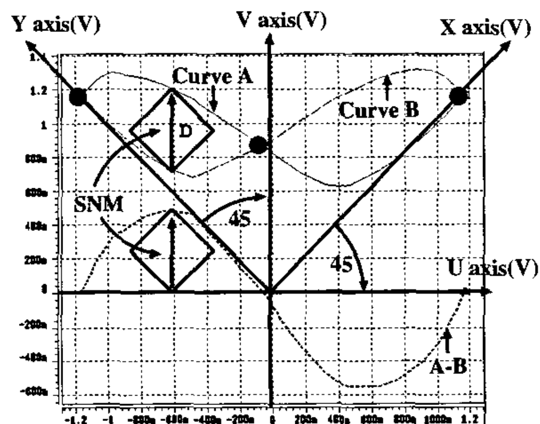

Fig. 7. Depiction of Seevinck's axis rotation and SNM measurement.

Fig. 7 describes how SNM can be obtained by measuring the diagonal span of smaller square and the distance between the curve A and the curve B, since the rotation makes the differences(D) between

the two curves in the new coordinate system an absolute value of noise margin.

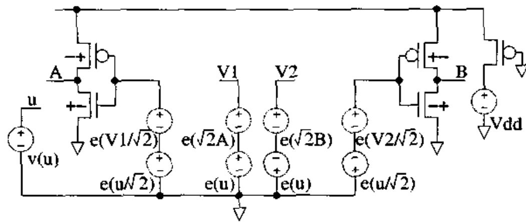

Fig. 8. Seevinck et àl. circuit implementing SNM measurement with offsets.

As shown in Fig. 8, the Seevinck used dependent voltage sources to accomplish the rotation of the SRAM cell voltage transfer characteristic in Fig. 7. Fig. 8 also shows the offsets to minimize the SNM. Table IV repesents the results of SNM test at TTLH (typical PMOS, typical NMOS, low voltage and high temperature) with α=1.5 and β=2.5.

TABLE IV
The Results of SNM Test at TTLH with α=1.5 and β=2.5.

Corner	Vdd(V)	T(°C)	Native(V)	Off.(V)
ffhh	1.65	100	0.342	0.288
fshh	1.65	100	0.325	0.287
fsll	1.35	0	0.276	0.252
sfhh	1.65	100	0.387	0.353
sfll	1.35	0	0.338	0.319
ssll	1.35	0	0.277	0.256
ttlh	1.35	100	0.295	0.279

As shown in Fig. 9, the safe read/write regions are defined from the switching point plus SNM to the power source and from the switching point minus SNM to the VSS, respectively. The spaces between the two regions and the switching point are marginal read/write ranges, respectively.

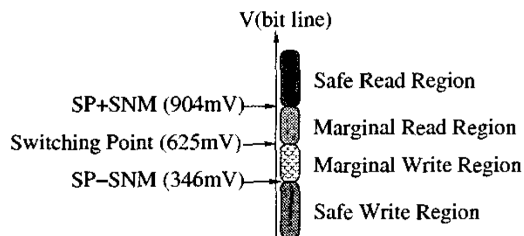

Fig. 9. Safe and Marginal Accessing Bands at TTLH with α=1.5 and β=2.5.

VI. Conclusions

Using the SRAM cell design criteria we successively evaluated the minimum size traditional 6-Transistor SRAM cell, considering static noise margin against geometry mismatches and supply voltage variations . These models can easily be applied to different memory architectures such as thin film loads, register loads, dual port, and other configurations. According to the experimental results for the 6-Transistor single port SRAM cell, the optimum α and β ratios with the reasonable stability margins are 1.5 times and 2.5 times, respectively with regards to the minimum design rule size of the access transistor in a deep sub-micron process (0.18μm).

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