

An Accurate DAC Modeling Technique Based on Wavelet Theory

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Abstract—Two new DAC modeling techniques based on principles of wavelet theory are described in this paper. Macro model and mathematical model are developed for analog and digital circuit simulation, respectively for fast and accurate results using exponential function, damped sine wave, and linear waveform. An 8 bit DAC has been implemented to simulate and evaluate the models. The INLs of the macro and mathematical model based simulations are $\pm 0.2\text{LSB}$, which are the same as HSPICE simulation. The DNLs of HSPICE simulation, macro model, and mathematical model based simulations are $\pm 0.22\text{LSB}$, $\pm 0.28\text{LSB}$, and $\pm 0.25\text{LSB}$, respectively. The simulation times are 2.9 second for macro model, 0.15 second for mathematical model, and 68.09 second for HSPICE simulation.

I. INTRODUCTION

The performance of digital signal processing is limited by the accuracies of the data converters and analog filters such as interpolation and anti-alias filter. Even though the performance of digital signal processor is improved with the advanced processing technology advent, the accuracy and performance of analog circuit cannot keep up with that of digital signal processor. As a result, the performance of the entire system is mainly limited by data conversion components such as DAC or ADC. Therefore, system and circuit designers, who intend to use the analog conversion components designed by other designers, should understand the characteristics of analog conversion components. The best way to understand the analog conversion components is to measure the characteristics directly from the component. However, it is time- and cost-consuming procedure, and the results cannot be used to verify the entire systems or integrated circuits under design. The alternative is to use analog circuit simulator. This gives us very close results to the measured ones at low cost. However, it still cannot be used to verify the entire system or integrated circuit due to its analog nature and excessive simulation time. Therefore, the demand for new modeling technique satisfying the cost- and time-effectiveness and versatility under the various simulation environments is increasing in the System-On-Chip era.

In [1], mathematical approach is used to model the DAC output signal. This technique was strictly based on a direct mathematical interpretation. Therefore, it is very cumbersome and numerically wasteful due to calculation complexity.

In [5], the performance effects by parasitic elements and circuit mismatches of DAC have been analyzed. However, it did not consider the other parasitic elements such as

power pad and interconnect wires. And the internal elements and timing information should be known in order to model DAC. These issues require too much resources for DAC modeling.

In this paper, a mathematical and a macro modeling techniques of DAC are presented. These models are able to accurately describe not only dynamic but also static behaviors, and it can be used for both digital and analog simulation environments.

II. PROPOSED MODELING METHODOLOGY

Traditional method to model an arbitrary complex repeating waveform at time domain is Fourier Series technique. This technique has been effectively used to model arbitrary complex periodic waveforms. The basic idea of this technique is that an arbitrary waveform can be obtained by the sum of sinusoidal functions. The merit of this technique is analytically tractable and arbitrary levels of accuracy are obtainable by adding the additional sine or cosine components. However, a relatively larger numbers of harmonic complex sine waves and cosine components are required to model the arbitrary waveform.

To avoid complex mathematical works, wavelet theory is considered [4]. Because wavelet theory can use another set of orthogonal functions in addition to sinusoidal functions, it can be used as an effective and basic principle for DAC modeling. To model the behaviors of DAC using wavelet theory, basis functions should be identified first. To identify them, the output signal of DAC is analyzed in time and frequency domain. Considering the output signal characteristics of DAC in time domain, the output signal of DAC can be divided into three nonlinear separable functions - exponential function, exponentially decaying sine wave, and linear waveform for glitch. In frequency domain, the most power of glitch is usually at higher frequency than those of exponentially decaying sine wave and exponential function. And the power of exponentially decaying sine wave is located at higher frequency range than that of exponential function.

To visualize these statements, the frequency characteristics of a DAC output signal is investigated in Fig.1, where three singular frequency areas are observed. A is assumed to be related to DC level of DAC output signal, B is originated from the damped sine wave which represents the instability within the DAC amplifier itself, and C results from glitch. Next, three functions are analyzed in frequency domain. The results are shown in Fig.2. Each of basis func-

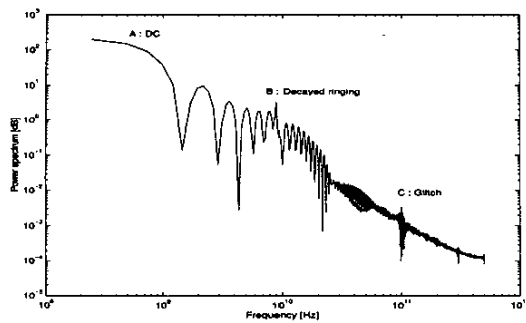


Fig. 1. Power spectrum of a DAC output

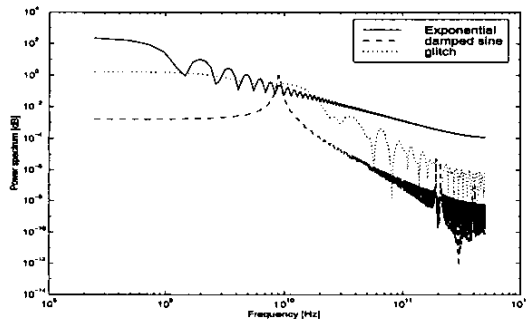


Fig. 2. Power spectrum of three basis functions

tions show similar frequency characteristics at three frequency areas. Therefore, three functions are considered as candidates for basis functions. Even though these functions are neither orthogonal functions nor linear function in time domain and power spectrums are a little bit overlapped, the frequency characteristics of these functions are separable by filters. Therefore, these functions can be treated as quasi basis functions of DAC. As a result, the principles of wavelet theory can be applied to model the operation of DAC.

III. MODELING METHODOLOGY

Two methodologies are suggested in this paper. First method is macro modeling that uses passive components and adders. The other method is mathematical modeling that uses mathematical equations to depict the basis functions. The basic block diagram for DAC modeling is shown in Fig.3. It consists of 4 parts - exponential function generator, damped sine wave generator, glitch generator, and adder to add the output of three generator.

A. Macro Modeling

For macro model, the basis functions are generated by simple circuits that consist of resistors, capacitors, and inductors. The advantage of this method is to reduce the simulation time under circuit level simulation environment, and it provides direct insight about the source of non-idealities. In addition, the parasitic elements also are included in the model.

The macro model of 1 bit DAC is shown in Fig. 4. Ex-

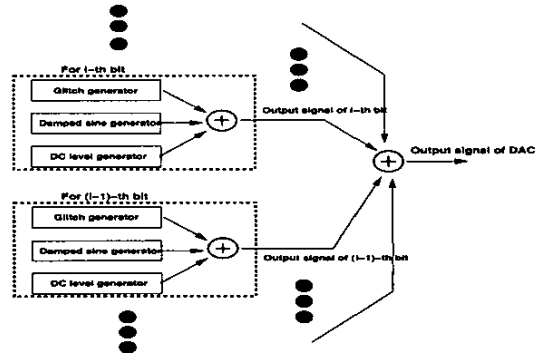


Fig. 3. Block diagram for DAC model

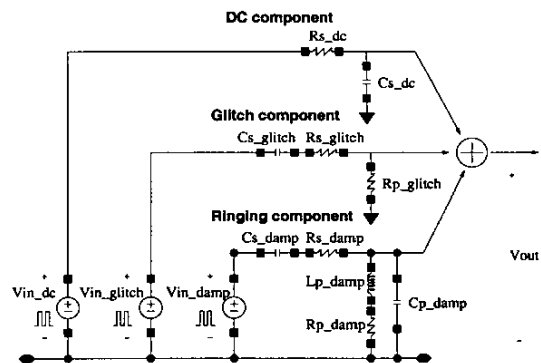


Fig. 4. Circuit diagram of all three circuit components for 1bit DAC Macro Model

ponential function generator is represented by a simple RC circuit. Its role is to generate DC level of DAC whose output slew rate depends on RC time constant and edge rate of input voltage. The circuit of a simple RLC ringing component contributes a damped sine wave to DAC model. As for the glitch, most of its energies are in high frequency range due to its nature. Therefore, a glitch can be represented by differentiating finite step response through a capacitively coupled RC network. The duration of glitch is also controlled by RC time constant and rising/falling time of stimulus voltage.

The simulation results of each component are shown in Fig. 5(a), which shows simulated superimposed results of all components. Fig. 5(b) demonstrates the summation of all three components output signal to produce the desired waveform. The result is a realistic replica of the actual waveform with considerably less numerical complexity. In macro model, the time delay of the stimulus input waveform can be incorporated into the recombination of signals to obtain the finer modeling results. Each coefficients of macro model can be easily obtained with the assistance of HSPICE[3].

B. Mathematical Modeling

For mathematical modeling of DAC, Equation (1) - (4) are used. These equations are coincided with the macro model of DAC except the one for glitch. Instead of con-

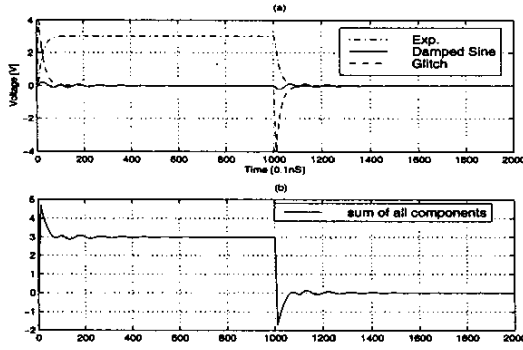


Fig. 5. Output waveform of (a) three basis functions and (b) summation of three basis functions from macro model

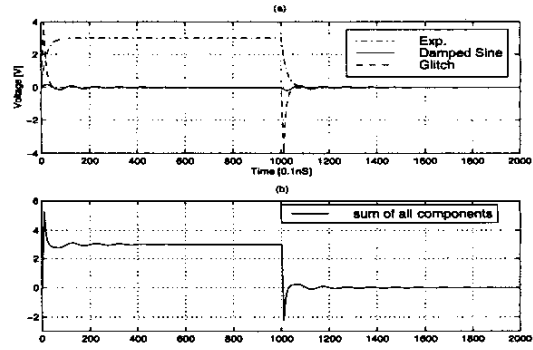


Fig. 6. Output waveform of (a) three basis functions and (b) summation of three basis functions from mathematical model

verting a simple RC circuit into mathematical expression, a glitch can be interpreted as a linear rising wave up to t_0 followed by an inverted and delayed replica for the same duration, or a linear rising waveform up to t_0 followed by exponentially decaying waveform whose decaying rate is determined by RC time constant. For more sophisticated version to represent a glitch, the glitch of every DAC output signal level is characterized as a function of DAC input, incorporated into a look-up table, and piecewise linear input is applied to the input of the DAC model with input signal. The direction of the glitch is established by the relative direction of the DAC input codes.

$$DC = A_{dc}(1 - \exp(\frac{-t}{\tau})) \quad (1)$$

, where

A_{dc} : magnitude of dc value

τ : rise time constant of dc value

t : time

$$Damp = A_{damp} \exp(-\alpha(t-t_d)) \times \sin(\frac{2\pi(t-t_d)}{T} + \phi) \quad (2)$$

, where

A_{damp} : magnitude of sine wave

α : damping factor of damped sine wave

t_d : time delay of damped sine wave

ϕ : phase of damped sine wave

$$Glitch = A_{gt}[(u(t) - u(t - t_0))t + (u(t - t_0)\exp(\frac{-(t-t_0)}{\beta}))] \quad (3)$$

or,

$$Glitch = A_{gt}[(u(t) - u(t - t_0))t - (t - 2t_0)(u(t - t_0) - u(t - 2t_0))] \quad (4)$$

, where

A_{gt} : magnitude of glitch

t_0 : time at peak voltage of glitch

$u(t)$: unit step function

β : fall time constant

In Equation (1), exponential function has 2 coefficients - DC amplitude and time constant. DC amplitude coincides with the magnitude of input stimulus waveform in macro model, and time constant is given by RC time constant in Fig.4. The damped sine wave can be represented by 3 coefficients; the amplitude and frequency of the sine wave, and the decay rate of the exponential envelope. These coefficients are obtained from the output waveforms of HSPICE simulation. A glitch can be represented by 3 coefficients, start time, peak time, and magnitude of glitch. In Equation (3), the additional coefficient for decaying rate is required.

The benefits of mathematical model are 1) Mathematical model is suitable for digital logic simulation environment. While the macro model of DAC can be easily used under analog simulation environment, the mathematical model is easy to be included in the digital logic simulation. Using a commercial tool such as PLI of VERILOG[2], mathematical model can be a part of the user-defined function for VERILOG logic simulation. 2) Simulation time using mathematical model is significantly reduced comparing to the macro model based simulation that uses an analog circuit simulator. C and MATLAB are used to implement mathematical model and to analyze the output data. Fig. 6 shows simulated superimposed result of all three components, and the summation of all three components output signal.

IV. EXPERIMENTAL RESULT

An 8bit R2R DAC is designed and simulated including power pads and interconnect wires as an example to verify the usefulness of the proposed modeling methods.

A. Static Behavior

To verify static behaviors of macro and mathematical model, the INLs and DNLs of 256 level are compared with the results of HSPICE for the 8bit example DAC. The sampling frequency of input data is 1MHz. Fig.7 shows the INLs of the example DAC circuit simulation, macro and mathematical model simulations. The number of sampling is 256 which is full range of 8bit DAC. The INLs of ex-

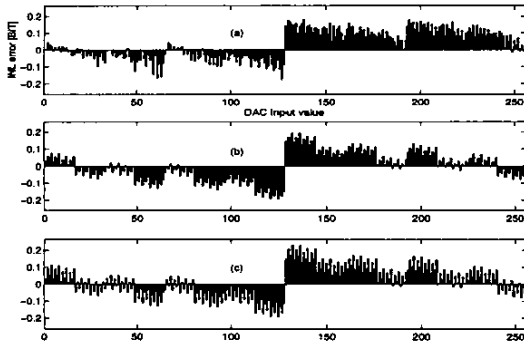


Fig. 7. INLs from (a) HSPICE simulation, (b) macro model, and (c) mathematical model

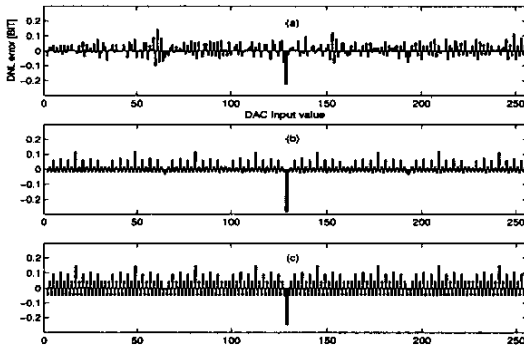


Fig. 8. DNLs from (a) HSPICE simulation, (b) macro model, and (c) mathematical model

ample DAC is $\pm 0.2\text{LSB}$. And the INLs of the macro and mathematical model are $\pm 0.2\text{LSB}$ and $\pm 0.22\text{LSB}$, respectively. Fig.8. shows DNLs of the DAC circuit simulation, macro and mathematical model simulations. The DNLs of the DAC example, macro model, and mathematical model are $\pm 0.22\text{LSB}$, $\pm 0.28\text{LSB}$ and $\pm 0.25\text{LSB}$, respectively.

B. Dynamic Behavior

Fig.9 shows the frequency spectrums when 10KHz sine waves are generated from the R2R DAC for HSPICE simulation and macro model. The sampling frequency of 10KHz sine wave is 1MHz. HSPICE is used to obtain the results of 4096-point FFT[3], and simple rectangular truncation window is selected. Fig.10 shows 8 level output signals in time domain. The spurious-free dynamic ranges are 51dB for HSPICE simulation and 54dB for macro model. The difference between the two results is 3dB, and it is 0.5LSB in terms of bit resolution. The total harmonic distortions (THDs) are 1.02% for HSPICE simulation and 1.0284% for macro model.

C. Benchmark Analysis

The other important factor of modeling is simulation run time. The simulation times of HSPICE, macro, and mathematical model are 68.09 second, 2.90 second, and 0.15 second, respectively. The results show that the simula-

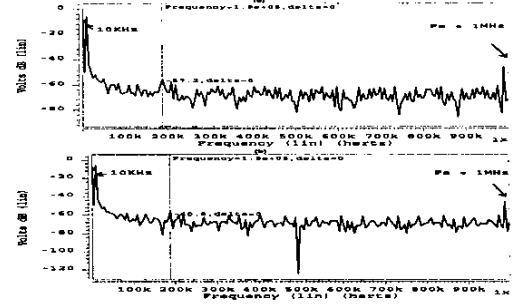


Fig. 9. Power spectrum analysis of 10KHz sine wave from (a) HSPICE simulation, (b) macro model; The frequency range is from DC to sampling frequency.

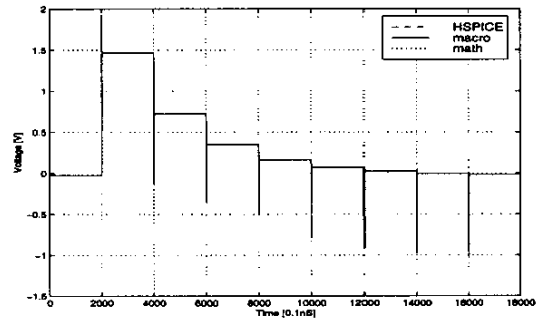


Fig. 10. Output signal from DAC circuit, macro model, and mathematical model

tion run time using the mathematical model is 453.9 times faster than that of HSPICE simulation, and simulation run time using macro model is 19.3 times faster than that of HSPICE simulation.

V. CONCLUSION

The macro and mathematical modeling techniques of DAC are proposed. These models provide an accurate and fast results in analog and digital circuit simulation environment. The previous models require bit skew time and internal parasitic components or complex mathematical procedures. However, our proposed method starts from the observation of output signal and use the wavelet theory with three basis functions. Therefore, our proposed modeling methodologies provide faster modeling turn-around-time comparing to the previously results.

REFERENCES

- [1] J. V. et al. Behavioral model of reusable d/a converters. *IEEE Transactions on Circuits and Systems*, 46(10):1323–1326, October 1999.
- [2] S. Palnitkar. *Verilog HDL*. Prentice Hall, New Jersey, 1996.
- [3] M. Software. *HSPICE User's Manual*. Meta Software, Inc., CA, 1996.
- [4] M. Thuillard. *Wavelets in Soft Computing*. World Scientific, Singapore, 2001.
- [5] J. J. Wikner and N. Tan. Modeling of cmos digital-to-analog converters for telecommunications. *IEEE Transactions on Circuits and Systems*, 46(5):489–499, May 1999.