

A CMOS LOW-POWER LOW-OFFSET AND HIGH-SPEED FULLY DYNAMIC LATCHED COMPARATOR

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ABSTRACT

This paper presents a novel dynamic latched comparator that demonstrates lower offset voltage and higher load drivability than the conventional dynamic latched comparators. With two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage is improved. The complementary version of the regenerative latch stage, which provides larger output drive current than the conventional one at a limited area, is implemented. The proposed circuit is designed using 90nm CMOS technology and 1V power supply voltage, and it demonstrates up to 19% less offset voltage and 62% less sensitivity of the delay to the input voltage difference (17ps/decade) than the conventional double-tail latched comparator at approximately the same area and power consumption.

I. INTRODUCTION

Due to fast speed, low power consumption, high input impedance and full-swing output, dynamic latched comparators are very attractive for many applications such as high-speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers. However, an input-referred latch offset voltage, resulting from threshold voltage V_{th} , current factor $\beta (= \mu C_{ox} W/L)$ and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of those comparators [5], [6]. A lower input-referred latch offset voltage can be achieved by using the pre-amplifier preceding the regenerative output-latch stage. However, the pre-amplifier based comparators suffer both from large power consumption for a large bandwidth and from the reduced intrinsic gain with the reduction of the drain-to-source resistance r_{ds} due to the continuous technology scaling [7].

With the aforementioned advantages, the dynamic comparators presented in [1, 2] have been

widely used. However, since this comparator has one tail transistor which limits the total current flowing through the both of the output branches, it shows strong dependency on speed and offset voltage with different common-mode input voltage V_{com} [2]. To mitigate this drawback, the comparator with separated input-gain stage and output-latch stage was introduced in [3]. This separation made this comparator have a lower and more stable offset voltage over wide input common-mode voltage (V_{com}) ranges and operate at a lower supply voltage (V_{DD}) as well. However, since it requires both Clk and $Clkb$ signals for its operation, high accuracy timing between Clk and $Clkb$ is required because the second stage has to detect the voltage difference between the differential outputs of the first gain stage at very limited time. The comparator from [4] without offset calibration technique resolved this problem by replacing $Clkb$ signal with the differential outputs of the first gain stage. As a result, Clk load was lessened and the input-referred offset was reduced as well since the gain for the output-latch stage was improved. However, the current drivability of the output load was weakened (and hence increased delay) because $Clkb$ signal was replaced with the output signal of the first gain stage that has a slower edge rate than $Clkb$, showing a slow exponential decaying shape, and the maximum drive current for each output was reduced to half of the single output tail current comparing to the comparator in [3].

In this paper, we present a new dynamic latched comparator which shows lower input-referred latch offset voltage and higher load drivability than the conventional dynamic latched comparators. The remaining sections of the paper are organized as follows. Section II provides the operation principle of the proposed comparator and the performance comparisons with the previous works, section III describes the optimization of the proposed comparator and the conclusion is followed in section IV.

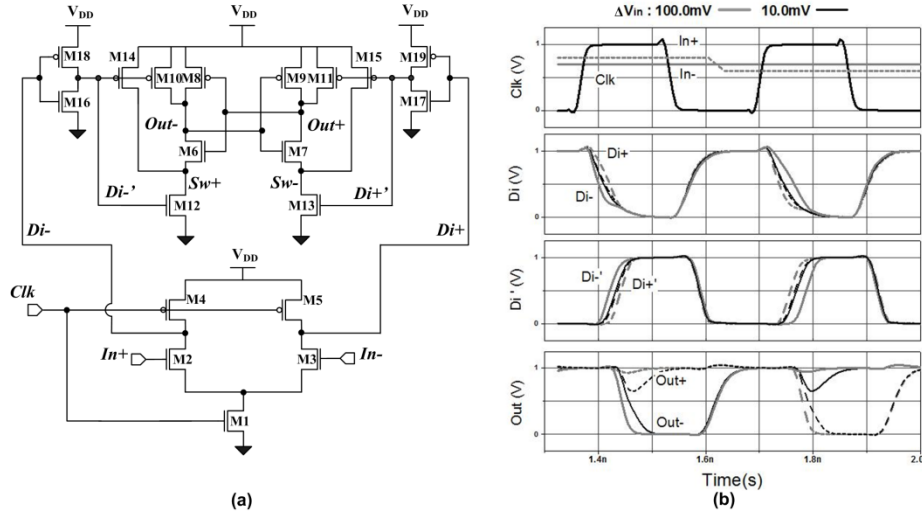


Figure 1 (a) Schematic of the proposed comparator; (b) Signal behavior of proposed comparator ($\Delta V_{in}=100mV$ (Grey), $10mV$ (Black) with $V_{DD}=1V$, $f_{clk}=3GHz$, $C_{load}=7fF$, $Temp.=25^{\circ}C$ and $V_{com}=0.7V$)

II. COMPARISONS WITH PREVIOUS WORKS

The schematic and simulated waveforms of the proposed comparator are shown in Figure 1. The circuit is designed and simulated with HSPICE using 90nm PTM (Predictive technology Model) [8] ($V_{DD}=1V$, $f_{clk}=3GHz$, $C_{load}=7fF$, $Temp.=25^{\circ}C$, and common mode voltage $V_{com}=0.7V$). The basic structure of the proposed comparator stems from the comparators from [3] and [4]. Therefore, the proposed comparator provides better input offset characteristic and faster operation in addition to the advantages of those comparators such as less kickback noise, reduced clock load and removal of the timing requirement between Clk and $Clkb$ over a wide common-mode and supply voltage range.

For its operation, during the pre-charge (or reset) phase ($Clk=0V$), both PMOS transistor M4 and M5 are turned on and they charge Di nodes' capacitance to V_{DD} , which turn both NMOS transistor M16 and M17 of the inverter pair on and Di' nodes discharge to ground. Sequentially, PMOS transistor M10, M11, M14 and M15 are turned on and they make Out nodes and Sw nodes to be charged to V_{DD} while both NMOS transistors M12 and M13 are being off.

During the evaluation (decision-making) phase ($Clk=V_{DD}$), each Di node capacitance is discharged from V_{DD} to ground in a different time rate proportionally to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between $Di+$ and $Di-$ node. Once either $Di+$ or $Di-$ node voltage drops down below around $V_{DD}-|V_{tp}|$, the additional inverter pairs M18/M16 and M19/M17 invert each Di node signal into the regenerated

(amplified) Di' node signal. Then the regenerated and different phased Di' node voltages are amplified again and relayed to the output-latch stage by transistor M10–M13. As the regenerated each Di' node voltage is rising from $0V$ to V_{DD} with a different time interval, transistor M12 and M13 turn on one after another and the final amplification is made between SW nodes before the regeneration process. Once either of SW node voltages falls below around $V_{DD}-V_{tn}$, the output-latch stage starts to regenerate the small voltage difference at Out nodes into a full-scale digital level: $Out+$ node will output logic high (V_{DD}) if the voltage difference at Di' nodes $\Delta Di'(t)$ is negative ($Di'+(t) < Di-(t)$) and $Out+$ will be low ($0V$) otherwise. Once either of Out node voltages drops below around $V_{DD}-|V_{tp}|$, this positive feedback becomes stronger because either PMOS transistor M8 or M9 will turn on.

To compare the performances of the comparators from [3], [4] with the proposed one in a fair way, each circuit was designed at a same area and designed to have the same transconductance for each input transistor pair (M2 and M3) by sizing their widths to $2\mu m$ and setting $C_D/I_{2,3}$ (Di node capacitance/drain current of M2 and M3) ratio constant. After setting the widths of the mismatch critical transistors to have relatively large size ($>1\mu m$), the rest sizes of transistors are optimized for high speed, low offset and less power consumption.

Figure 2 shows the simulated delay (ps) of each comparator versus the input voltage difference (V) with the different load capacitance of $7fF$ and $10fF$. The absolute delay was measured between the 30% of the rising Clk edge to the 70% of the rising output

Table 1: Performance Comparison

	Number of Transistors	Σ Width [μm]	Delay [ps] / $\log(\Delta V_{in})$	σ Offset Voltage [mV]	Energy [fJ] / Decision
Comparator [3]	14	20.6 μm	~ 33 ps/decade	20.1 mV	65.43 fJ
Comparator [4]	15	20.5 μm	~ 45 ps/decade	15.8 mV	58.43 fJ
Proposed Comparator	19	20.5 μm	~ 17 ps/decade	16.3 mV	59.20 fJ

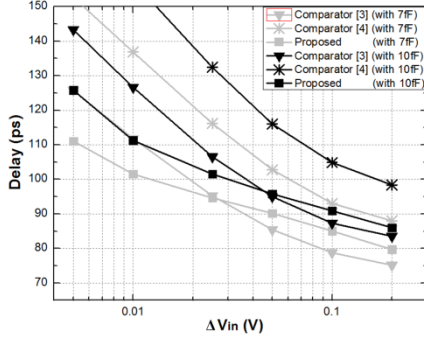


Figure 2 Simulated delay (ps) versus $\Delta V_{in}=|V_{in+}-V_{in-}|$ [V] with different load capacitances of 7fF and 10fF ($V_{DD}=1V$).

edge for the comparators from [3] and [4] and to the 30% of the falling output edge for the proposed comparator. Even with the additional inverter delays formed from transistor M16-19, the proposed comparator outputs faster decision over the comparator from [3] when the input differential voltage ΔV_{in} is less than around 25mV with 7fF capacitance load and less than around 50mV with 10fF capacitance load, which shows 62% less sensitivity of the delay versus the input voltage difference (17ps/decade) than the conventional double-tail latched comparator at approximately the same area and power consumption. As the size of the load gets larger, the proposed comparator shows better speed in general over the comparator [3] since the proposed comparator can drive more current to the load than the comparator [3] and [4] at the same area of the output-stage.

In order to compare the σ offset voltage of each comparator, random mismatch in threshold voltage V_{th} and current factor β ($=\mu C_{ox}W/L$) for each transistor pair were modeled as follows,

$$\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{WL}} \text{ where } W, L \text{ are in } \mu\text{m} \quad (1)$$

$$\sigma_{\beta} = \frac{A_{\beta}}{\sqrt{WL}} \text{ where } W, L \text{ are in } \mu\text{m} \quad (2)$$

$A_{V_{th}}$ and A_{β} are process dependent parameters and assumed to be $3\text{mV}\cdot\mu\text{m}$ and $1\%\cdot\mu\text{m}$, respectively in our mismatch analysis.

The overall performance comparison of each comparator is summarized in Table 1. The fifth column in Table 1 shows the resulting total offset voltages ($\sigma_{V_{OS}}$) for each comparator, which were obtained from 500 iterations of Monte Carlo transient simulations with 7fF capacitance load, $V_{com}=0.7V$ and $V_{DD}=1V$. The simulated result shows that the resulting V_{OS} of the proposed one is 16.3mV which is 3.8mV less than that of the comparator [3] and comparable with that of the comparator [4]. The second and third columns show the number of transistors and total channel widths of the transistors, which can be considered as approximate measures of circuit complexity and chip area. The fourth column is the delays (ps) per the input voltage differences ($\log(\Delta V_{in})$ or decade) of each comparator. The sixth and last column in Table 1 show that the proposed comparator consumes even less energy than the comparator [3] while presenting more stable $\text{delay}/\log(\Delta V_{in})$ and even less input-referred latch offset voltage at the same area.

III. OPTIMIZATION OF THE PROPOSED COMPARATOR

To further reduce the offset voltage of the proposed comparator, it is necessary to find the most critical mismatch transistor pair first. Since transistor M2 and M3 pair is the input transistors and starts to operate in the saturation region during evaluation phase, they are the most critical mismatch pair for the total offset voltage and the offset voltage caused by the mismatch between them can be expressed as [9]

$$V_{OS2,3}^2 = \left(\frac{V_{GS2,3} - V_{tn}}{2}\right)^2 \left\{ \left(\frac{\Delta C_{Di}}{C_{Di}}\right)^2 + \left(\frac{\Delta\beta_{2,3}}{\beta_{2,3}}\right)^2 \right\} + \Delta V_{tn2,3}^2 \quad (3)$$

Equation (3) shows that $V_{OS2,3}$ is affected by device mismatches and bias conditions. It implies that the total offset voltage increases directly proportional to the threshold voltage mismatch $V_{tn2,3}$ and also increases with the increase of the common mode voltage V_{com} , Di node capacitance mismatch (which is mostly the gate capacitance mismatch of the inverter pair), and the current factor $\beta_{2,3}$ mismatch. From (1)

and (2), it is clear that the offset voltage can be reduced by increasing transistor size.

In addition, to minimize the input-referred offset voltage of the output-latch stage, the gain of the dynamic preamplifier should be maximized. By assuming that $\lambda = \gamma = 0$ for simplicity, since both transistor M2 and M3 operate in the saturation region between the time t_1 and t_2 (t_1 : time at which transistor M1 is just turned on at the rising Clk edge and transistor M2 and M3 start to operate in the saturation region, t_2 : time at which either of transistor M2 or M3 moves out of the saturation region operation and goes into the linear region operation), the drain-to-source currents of M2 and M3 are constant over $[t_1, t_2]$. Therefore, the currents can be expressed as

$$C_{Di-} \frac{dV_{Di-}(t)}{dt} = -I_{D2} \quad C_{Di+} \frac{dV_{Di+}(t)}{dt} = -I_{D3} \quad (4)$$

By integrating both sides of (4) over $[t_1, t]$ and applying the initial condition: $V_{Di}(t_1) = V_{DD}$, the following equations are obtained;

$$V_{Di-}(t) = V_{DD} - \frac{I_{D2}}{C_{Di-}} t \quad V_{Di+}(t) = V_{DD} - \frac{I_{D3}}{C_{Di+}} t \quad (5)$$

By applying the small-signal approximation and assuming that $C_{Di-} = C_{Di+} = C_{Di}$, the dynamic gain of the differential input stage can be defined as

$$A_{V1}(t) \triangleq \frac{\Delta V_{Di}}{\Delta V_{in}} = -\frac{g_m}{C_{Di}} t \quad (6)$$

Equation (6) shows that as long as transistor M2 and M3 operate in the saturation region, the dynamic gain $A_{V1}(t)$ keeps increasing with the increasing time. To maximize the gain $|A_{V1}(t)|$, $|g_m/I_{D2,3}|$ should be maximized because the integration time t is proportional to $C_{Di}/I_{D2,3}$ from (5). This can be simply done with reducing the size of transistor M1. However, as equation (5) also indicates, the reduced $I_{D2,3}$ increases the discharging time of Di node voltages during evaluation phase. Therefore, the higher gain can be achieved at the cost of the increased delay.

Furthermore, by increasing the channel length of the input transistor, for example 90nm to 120nm in 90nm technology, one can get higher gain with the same $W_{2,3}/L$ ratio by reducing short-channel effects such as a dynamic conductance variation due to DIBL. If a negative supply voltage is available, by replacing the ground of the input differential pair with a negative supply voltage and further reducing the size of transistor M1, one can get wider common mode input range. Therefore, this differential input stage can be designed in a different way depending on the

requirements such as the speed, offset voltage and common mode input voltage range.

From the simulation results, the dynamic voltage gain up to around 12 V/V can be easily obtained, where around 1.7 times of the gain is produced by the inverter pairs (M18/M16 and M19/M17) followed by Di node gain of around 7 V/V. That means that the input referred offset voltage caused from the output latching stage mismatch is reduced by 12 (1.7 X 7) times. Therefore, the output-latch stage is relatively offset insensitive and does not need to be designed too big. Instead, the offset voltage caused from the mismatch between inverter pairs is the second dominant component of the total offset voltage and both pairs need to be designed big enough to meet the offset requirement.

IV. CONCLUSION

In this paper, we present a new low power dynamic latched comparator which shows lower offset voltage and higher output load drivability over the conventional double-tail dynamic latched comparator. It shows up to 19% less offset voltage and 62% less sensitivity of the delay to the input voltage difference ($delay/\log(\Delta V_{in})$), which is about 17ps/decade, than the conventional double-tail latched comparator at approximately the same area and power consumption.

REFERENCES

1. T. Kobayashi, K. Nogami, T. Shirotori and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," *IEEE J. Solid-State Circuits*, vol. 28, pp. 523-52, April 1993.
2. B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1148-1158, July 2004.
3. D. Schinkel, E. Mensink, E. Kiumperink, E. van Tuijl and B. Nauta, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," *ISSCC Dig. Tech. Papers*, pp. 314-315 and 605, Feb. 2007.
4. M. Miyahara, Y. Asada, P. Daehwa and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," in *Proc. A-SSCC*, pp. 269-272, Nov. 2008.
5. Jun He, Sanyi Zhan, Degang Chen, and R.L. Geiger, "Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 56, pp. 911-919, May 2009.
6. Nikoozadeh and B. Murmann, "An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 53, no. 12, pp. 1398-1402, Dec. 2006
7. B. Murmann *et al.*, "Impact of scaling on analog performance and associated modeling needs," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2160-2167, Sep. 2006.
8. <http://www.eas.asu.edu/~ptm/latest.htm>
9. B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY: McGraw-Hill, Inc., 2000.