

# A FAST AND PRECISE INTERCONNECT CAPACITIVE COUPLING NOISE MODEL

Young Jun Lee, Yong-Bin Kim

Electrical and Computer Engineering Department, Northeastern University  
yjlee@ece.neu.edu, ybk@ece.neu.edu

## ABSTRACT

This paper presents an accurate and fast method for calculating the time domain crosstalk noise for finite length on-chip distributed RC interconnect line. We begin with T. Sakurai's crosstalk noise model and develop the new model by fitting the equation to HSPICE simulation data. The developed model was applied to long wires ranging from 1000um to 8000um, and the experiments in realistic environment demonstrate that the error between HSPICE simulation and the analysis using the proposed model is within  $\pm 10$  percent for an 0.12um CMOS technology.

## 1. INTRODUCTION

Over the past few years the demand for higher speed integrated circuits has skyrocketed, and with the advancement in device and design technology, more and more devices are being integrated into a single chip. As a result, these technology trends induce many parasitic interactions such as capacitive and inductive coupling between interconnect wires. These interactions may cause faulty functional and timing behaviors on the silicon[1]. Therefore, in order to design well-performing integrated circuit, a designer should be able to forecast the coupling influence on chip functionality and timing from the early design stage.

To estimate RC crosstalk noise accurately, a circuit-level simulator such as HSPICE has been widely used[3]. However, it requires a considerable time to simulate RC crosstalk noise even for simple cases. When a new modern microprocessor that has hundred millions of interconnect wires and gates is considered, this is not a practical solution.

Therefore, several methods have been proposed to obtain RC crosstalk noise analysis[2][3]. The drawback of [2] is that the results of this approach turn out to be too pessimistic because parameters are overestimated to simplify the RC crosstalk noise analysis. Therefore, it could report too many unnecessary and unrealistic warnings. These warnings require a lot of time for scrutinizing. In order to avoid such time-consuming process, an accurate model is proposed in this paper.

In this paper, an improved and accurate RC crosstalk noise model is presented with simulation results. This ap-

proach is developed from Sakurai's formula[2]. Empirical factors are introduced to adjust the accuracy of the model based on HSPICE simulations. In order to verify the effectiveness of the new formula, a wire model of 0.12um CMOS technology was used for HSPICE simulation, and the simulation results were compared against analytic data from the developed model.

The main part of the paper is divided into three sections. Section 2 discusses Sakurai's formula and its drawbacks. The new formula and its results are described in Section 3. Section 4 presents the comparison between the results of Sakurai's formula and the results obtained from the proposed formula.

## 2. REVIEW OF SAKURAI'S FORMULA

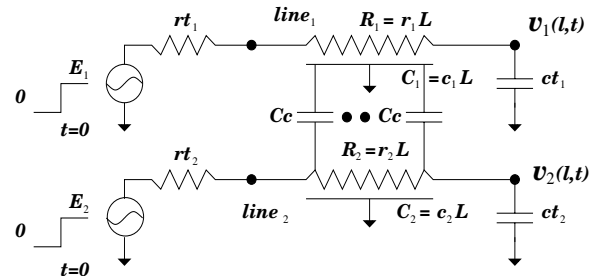


Fig. 1. Coupling capacitance wire model

T. Sakurai suggested closed-form expressions to estimate RC crosstalk noise[2]. Fig.1 shows a wire capacitive coupling model. This model consists of two wires - line 1 and line 2. The notations of this paper are summarized in Table 1. The Sakurai's formula is derived from the Equations (1) and (2) which can be set up from the Fig.1[2].

$$\frac{1}{r_1} \frac{\partial^2 v_1(l, t)}{\partial x^2} = (c_1 + c_c) \frac{\partial v_1(l, t)}{\partial t} - c_c \frac{\partial v_2(l, t)}{\partial t} \quad (1)$$

$$\frac{1}{r_2} \frac{\partial^2 v_2(l, t)}{\partial x^2} = (c_2 + c_c) \frac{\partial v_2(l, t)}{\partial t} - c_c \frac{\partial v_1(l, t)}{\partial t} \quad (2)$$

, where

$v_1(l, t)$  : the output voltage at line 1.

**Table 1.** Summary of Notations

Notation	meaning
$L$	Wire length
$r_{t1}, r_{t2}$	Input resistance of driving TR.
$c_{t1}, c_{t2}$	Output load gate capacitance
$c_1, c_2$	Wire capacitance per unit length
$r_1, r_2$	Wire resistance per unit length
$c_c$	Coupling capacitance per unit length
$R=rL$	Line resistance of wire
$C=cL$	Line capacitance of wire
$R_T$	$r_t/R$
$C_T$	$c_t/C$
$E_1, E_2$	magnitude of input voltage
Subindex 1,2	wire number

$v_2(l, t)$  : the output voltage at line 2.

Because these Equations do not have a closed-form solution[6], Sakurai introduced Equation(3) and (4) to simplify the equations.

$$v_+(l, t) = (v_1(l, t) + v_2(l, t))/\sqrt{2} \quad (3)$$

$$v_-(l, t) = (v_1(l, t) - v_2(l, t))/\sqrt{2} \quad (4)$$

Combining equations (1) through (4), Equations(5) and (6) are obtained.

$$\frac{\partial^2 v_+(l, t)}{\partial x^2} = rc \frac{\partial v_+(l, t)}{\partial t} \quad (5)$$

$$\frac{\partial^2 v_-(l, t)}{\partial x^2} = r(c + 2c_c) \frac{\partial v_-(l, t)}{\partial t} \quad (6)$$

, where  $c_1 = c_2 = c, r_1 = r_2 = r$ .

The solutions of the differential Equation(5) and (6) are obtained in the form of Equation(7) and (8)[4].

$$\frac{v_+(l, t)}{E_+} \simeq 1 + K_+ e^{-\sigma_+ t/rc} \quad (7)$$

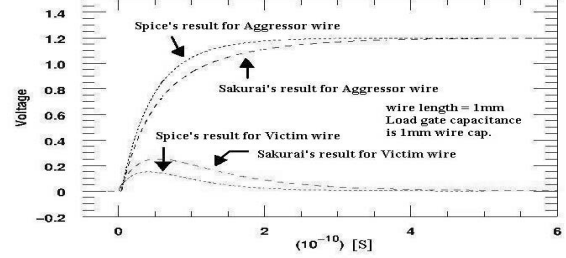
$$\frac{v_-(l, t)}{E_-} \simeq 1 + K_- e^{-\sigma_- t/r(c+2c_c)} \quad (8)$$

, where

$K_{+, -}$  and  $\sigma_{+, -}$  : the coefficients of the series expansion.  
 $E_+ = (E_1 + E_2)/\sqrt{2}, E_- = (E_1 - E_2)/\sqrt{2}$ .

Using Equation(3),(4),(7) and (8), the solutions of  $v_1$  and  $v_2$  are obtained as following.

$$v_1(l, t) \simeq E_1 + \frac{1}{2} [K_+(E_1 + E_2) \exp(-\sigma_+ \frac{t}{rc}) + K_-(E_1 - E_2) \exp(-\sigma_- \frac{t}{rc + 2rc_c})] \quad (9)$$



**Fig. 2.** Noise voltage for  $R_{T1} = R_{T2} \neq 0, C_{T1} = C_{T2} \neq 0$

$$v_2(l, t) \simeq E_2 + \frac{1}{2} [K_+(E_1 + E_2) \exp(-\sigma_+ \frac{t}{rc}) - K_-(E_1 - E_2) \exp(-\sigma_- \frac{t}{rc + 2rc_c})] \quad (10)$$

However, the variables of Equation(5) and (6) are not equal to those of Equation(1) and (2). Therefore, the variables of Equation(9) and (10) should be changed to obtain the solutions of Equation(1) and (2). To do this, Sakurai assumed that  $K_+ = K_- = K_1$  and  $\sigma_+ = \sigma_- = \sigma_1$ , and the voltages of the interconnect wires are given by Equation(11) and (12).

$$v_1(l, t) \simeq E_1 + \frac{K_1}{2} [(E_1 + E_2) \exp(-\sigma_1 \frac{t}{rc}) + (E_1 - E_2) \exp(-\sigma_1 \frac{t}{rc + 2rc_c})] \quad (11)$$

$$v_2(l, t) \simeq E_2 + \frac{K_1}{2} [(E_1 + E_2) \exp(-\sigma_1 \frac{t}{rc}) - (E_1 - E_2) \exp(-\sigma_1 \frac{t}{rc + 2rc_c})] \quad (12)$$

, where

$$K_1 = -1.01 \frac{R_T + C_T + 1}{R_T + C_T + \pi/4} \quad (13)$$

$$\sigma_1 = \frac{1.04}{R_T C_T + R_T + C_T + (2/\pi)^2} \quad (14)$$

$v_1(l, t)$  and  $v_2(l, t)$  are a function of wire length and time. Despite the fact that Equation(11) and (12) give us the analytic solution of crosstalk noise voltage, Equation(11) and (12) do not match with HSPICE simulation results unless that  $r_{t1}, c_{t1}, r_{t2}$  and  $c_{t2}$  are equal to zero. Fig.2 show HSPICE simulation and calculation results using Sakurai's equations. This figure shows disagreements between the Sakurai model and HSPICE results for this case. Therefore, Sakurai's assumption should be reviewed to validate the Equation(11) and (12).

First of all, Sakurai assumed  $c_{t1}$  and  $c_{t2}$  to be zero. These capacitances components contribute to the total output node to ground capacitance. If the capacitance of interconnect wire is sufficiently larger than that of load(long

wire case), the crosstalk noise voltage due to the load gate capacitance is negligible. However, in order to minimize the delay of long wires, buffers are usually inserted into long interconnect wires in real design. These buffers divide large wire capacitance into smaller ones. Thus, load gate capacitances should be considered to estimate the precise crosstalk noise voltage for short and medium length of wires.

Secondly, Sakurai assumed  $r_{t1}$  and  $r_{t2}$  to be zero. The value of  $r_{t1}$  and  $r_{t2}$  do not play a critical role in determining the magnitude of crosstalk noise. Despite the drawbacks of Sakurai's model, it has been widely used for signal integrity analysis. However, the signal integrity criterion becomes tighter as the technology goes into deeper sub-micron area. Therefore, there is a strong need to develop more accurate interconnect crosstalk noise analysis model and methodology.

### 3. PROPOSED FORMULA AND ITS RESULTS

In order to address the aforementioned problems, we propose the improved equations modified from the Equation(11) and (12). The new equations are obtained by modifying the Sakurai equation and fitting the curve to the HSPICE simulation data, and the best fitting curve is obtained in the form of Equation (15) and (16).

$$v_{1\text{new}}(\mathbf{l}, \mathbf{t}) = \frac{v_1(\mathbf{l}, \mathbf{t})}{(1 + \alpha)^{\frac{3}{2}}} + \beta\sqrt{(1 + \alpha)} \quad (15)$$

$$v_{2\text{new}}(\mathbf{l}, \mathbf{t}) = \frac{v_2(\mathbf{l}, \mathbf{t})}{(1 + \alpha)^{\frac{3}{2}}} + \beta\sqrt{(1 + \alpha)} \quad (16)$$

In order to include the effect of  $c_{t1}$  and  $c_{t2}$  in the crosstalk noise model, Equation(15) and (16) contain two factors -  $\alpha$  and  $\beta$ .  $\alpha$  is the coefficient to consider the effect of the ratio between the interconnect wire capacitance and load gate capacitance, and  $\beta$  is the heuristic coefficient to fit the model.  $\alpha$  is defined as  $C_{load}/C_{wire}$  and  $\beta$  is selected as 0.005. To verify this equation, we ran the extensive HSPICE simulation with 8 segment distributed  $\pi$  wire model of 0.12um CMOS technology. To simulate the circuit for various cases, the range of  $c_{t1,t2}$  value is changed from 0.125X of  $C_{1,2}$  to 1.5X of  $C_{1,2}$ , and the length of interconnect wires is changed from 1000um to 8000um. As for the input conditions of the entire HSPICE simulation, the resistance values of  $r_{t1,t2}$  are set to be equal to the resistance of 1mm interconnect wire, and  $E_1$  and  $E_2$  are set to be 1.2V and 0V, respectively. Fig.3 and Fig.4 show the results of HSPICE simulation and calculated results using the proposed approach. In these figures,  $C_W$  represents interconnect wire capacitance. The error ratios of these two results are shown in Fig.5. Simulation results are well matched with the proposed model within  $\pm 10$  percent error. If the  $\beta$  is selected

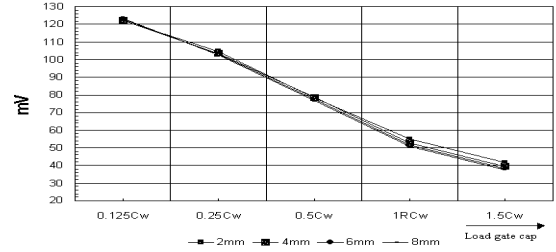


Fig. 3. Simulation Result (Noise voltage vs. Load gate cap)

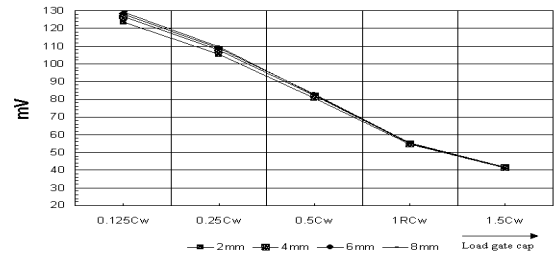


Fig. 4. Calculation Result (Noise voltage vs. Load gate cap)

very carefully, the error ratio can be reduced even further. Next, we ran the HSPICE simulations with three fixed  $C_{t1}$  and  $C_{t2}$ , which are 2X, 1X, 0.5X of the 1000um interconnect wire capacitance. The error between the simulation and calculated results using the proposed model is within  $\pm 7$  percent. These simulation results are shown in Fig.6, Fig.7, Fig.8 and Fig.9.

### 4. COMPARISON WITH SAKURAI'S RESULT

A set of simulation has been run for a fixed load gate capacitance using Sakurai's approach, and the simulation results are compared with our proposed approach for the same load gate capacitance. The comparison is shown in Fig.10. Our proposed model matches better, especially in relatively shorter wire cases. The Sakurai's model works fine for the long interconnect wire crosstalk noise analysis. However,

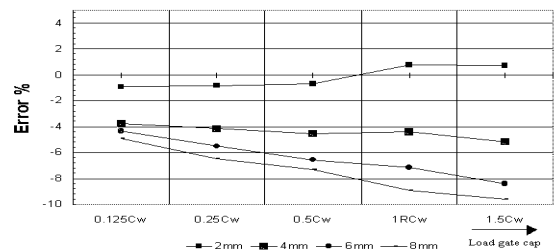


Fig. 5. Error ratios between Fig.3 and Fig.4

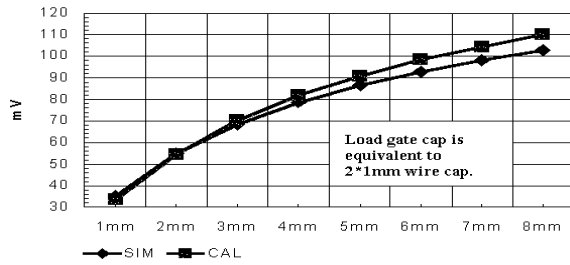


Fig. 6. Noise voltage vs. Wire length (when load gate cap is equivalent to 2\*1mm wire cap)

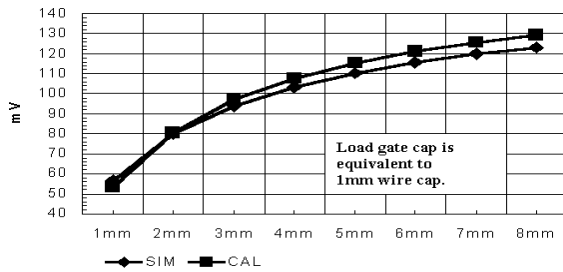


Fig. 7. Noise voltage vs. Wire length (when load gate cap is equivalent to 1mm wire cap)

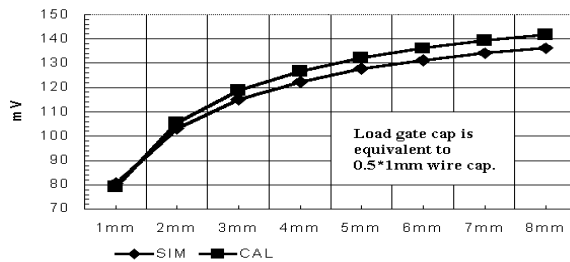


Fig. 8. Noise voltage vs. Wire length (when load gate cap is equivalent to 0.5\*1mm wire cap)

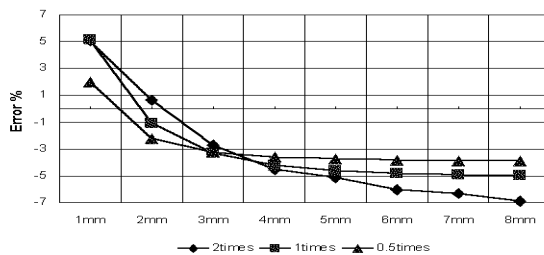


Fig. 9. Error ratios of Fig.6, Fig.7 and Fig.8

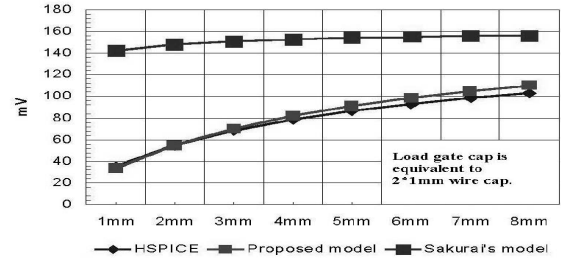


Fig. 10. Noise Voltage comparison using Sakurai's formula and proposed formula

the Sakurai's formula cannot be used effectively for short and mid range length of interconnect wires since the accuracy of the model deteriorates as the load gate capacitance becomes comparable to interconnect wires in those cases.

## 5. CONCLUSION

In this paper, we proposed a new closed-form equation for calculating crosstalk noise voltage in deep-submicron interconnect wires. It is shown that the model is more accurate than the conventional models for crosstalk noise voltage calculation, especially for short and mid range of wire length. Therefore, this model will help designers predict coupling noise more accurately for broader and more general cases compared to the conventional approaches, and reduce design turn-around time.

## 6. REFERENCES

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