

CMOS SENSOR INTERFACE FOR A ROBOTICS LAN

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ABSTRACT

This paper describes a CMOS design for interfacing low-level analog levels from sensors to a robotics network. This interface IC contains analog signal conditioning, 8-bit ADC, and protocol control for the interface between simple analog sensors and the LAN. The ADC uses a combination linear switched capacitor array and a resistor-string successive approximation register technique for conversion. A bandgap reference utilizes the vertical NPN device obtained using the substrate as a collector. Calculated analog and digital power dissipation are 4.1 mW and 8.1 μ watt/Hz, respectively. Technology is 3 μ double-polysilicon, single-metal for the 3.5 \times 4.0 mm² chip.

SPECIFICATION

A low power, mixed-mode IC is needed to interface simple pressure, temperature, humidity, and force sensors into a data acquisition network. The design goals are for

- Analog input levels 0–20 and 0–1000 mW
- 8-bit ADC with bandgap reference
- On-chip clock generator
- Photonic fiber optics network media
- Data bit rate 500 bps
- Chip power dissipation 5 mW nominal

CMOS p-well technology with double-polysilicon and single-level metal is selected to meet these design goals. Three-micron design rules are used for the digital layout and further relaxed rules for the analog layout. A 100 kHz on-chip clock generator is found to be optimum to meet the low-power-budget and the modest network bit-rate goals. A power supply with +5 and -5v levels is used.

CHIP ARCHITECTURE AND OPERATION

The chip block diagram of Fig. 1 shows the digital for control functions and analog for the IO sections. The control input to the chip is light sensed by the photodetector circuit. The control input is a manchester-encoded serial bit stream which contains the data request packet. The destination address contained within the data request packet is compared with the 10-bit ID which is derived locally from the ID pulse register (DIP switch or EEPROM). If the local ID matches the destination address in the data request packet, then an ADC conversion operation is initiated through the controller circuit and clocked by the on-chip oscillator. The ADC operation utilizes the SAR- and the capacitor-sections to be detailed in ADC Circuit Section. The voltage reference is used to obtain the absolute conversion levels. The dc sensor input is conditioned by an op amp circuit which has external-strappable gain control to accommodate the two input ranges 0–20 and 0–1000 mW.

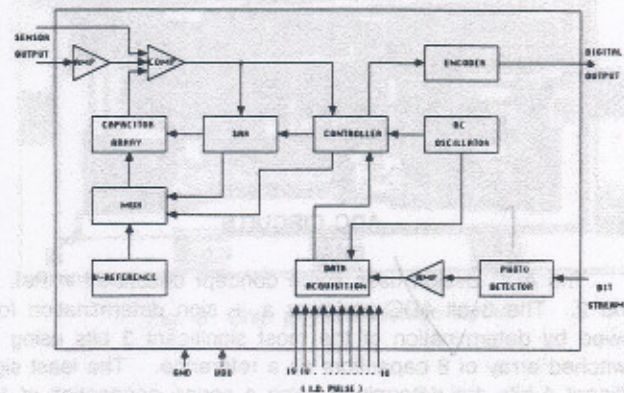


Fig. 1 Functional block diagram

A completed conversion is encoded into a sensor data packet which is output as a manchester bit-stream to the data network through an LED.

The chip functions are sequenced using the controller circuit, which is continuously active. A power down circuit reduces the ADC power dissipation during periods when conversions are not requested.

INPUT CONTROL PROCESSOR

Two series diodes are used to convert the incoming photon stream from optical fiber to the desired binary signals. In Fig. 2 the lower diode is exposed to light and the upper diode remains covered to incident light. The upper diode designed with a 10 \times periphery compared with the photodiode and acts as a pull up load device. This simple photodetection scheme is adequate at the low 500 bps data bit rates used here. The signal from the series-connected diodes is conditioned through a CMOS inverter to obtain a full rail-to-rail voltage swing.

The incoming manchester encoded bit stream contains an 8-bit ID which must be matched with the locally stored ID. The ID matching problem is made more difficult since the on-chip clock generator may be mismatched as much as 25% to the incoming 500 bps photonic stream. The circuitry used to match the ID bytes implements a detection algorithm which samples at 2 \times the nominal serial data rate using an up-down counter. When a match is found to the decoded ID, then control sequencing for the analog-to-digital conversion begins.

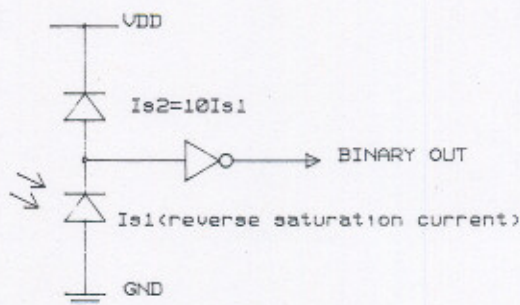


Fig. 2 Photodiode sensor circuit

ADC CIRCUITS

The ADC design uses some concept described in Ref. 1 and 2. The 8-bit ADC performs a \pm sign determination followed by determination of the most significant 3 bits using a switched array of 8 capacitors as a reference. The least significant 4 bits are determined using a series-connection of 16 resistors as a reference and with successive approximation sampling. Both sections provide the necessary reference voltage levels for the full 8 bit conversion.

The master reference V_{ref} is obtained from a differential bandgap reference circuit using a CMOS-compatible NPN transistor with a substrate collector.^{3,4} The circuit provides a V_{ref} of 1.283 v at the output of the feedback op amp.

The least significant 4 bits of data conversion are obtained by successively sampling the tapped resistor string of Fig. 3. Each of the 16 levels available from the resistor string are increments of the V_{ref} generated directly by the bandgap reference cell. In Fig. 3, the decision sequence used to generate the SAR INC levels is the standard successive approximation sequence often used in ADC circuits.

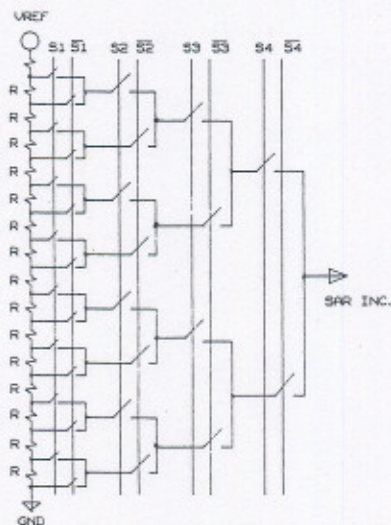


Fig. 3 Successive approximation 4-bit section.

The principle involved in the 3 most significant bit conversion is illustrated in Fig. 4a where the sampling capacitors $C\phi - C7$ are used to provide a V'_{ref} value incremented in steps of V_{ref} from 0 to V_{ref} . These 8 stepped reference levels are compared with the sampled analog input voltage levels to provide the basis for a 3-bit conversion.

The more complete MOS switch matrix is shown in Fig. 4b which includes the 8 capacitors of Fig. 4a. The analog reference level to the comparator (COMP IN) is sensed as either more or less than the analog input voltage at each of n_i to 8 comparison intervals.

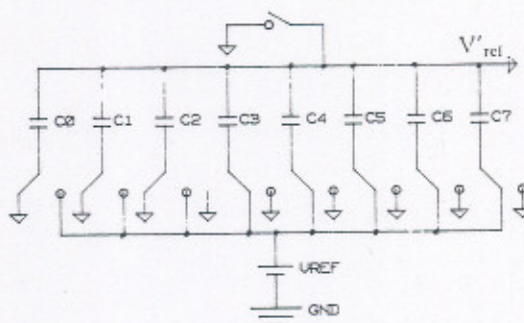


Fig. 4a Capacitor array for 3-bit MSB section

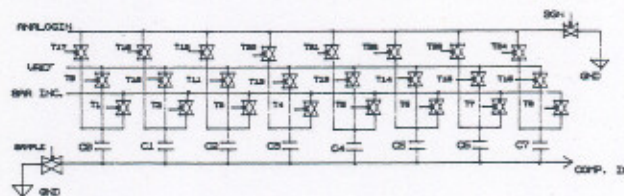


Fig. 4b Switching matrix for 3a

ON-CHIP CLOCK GENERATOR

The need for minimum size and low cost design dictated an on-chip clock generator.^{5,6} An RC oscillator with CMOS current steering provides an adequate low frequency source at 100 kHz. The circuit shown in Fig. 5 ramps a voltage level up on capacitor C to a level necessary to trigger a threshold of the differential pair Q_4 and Q_5 . The internal oscillation is a sawtooth waveform which is shaped to a square wave at OUT by the two CMOS inverters. The circuit components Q_1 , Q_2 , R_3 and R_4 provide the reference voltage for the Q_3 and Q_7 devices. Positive feedback is obtained in the Q_4 , Q_5 diff amp via the current mirror Q_3 and Q_7 .

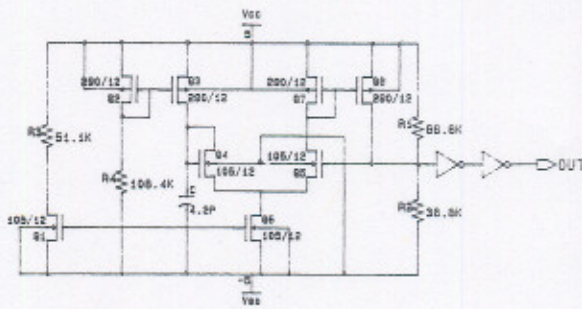


Fig. 5 On-chip clock generator

STATE CONTROL SEQUENCER

The state control sequencer provides control for the ADC and the digital IO functions. In the ADC described one comparison period is used for the sample and hold, one for \pm sign determination, 8 periods for the most significant 3 bits, and up to 4 periods for the least significant 4 bits. A maximum of 14 periods is needed to complete an ADC conversion. In addition a reset and enable serial output sequence is used.

The ADC conversion byte is stored in the output register which can operate as a shift register buffered into the chip serial output pin. An output packet consists of ten ID bits, a data byte, two parity bits. This output packet is the acknowledgment returned to the server node in the network when a data conversion is requested

CHIP LAYOUT

The composite layout plot is shown in Fig. 6. The completed design utilizes standard cells of 150 micron height and varying width. Input and output buffers are ESC protected. The technology used is a 3-micron critical dimension, double-level polysilicon for capacitors, and a single-level metallization. The technology is MOSIS foundry compatible with NMOS and PMOS threshold voltage levels of ± 1.1 volt. The chip measures 3.5×4.0 mm² with 18 bonding pads. Ten pins are used for the externally handwired node ID.

DISCUSSION

The IC design described meets the specification goals listed. The chip accepts inputs from a variety of semiconductor sensors with dc levels of a few millivolts (0-20 mV) and high level (0-100 mV). We are continuing work on characterizing the overall chip sensitivity: PSRR, temperature ambient, and offset control for this IC. We appreciate the help from Dr. Zheng Tang in the NJT Microelectronics Research Center.

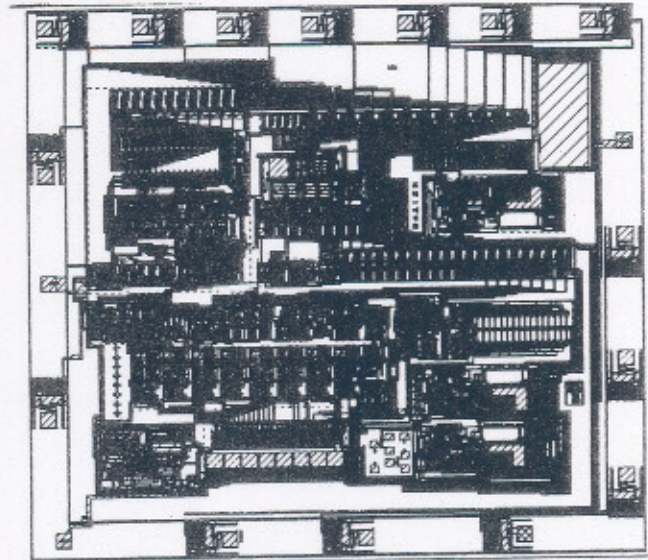


Fig. 6 Chip physical design layout

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