

A CMOS Subbandgap Reference Circuit With 1-V Power Supply Voltage

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Abstract—A CMOS subbandgap reference circuit with 1-V supply voltage is described. To obtain subbandgap reference voltages with a 1-V supply voltage, threshold voltage reduction and subthreshold operation techniques are used. Large ΔV_{BE} (100 mV) as well as a 90-dB operational amplifier are used to circumvent the amplifier offset. A power-on-reset (POR) circuit is used as startup. This circuit has been implemented using a standard 0.5- μm CMOS process, and its size is 940 $\mu\text{m} \times 1160 \mu\text{m}$. The temperature coefficient is 17 ppm from -40°C to 125°C after resistor trimming and the minimum power supply voltage is 0.95 V. The measured total current consumption is below 10 μA and the measured output voltage is 0.631 V at room temperature.

Index Terms—CMOS, current source, power-on-reset (POR) circuit, subbandgap reference voltage circuit, subthreshold operation, stability, temperature sensitivity.

I. INTRODUCTION

BANDGAP reference voltage circuits are one of the most widely used analog circuits in memory, analog-to-digital converter (ADC), and power management circuits [1]. As process technologies go into the deep-submicron eras and the demand for battery-operated portable equipment increases, supply voltage has to be scaled down. This low supply voltage requires new circuit technology for designing a bandgap reference voltage circuit because conventional bandgap reference voltage circuits require at least 1.25 V. Stable operation of bandgap reference circuits is difficult to obtain under 1.5 V because of voltage, temperature, and process variation (PVT variation) as well as design margin. To keep pace with supply voltage requirements of a state-of-the-art CMOS process, several subbandgap reference voltage circuits have been proposed [1], [3]–[6]. However, these circuits use nonstandard CMOS process options such as native transistors [1], [5], DTMOST [4], and BiCMOS [6]. These approaches also require specialized modeling and characterization that add cost in addition to the expense associated with extra mask layers and process steps. Thus, a subbandgap reference that can be implemented in a standard CMOS process is in high demand. A new design technique using subthreshold MOSFET was proposed in [2]. Although this technique requires no special devices and has a small area compared with previous subbandgap circuits, the temperature coefficient is large (119 ppm/ $^\circ\text{C}$) and the operating temperature range is narrow (-25°C to 125°C). Furthermore,

a capacitor taking a considerable area is required for stability compensation.

In this paper, a new subbandgap reference voltage circuit is proposed using a standard CMOS process; this novel circuit exhibits a wide operating temperature range and low temperature coefficient.

II. PROPOSED SUBBANDGAP REFERENCE VOLTAGE CIRCUIT

Threshold voltage (V_{TH}) is a major bottleneck to implement a subbandgap reference voltage circuit that operates under 1.2 V using a standard CMOS process. Though an advanced IC fabrication process can be used to implement a subbandgap voltage reference circuit, V_{TH} does not scale with any other process parameters due to leakage current, which is inverse-exponentially proportional to threshold voltage [7]. In this paper, two techniques are used to circumvent the V_{TH} limit. The first is a threshold voltage reduction technique using the transistor body effect. If the source potential is higher than the n-well substrate, V_{THP} is reduced and a bulk bias circuit applies an appropriate voltage to the substrate. However, V_{THN} cannot be reduced by this technique. V_{THN} is reduced by using large channel width transistor. Using this technique, V_{THP} and V_{THN} are lowered by 300 and 200 mV, respectively, in a 3-V CMOS standard process. In the proposed circuits, these techniques are applied to all pMOS transistors as well as to some nMOS transistors. The second technique to bypass V_{TH} 's bottleneck is to operate the circuit in the subthreshold region. In subthreshold operation, V_{TH} is no longer a significant bottleneck in subbandgap reference voltage design. In this paper, both techniques are used to accomplish design goals.

The fabrication process for the proposed subbandgap reference circuit shown in Fig. 1 is a standard four-metal n-well 0.5- μm CMOS process with a 6-V breakdown. The n-well sheet resistance has positive temperature coefficient, about 4000 ppm, which is cancelled to the first order in the bandgap application. The gate oxide capacitance C_{ox} is 2877 af/m², the slope factor is 1.7, and the channel length modulation factors λ_p and λ_n are 0.02 and 0.1, respectively.

The voltage–current characteristics of general diode is given by

$$I_D = I_S \left(e^{\frac{V_D}{V_T}} - 1 \right). \quad (1)$$

If $V_D \gg V_T$, (1) is approximated as

$$V_D = V_T \ln \frac{I_D}{I_S} \quad (2)$$

where V_D is the voltage across the diode, I_D is diode current, I_S is saturation current, and V_T is thermal voltage ($=kT/q$).

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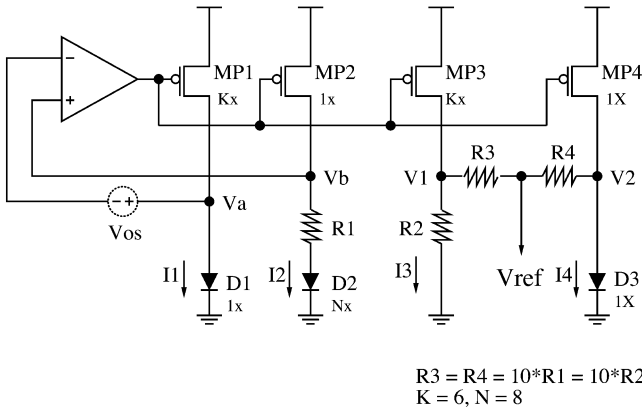


Fig. 1. Proposed bandgap reference voltage circuit.

Using (2), V_a and V_b in Fig. 1 are

$$V_a = V_{D_1} = V_T \ln \frac{I_1}{I_S} \quad (3)$$

$$V_b = I_2 R_1 + V_T \ln \frac{I_2}{N I_S} = V_a - V_{os} \quad (4)$$

where N is the area ratio of diode between D_1 and D_2 and V_{os} is the amplifier offset voltage.

Since $I_1 = K I_2$, I_1 can be expressed as

$$I_1 = \frac{K}{R_1} \{V_T \ln(KN) - V_{os}\}. \quad (5)$$

Choosing $I_1 = I_3$, $I_2 = I_4$, $R_1 = R_2$, and $R_3 = R_4$, V_{out} is now given by

$$V_{out} = \frac{V_{D_3} + \{K V_T \ln(KN) - V_{os}\} \times \frac{1}{1+R_2/R_3}}{1 + \frac{1}{1+R_2/R_3}}. \quad (6)$$

In this design $R_3 = R_4 = 10 \times R_2$, then the currents in R_3 and R_4 are negligible and (6) reduces to

$$V_{out} = \frac{1}{2} \times \{K V_T \ln(KN) + V_{D_3} - K V_{os}\}. \quad (7)$$

Therefore, the positive temperature coefficient of V_T and negative temperature coefficient of diode built-in voltage are compensated, and the output voltage of the subbandgap reference circuit is half that of a conventional bandgap reference voltage circuit.

The advantages of this circuit are as follows.

- 1) A large ΔV_{BE} reduces the effect of amplifier input offset [8]. In conventional bandgap reference circuits, ΔV_{BE} is around 54 mV (8:1 cathode area ratio). Using the cathode area and current mirror ratios, the ΔV_{BE} of the proposed circuit is 100 mV (48:1).
- 2) Since this approach uses an average voltage outside the feedback loop, it eliminates the stability problem due to loading inside the feedback loop.
- 3) The proposed architecture reduces the total sources of error to three component matching relationships between diodes, resistors, and pMOS. Conventional CMOS architectures require three or more resistor matchings and are heavily dependent on amplifier gain and the offset voltage to generate the V_{BE} and proportional-to-absolute-temperature (PTAT) components.
- 4) The matching quality is proportional to the device density. The active device matching is superior to passive device

matching due to the higher active area density. The area density of the active device is higher than that of the passive device because the active device can be interdigitated in a common centroid layout. However, some space is required between each resistor and capacitor. Consequently, the proposed solution to matching results in a significant improvement over conventional circuits.

The temperature dependency of the output reference voltage V_{D_3} [10] is

$$V_{D_3} = V_{G_o} - V_T \{(\gamma - \alpha) \ln T - \ln(EG)\} \quad (8)$$

where E and G are temperature-independent constants, $\gamma = 4 - n$ (n is a constant which is dependent on the doping level in the base of the bipolar transistor), and α is the exponent constant when the base-emitter current is dependent on temperature.

Using (7) and (8), and assuming zero offset voltage, the output voltage is given by

$$v_{out} = \frac{1}{2} \times \left\{ V_{G_o} + V_T (\gamma - \alpha) \left(1 + \ln \frac{T_o}{T} \right) \right\}. \quad (9)$$

For the proposed subbandgap reference circuit, a new PTAT current source shown in Fig. 2 is used. This current source is similar to a conventional PTAT current source [3] except for an additional operational amplifier (opamp). As a conventional PTAT source circuit shows poor performance due to process variation, this circuit has been slightly modified. Process-related sensitivities are significantly reduced due to the feedback provided by the opamp. In addition, when a conventional two-stage opamp operates in the subthreshold region [9] with the proposed current source circuit, the opamp shows a stable temperature performance since the temperature dependencies of the two circuits cancel out.

Conventional bandgap references have two stable operating states, given by *off* and the *bandgap potential*. To avoid a stable *off* state, a startup circuit is usually used [11]. When conventional startup circuits are used in a battery-powered system, the main issue is the continuous standby current. In ultralow-power applications, even microamperes are so important that the current consumption of the startup circuit should be zero when the subbandgap reference circuit is in operation.

Another issue in startup circuits is stability. When a second wraparound closed loop is used to implement a startup circuit, the potential for oscillation is greatly increased. Therefore, an open-loop startup circuit is advisable. To satisfy these requirements, the power-on-reset (POR) circuit shown in Fig. 2 has been designed. The basic principle of the POR circuit is the use of two RC circuits (M18–M19–C1, M12–C2) with different time constants. The comparison between these two time constants determines when the power is sufficiently high to ensure a proper subbandgap operation. When a battery is inserted into the system, node A approaches V_{dd} faster than node B. This voltage difference makes node C high and node D low. This is accelerated by positive feedback transistors (M16 and M17) acting as a latch. The output of the POR circuit is buffered and feeds the gate of M20.

The problem encountered with this type of POR circuit is that under heavy loading, the power supply glitch can shut the subbandgap circuit off and the POR circuit may not reset. This does not occur in this application for the three following reasons.

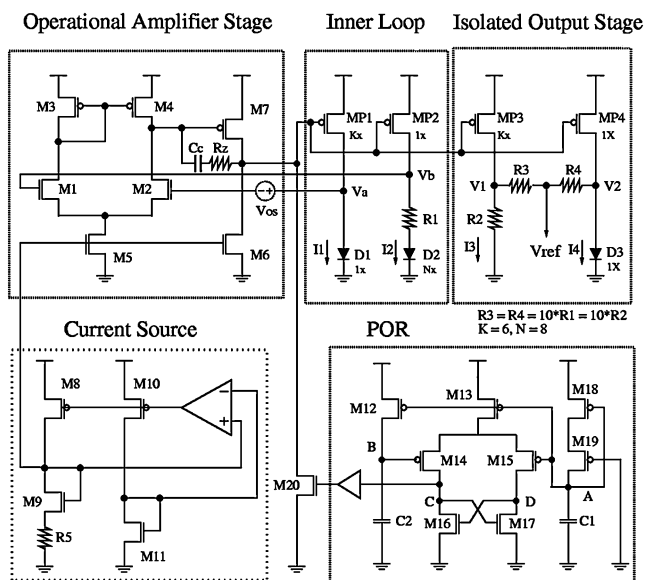


Fig. 2. Subbandgap reference voltage circuit.

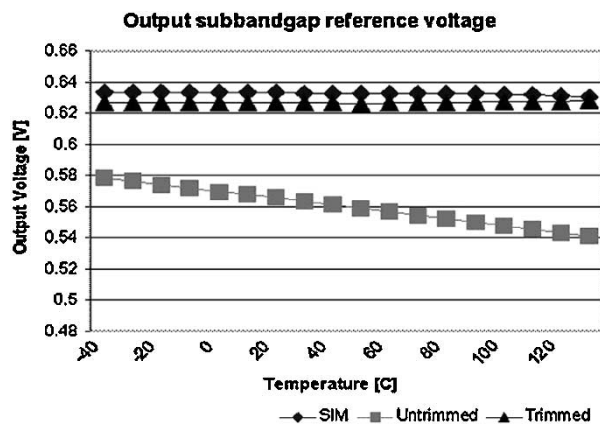


Fig. 3. Measured output voltage versus temperature.

- 1) Because the current consumption of our application is low, the magnitude of the glitch is small enough not to cause a problem.
- 2) Even if a glitch is likely, node capacitances retain charge and the power supply voltage drop is insufficient to shut off the bandgap circuit.
- 3) The glitch levels on the power line (either ground bouncing or ringing on the positive rail) are normally clamped by the source/drain-to-substrate diode, limiting the maximum excursion to less than a diode voltage drop in either direction.

III. EXPERIMENTAL RESULTS

The proposed subbandgap reference voltage circuit is implemented using a 0.5- μm standard CMOS process. The size of the subbandgap reference voltage circuit is 940 μm \times 1160 μm including subbandgap core circuit, current source, and POR circuit.

The measured output voltages for the test circuit with and without trimming and simulated output voltage of subbandgap

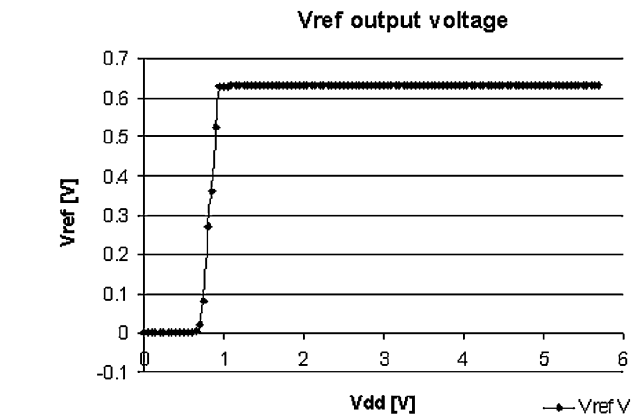


Fig. 4. Measured subbandgap reference voltage outputs versus V_{dd} .

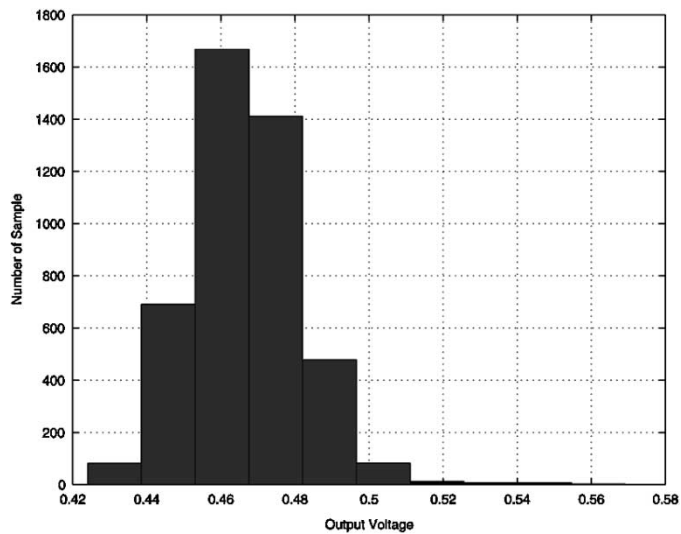


Fig. 5. Histogram of subbandgap reference circuit before trimming.

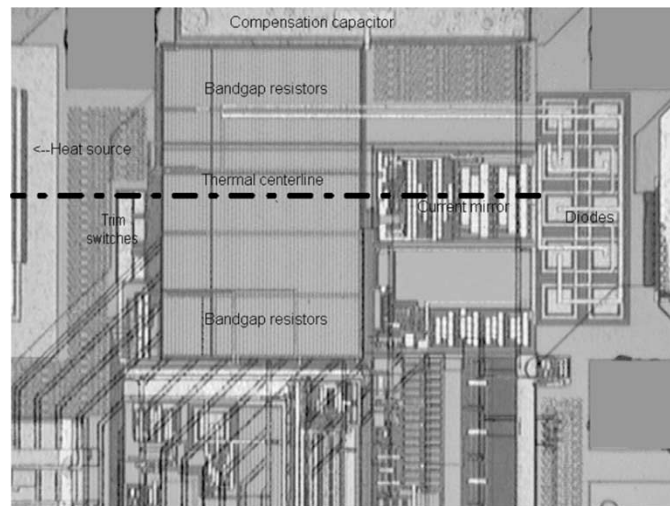


Fig. 6. Photograph of proposed subbandgap reference voltage circuit.

reference voltage are shown in Fig. 3. The maximum and minimum output voltages after trimming are 0.6268 V and 0.6283 V, respectively. The maximum current consumption is below 10 μA and the measured temperature coefficient is 17 ppm from -40°C to 125°C .

Fig. 4 shows the output voltage variation when the supply voltages change from 0–6 V with minimum operation at 0.95 V. Fig. 5 shows the histogram of the output voltage before trimming for 4437 samples. The center of the histogram is a slightly lower voltage due to amplifier offset. The microphotograph of the subbandgap reference voltage circuit is shown in Fig. 6.

IV. CONCLUSION

A new subbandgap reference voltage circuit which operates with very low power supply voltage has been proposed and verified using CMOS technology. V_{ref} is generated by the average of two voltages provided by the circuit out of the loop in the subbandgap core circuit. In this architecture, only one-to-one resistor matching is required, while one-to-three or higher matching ratio is commonly required for the conventional subbandgap reference voltage generator, resulting in improved matching. This architecture also helps reduce the sensitivity to amplifier gain and offset. Subthreshold circuit design techniques are aggressively used to achieve low power supply voltage operation and low power consumption. In the proposed architecture, the output voltage has a nonlinear term R_2/R_3 . If $R_1 = R_2 = R_4$ and R_3 is zero, then this nonlinear term vanishes.

A new current source is used to avoid PVT variation in the conventional current source output, and a POR circuit is used to reduce redundant current consumption and to secure the stability of the proposed subbandgap circuit.

The measured output voltage of the proposed subbandgap reference circuit is 0.628 V at the minimum operating power supply voltage of 0.95 V, and 0.631 V at nominal 3.3-V power supply. The maximum current consumption is below 10 μA , and the measured temperature coefficient of the designed circuit is

17 ppm from -40°C to 125°C after resistor trimming. The proposed subbandgap reference voltage circuit has been successfully applied to power management ICs.

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