

# CLOCK SKEW ON DRAM/LOGIC MERGED TECHNOLOGY BASED SYSTEMS

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## ABSTRACT

This paper describes the clock skew estimations considering all the possible clock skew factors on DRAM/Logic merged systems. The clock skew difference between standard logic chip and DRAM/Logic merged chips has been estimated as 521ps for  $4 \times 4 \text{ cm}^2$  die size. The relationship between clock skew and die size on DRAM/Logic merged systems has been obtained along with the maximum operating clock frequency assuming clock skew can take up to 15% of the total clock cycle on such a large chip.

## 1 INTRODUCTION

It has been suggested that DRAM component should be integrated on the same chip with a logic component that uses it. The actual memory bandwidth of a system is limited by off-chip interconnects. If they are integrated into a single chip, the memory access time is improved dramatically by utilizing the bandwidth available from internal arrays. Typically, there are less than two dozen off-chip interconnects available on a DRAM part, and for the densest DRAM technologies these interconnects provide typically something considerably 50MB/s of bandwidth per part. This is in contrast to the 1 to 2 GB/s bandwidth needed to support the core of most modern microprocessor. If one looks internally to the memory part, the actual bandwidth is much higher. Only a small percentage of the actual number of memory bits read from these internal memory arrays are actually made available off-chip. This limited bandwidth then causes designers of even higher performance CPU chips to spend more of their CPU silicon chip area and external glue logic on bandwidth acceleration and memory subsystem support circuits. DRAM/Logic merged technology now permits very significant amount of logic to be placed on DRAM chips, meaning that the bandwidth available from internal memory arrays can be utilized directly by one or more CPUs placed directly on the chip. The second advantage is power dissipation. If memory bus can be eliminated, almost of memory bus related power dissipation which is major portion of total power dissipation of the system can be removed.

As silicon fabrication technology develops, It is likely that embedded DRAM will become as common as embedded SRAM at some point. In fact, Neo Magic Corp. announced revolutionary graphics controller chip that embedded 1 Mb frame buffer on the die alongside the controller logic using an available 16Mb

DRAM process[1]. And a chip that merged 100K custom circuits and 4.5Mb DRAM onto a single die has been announced by Loral Federal Systems. However, any quantitative investigation has not been done about many open issues including clock skew.

To fully exploit the increase in computational power of such a large chip as DRAM/Logic merged system, the communication bandwidth within a chip must also be increased[2]. However, with a synchronous communication protocol, it is impossible to increase the communication clock speed without reducing the clock skew on chip. The clock skew is caused by different RC delay of clock interconnects along different clock signal paths and different delays of clock buffers due to process variations, temperature differences on the same chip, and power supply differences due to power rail IR drop. The H-tree clock structure has effectively provided a synchronous clocks to the elements on the large systems[3] [4]. However, as integrated circuits becomes larger and scaling decreases, the distributed resistance and capacitance of the interconnect will be much larger. Interconnects will have more buffers to reduce the dampening effect of the distributed RC lines on the shape of the clock signal. Buffers are needed to change the rise and fall time to minimize the amount of dynamic power dissipation of the system. It is therefore inevitable that clock networks in large system will have many buffers. This means that the chances of clock skew occurring in the distribution network will increase. The operating clock frequency will be limited by clock skew in a large system such as DRAM/Logic merged integrated circuit. And it will be valuable to investigate the clock skew quantitatively on DRAM process used for DRAM/Logic merged chip, and estimate the maximum clock frequency limited by clock skew of such a large system considering all the possible clock skew components.

## 2 CLOCK SKEW COMPONENTS

Techniques for synchronous clock distribution in large integrated circuit systems often utilize a tree-like structure with several levels of hierarchy. In fact, Dikaiakos and Steiglitz[5] have shown that the "tree" approach offers better control for signal distribution within long systolic arrays as compared with pipelined clocking schemes. There are five well known clock distribution networks. They are 3-Level Buffer Tree, H-Tree, Wide Trunk with Separate Sub-buffers, Wide Trunk with Connected Sub-buffers, and Separate Quadrants [6]. Among those clock distribution trees, the H-tree approach achieves minimal clock skew

at the expense of degraded edge rates since signals arrive simultaneously at each tree due to the symmetry of the layout. In a large system like DRAM/Logic merged systems, active buffers are placed between different hierarchical levels in H-tree clock distribution to minimize the problem associated with potentially large RC time constants of the interconnects [7]. A buffered version of the H-tree clock distribution is shown in Fig.1.

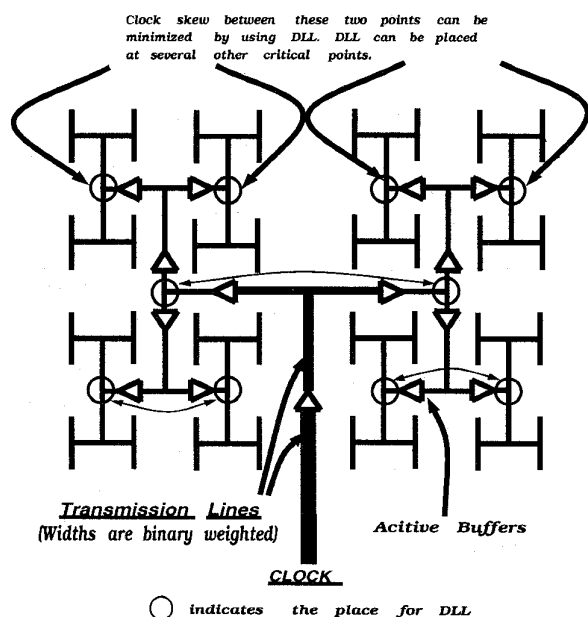


Fig.1. Buffered H-tree clock distribution.

However, clock skew is now influenced by process variations across the wafer which affects the speed of the individual buffers. For small die size, the RC time constant may not be so critical and regular H-tree clock distribution may be used without buffers, which eliminates almost half of the clock skew component due to process variations. But as die size increases the RC time constants of the interconnects become dominant and buffered version of H-tree clock distribution is required. The major clock skew component in the buffered H-tree clock distribution for large system such as DRAM/Logic merged chip is RC delay in a block. This is due to the fact that some blocks tap off clock right at the output of the clock buffer, while some other blocks tap off clock a distance away from the clock buffer. The second clock skew component is the skew due to process drift. The process parameters are not uniform across the wafer and different from one point to another even inside a chip. That causes a clock skew component. The third clock skew component is the clock skew due to temperature difference between one point and another. The commercial worst case temperature of a clock-gater when it is turned on is close to 110°C, while a gater that was off most of the time would be at 85°C for the worst case. This gives a temperature delta of 25°C. The fourth clock skew component is the clock skew due to power supply variations. For most of state-of-the-art Very Large Scale

Integrated systems, 200mV IR drop in VDD between distant blocks is assumed. And transistor level supplies are varied between 2.8V and 3.0V for 3V power supply design. The last clock skew component is the clock skew due to clock buffer loading difference. Clock buffer loadings are rated at  $\pm 25\%$  from the nominal load. This accounts for process variations and operator error in matching number of clock-gaters to blocks' clock loading.

Assuming that any given die would have temperature, VDD, and clock buffer loading all aligned worst-case at the same time, but the process drift in the transistors could be independent, the total clock skew is summed as

$$CK_{sk} = \sqrt{(S_P)^2 + (S_{Vdd} + S_{Temp} + S_{RC} + S_{Load})^2} \quad (1)$$

where  $S_P$  is the clock skew component due to process variation,  $S_{Vdd}$  is the clock skew component due to power supply variation,  $S_{Temp}$  is the clock skew component due to temperature variation,  $S_{Loading}$  is the clock skew component due to clock buffer loading variation, and  $S_{RC}$  is the clock skew component due to RC delay in the local block.

### 3 CLOCK SKEW ON DRAM/LOGIC MERGED CHIP

One of the major differences between standard logic process and DRAM process is that DRAM processes typically have only two metal layers while standard logic processes have at least four metal layers. Typically, the logic processes use the fourth metal layer for clock distribution because it has less RC time constant due to the metal thickness. If DRAM/Logic merged chip is to be implemented using DRAM process, clock will be distributed using the second metal of the DRAM process.

The distributed resistance and capacitance per unit square micron used for this research are 0.04Ω/μm<sup>2</sup> for the fourth metal of logic process and 0.09Ω/μm<sup>2</sup> for the second metal of DRAM process, 0.27ff/μm<sup>2</sup> for the fourth metal of logic process, and 0.26ff/μm<sup>2</sup> for the second metal of DRAM process. The state of the art microprocessors are designed to operate at several megahertz clock rate. In this speed range the traditional lumped-RC model can no longer provide sufficient modeling information about interconnections. Instead, a distributed or transmission line model needs to be used. A simple distributed RC pi model is used for this research. Fig.2 shows the RC delay vs. interconnect length characteristics for different metal layers. It shows that the fourth metal layer's RC delay is smaller than that of the second metal's RC delay by factor of two. The buffered H-tree clock distribution structure was built using 23μm wide the fourth metal for logic process, and 35μm wide the second metal for DRAM process for 4×4(cm<sup>2</sup>) die size considering metal migration requirements for 300MHz, 50pF loading, and two transition per clock cycle scenario.

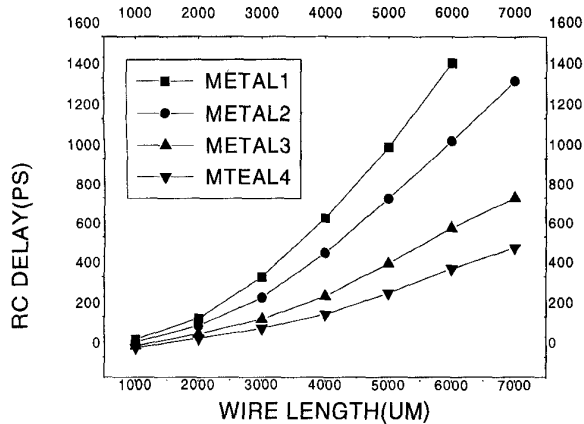


Fig.2 RC delay vs. interconnect length

The transistor sizes of the buffer driver was determined so that the rise time and fall time of the buffer output is not worse than 1.5 nsec.

The RC delay in a block can be found by measuring the delay from the clock buffer to the last point of clock interconnect. And the load dependent clock skew component is obtained by simulating with different load capacitance ( $\pm 25\%$  of nominal load) of the buffer. The clock skew component due to process variation can be obtained by simulating at discrete process points. The discrete process points used for this component are FAST, NOMINAL, and SLOW corners of the process with 2.8V power supply and nominal clock buffer load. As described in section 2, it is over worst case assumption that transistors are half-way between adjacent process points within a die. Therefore, it is necessary to divide the worst delay difference between process corners by statistical empirical number(four). Simulations have to be performed for different power supply(2.8V and 3.0V) for each process corner and the worst difference is picked for the clock skew component due to power supply IR drop. The last component is the clock skew due to temperature variation. It can be obtained by simulating the buffered H-tree circuit at different temperature(110°C and 85°C) for each process corner and picking the worst difference. Table 1 shows the clock skew component for standard logic process and DRAM process for  $4 \times 4 \text{ cm}^2$  die size.

Table 1. Clock skew components for DRAM and Logic process( $4 \times 4 \text{ cm}^2$  die)

$CK_{Comp}$	Logic Proc.(psec)	DRAM Proc.(psec)
$S_P$	404	163.25
$S_{Vdd}$	143	214
$S_{Temp}$	95	276
$S_{Load}$	148	306
$S_{RC}$	258	475
Total	760.2	1,281

As shown in Table 1 the major clock skew component for DRAM process is RC delay from the clock buffer to the final destination of clock interconnect of the block.

The resistance of the second metal is larger than that of the fourth metal in logic process, and the capacitance loading of the interconnect of the second metal in logic process is larger than that of the fourth metal in logic process, because the metal width has to be wider for electromigration issue. Consequently, RC delay of the interconnect on DRAM process is worse than that of logic process. Furthermore, those larger capacitance of the clock interconnect undermines the clock buffer driving capability, which in turn, degrades load dependent delay and makes the buffer delay more sensitive to temperature, power supply and process variations. Table 2 shows the clock skew components and total clock skew for different die sizes on DRAM process. The clock skew component due to RC delay in the block and load capacitance variation becomes dominant as die size increases. Assuming that the clock skew can take up to 15% of the total clock cycle time, the maximum operating frequency of DRAM/Logic merged chip is plotted as a function of die size in Fig.3.

Table 2. Clock skew vs. die size

-	$2 \times 2 (\text{cm}^2)$	$3 \times 3 (\text{cm}^2)$	$4 \times 4 (\text{cm}^2)$	$5 \times 5 (\text{cm}^2)$
$S_P$	157psec	158psec	163psec	192psec
$S_{Vdd}$	196psec	144psec	214psec	222psec
$S_{Temp}$	157psec	130psec	276psec	221psec
$S_{Load}$	78psec	175psec	306psec	337psec
$S_{RC}$	125psec	349psec	475psec	1,048psec
total	730psec	813psec	1,281psec	1,838psec

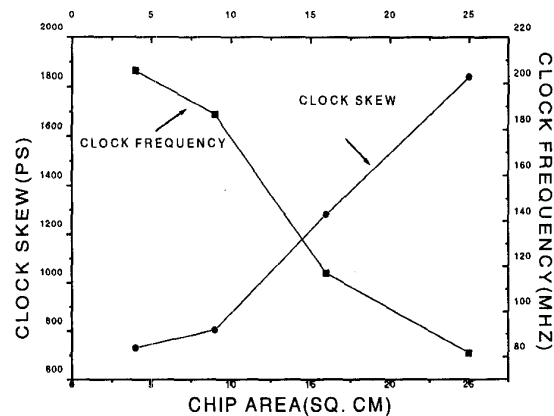


Fig.3 Clock skew and maximum clock frequency vs. die size

Fig.3 shows that the maximum clock frequency on  $2 \times 2 (\text{cm}^2)$  die is 220MHz with 712PS clock skew and the maximum clock frequency on  $5 \times 5 (\text{cm}^2)$  die is 80MHz with 1,812PS clock skew. Clock skew is defined as the difference between the arrival times in the terminals of the clock powering tree. Clock skew is very probable in large systems, and will have an increasing impact on system performance as frequencies and chip sizes

get larger. Communications between processing element is inhibited by clock skew. By reducing clock skew introduced to a system, the clock speeds can be increased for higher performance.

#### 4 CONCLUSION and DISCUSSION

This paper has shown the total clock skew and each clock skew component consisting the total clock skew for different die sizes on DRAM/Logic merged chip. The total clock skew on DRAM process has been compared with that of logic process for  $4 \times 4$  ( $cm^2$ ) die size to give a insight of how much clock skew will be when DRAM/Logic merged circuits are implemented using DRAM process. It was shown that the clock skew on DRAM process is larger than that of standard logic process due to the larger distributed resistance and capacitance of the second metal of DRAM process. Circuit techniques such as Phase Locked Loop(PLL) and Delayed Locked Loop(DLL) may become necessary to reduce the total clock skew by employing the circuit in several critical points of the H-tree clock structure. The circuit technique to reduce the total clock skew will improve the maximum operating clock frequency on DRAM/Logic merged integrated circuit design. However, PLL and DLL as they exist now may subject to supply voltage and temperature fluctuations as analog circuits are more susceptible to these fluctuations. Furthermore, with the increase in die size, more than one on-chip PLL or DLL may be necessary. Therefore, the complexity and silicon area may become an critical issue. New circuit techniques to better handle the clock skew problem is necessary in the near future.

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