Analysis and Measurement of Timing Jitter Induced by Radiated EMI Noise in Automatic Test Equipment

Y. J. Lee, *Student Member, IEEE*, T. Kane, *Member, IEEE*, J.-J. Lim, *Student Member, IEEE*, L. Schiano, *Student Member, IEEE*, Y.-B. Kim, *Senior Member, IEEE*, F. J. Meyer, *Member, IEEE*, F. Lombardi, *Senior Member, IEEE*, and S. Max, *Senior Member, IEEE*

***Abstract*—This paper deals with the generation, measurement and modeling of the jitter encountered in the signals of a testhead board for automatic test equipment (ATE). A novel model is proposed for the jitter; this model takes into account the radiated electromagnetic interference (EMI) noise in the head of an ATE. The RMS value of the jitter is measured at the output signal of the testhead board to validate the proposed model. For measuring the RMS value, a novel circuitry has been designed on a daughter board to circumvent ground noise and connectivity problems arising from the head environment. An H-field is applied externally at the loop filter of a phase-locked loop (PLL), thus permitting the measurement of the RMS jitter to verify the transfer function between radiated EMI and jitter variation. The error between measured and predicted jitters is within a 15% level at both 200 kHz and 500 kHz.**

***Index Terms*—Automatic test equipment (ATE), daughter board design, jitter measurement, jitter modeling, testhead board.**

I. Introduction

RECENT ADVANCES in high integration circuit design must meet new requirements in manufacturing and design to ensure the efficient design and test of large VLSI circuits and boards. These are particularly important considerations for keeping the overall cost per chip at a level compatible with today's competitive markets. This is vital for applications like consumer electronics, for which new design paradigms [such as systems-on-chip (SoCs)] are emerging rapidly as innovative solutions.

To meet these challanges, automatic test equipment (ATE) architectures have undergone a radical change in operation and design [1]. Past ATE architectures were based on shared resources [i.e., all channels shared the different components of a ATE, such as test processor, pattern generator and timing generator (TG)]. These architectures have quickly become obsolete; in the last decades, so-called per-pin architectures have been implemented as first stage of ATE evolution. In a per-pin ATE architecture, each channel has its own TG to provide flexible test signal generation; in this architecture, all components except the test processor are integrated on a single board. Recently, ATE architectures have been designed as per-pin test Pprocessor architectures in which nearly all system components are integrated onto a single chip.

This evolution provides excellent test flexibility, compact physical packaging (i.e., a smaller space to install a ATE of reduced size) and has lowered the test cost per chip. However, the output signal integrity in these ATE systems has become a critical issue, because the clock speed of the ICs under test have entered the gigahertz region. As ATEs provide the necessary instrumentation for the generation of tests and signals to device-under-test (DUT) with high operating frequency, jitter has become a critical feature to consider [2]. Moreover, as a number of chips might be simultaneously tested on a ATE, and as testing involves many pins on the same chip, pin-to-pin timing variation has grown in importance as part of ensuring integrity of signals. This is a tighter requirement with submicron technology due to the susceptibility of embedded circuits to new failure modes by clock-skew, crosstalk noise, ground bounce by parasitic inductance and jitter variation. While clock-skew, crosstalk, and ground problems are well known to circuit and board designers, jitter variation due to radiated electromagnetic interference (EMI) from switching power supplies or other EMI sources is a emerging problem. In design of testhead board for next generation ATE system, various dc-dc converters, which are regarded as a major radiated EMI source, are required to allow more integration of circuitry onto a testhead board.

The goals of this paper are to provide the framework by which jitter variation due to radiated EMI can be predicted through an analytical model. A measurement methodology as well as a quantitative analysis method are proposed for the jitter due to radiated EMI. Experimental results are presented to validate the proposed methodology.

The remaining sections are organized as follows: Section II discusses the basic issues associated with the signal integrity problem and, in particular, the issues revolving around dc-dc converters and their electrical characteristics are outlined. A model and associated technique which is amenable to an analytical approach are introduced to predict the jitter caused by the radiated EMI from the converters. A methodology for measuring the jitter due to radiated EMI is proposed in Section III, followed by experimental results in Section IV. Finally, conclusions are drawn in Section V.

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Y. J. Lee, J.-J. Lim, L. Schiano, Y.-B. Kim, F. J. Meyer, and F. Lombardi are with the Electrical and Computer Engineering Department, Northeastern University, Boston, MA 02115 USA (e-mail: yjlee@ece.neu.edu; jlim@ece.neu.edu; lschiano@ece.neu.edu).

T. Kane and S. Max are with the LTX Corporation, University Avenue, Westwood MA 02090 USA (e-mail: thomas_kane@ltx.com; sol_max@ltx.com).

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II. Model and Analysis for Jitter Characterization

This section outlines the proposed model and analysis of the jitter due to radiated EMI noise in the testhead board of a ATE.

The block diagram of a simple testhead board in a ATE is shown in Fig. 1. The ATE consists of a power supply module, the chiller system, and a reference clock generator in addition to multiple testhead boards such as the one shown in Fig. 1.

The testhead board consists of memories, generators (test pattern and timing), pin electronics, and programmable parametric measurement unit functions. The memories store the test vectors and the measured data collected from the DUT. The pattern and timing generators provide patterns and timing signals, respectively. The pin electronics circuitry adds the timing and format information to drive the DUT pin while the programmable parametric measurement unit acquires the dc output signal from the DUT. A comparison takes place between expected data and the actual DUT pin signal. As for the considered sources of radiated EMI affecting the signal integrity, in this paper, we focused on on-board dc-dc converter. Although other EMI sources are in the testhead board, results from preliminary experiments showed dc-dc converters are the principal source of radiated EMI noise.

A. Signal Integrity Problem and DC-DC Converter

As the testhead board is made of various components whose supply voltage levels are much likely different, dc-dc converters are also required. Use of dc-dc converter has several advantages.

1) Its size is so small that it can be mounted on a printed circuit board (PCB).
2) It can generate virtually any desired voltage level, independently of the input voltage level.
3) It is usually cheaper and much more efficient than linear power supply modules.

However, converters may cause EMI in the testhead board due to its switching characteristics [3] and, as a result, the jitter of the test signal might be increased. As the operating frequency of an ATE is expected to increase and to operate in the gigahertz region, the timing margin of the test measurement decreases significantly. In general, the timing margin will become worse due to the increasing clock speed by which the ATE has to operate for testing the DUT. Eventually, the timing margin may have a catastrophic impact on the test outcome as a good DUT can be diagnosed as faulty due to jitter invalidating the measurement and the timing characteristics of the DUT. In this case, a good DUT could be erroneously be rejected from the fault-free batch.

Therefore, particular attention must be paid to EMI noise due to the dc-dc converters present on the testhead board.

A dc-dc converter transfers the energy from the input to an output in discrete packets. In a typical testhead board, the input voltage comes from a power supply (at 48 V) and the output voltages of some dc-dc converters are used. All dc-dc converters are typically step-down dc-dc converters, whose block diagram is shown in Fig. 2. This converter consists of a power transistor, a power diode, an inductor, and a capacitor. Additional circuitry is required to adjust the timing to maintain the output voltage. The *first order transfer function* of this circuit is given by [4]

$$\frac{V_o}{V_{\text{in}}} = \frac{t_{\text{ON}}}{T} \tag{1}$$

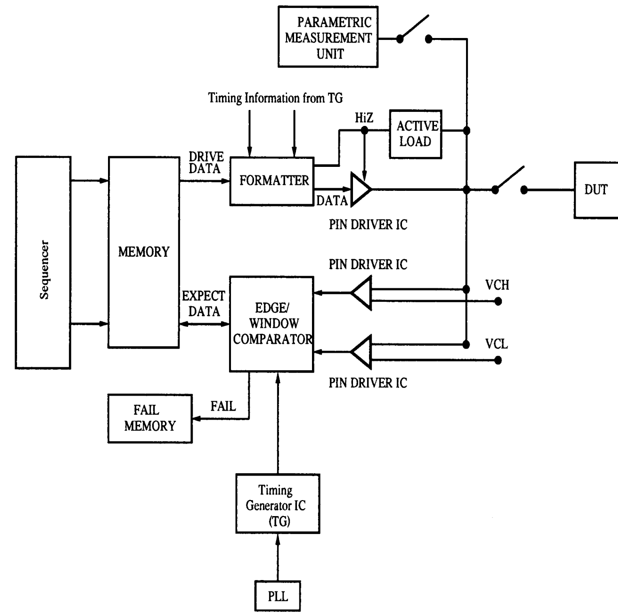

Fig. 1. Block diagram of an ATE system.

and the *duty cycle* is defined as

$$D = \frac{t_{\text{ON}}}{T} \tag{2}$$

where D is the duty cycle, T is the period of the switching signal, and t_{ON} is the ON period of the switching signal.

The *output voltage* can be expressed as

$$V_o = D \times V_{\text{in}}. \tag{3}$$

When the switching state is changed (from ON to OFF, or vice versa), the current is quickly changed in the transistor and the diode. This current may induce EMI noise, thus affecting the jitter.

B. Jitter Model

Jitter is usually defined as the *deviation* in the output transition of the clock from its desired (ideal) position. An extensive treatment of jitter can be found in [5], [6].

In this paper, a more restrictive characterization is required to take into account the testhead board as part of a ATE. In the testhead board, the radiated EMI affects the jitter in two different ways.

1) The radiated EMI directly affects the time location of a signal edge.
2) The edge location is indirectly affected by the radiated EMI.

1) Case 1: In the first case a direct relationship exists. The radiated EMI generates the noise voltage at the timing generation circuitry. This is analytically expressed as (4) below. This model is shown in Fig. 3 and is generally referred to as the "equivalent noise model" [6]

$$\Delta t_{\text{jitter}} = \frac{v_n}{S_R} \tag{4}$$

where S_R is the slew rate and v_n is the EMI induced voltage at the input of a circuit.

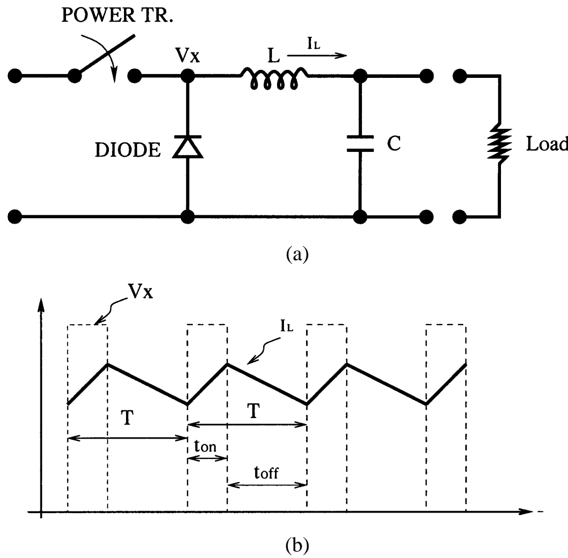

Fig. 2. Step down dc-dc converter (a) circuit diagram and (b) timing diagram.

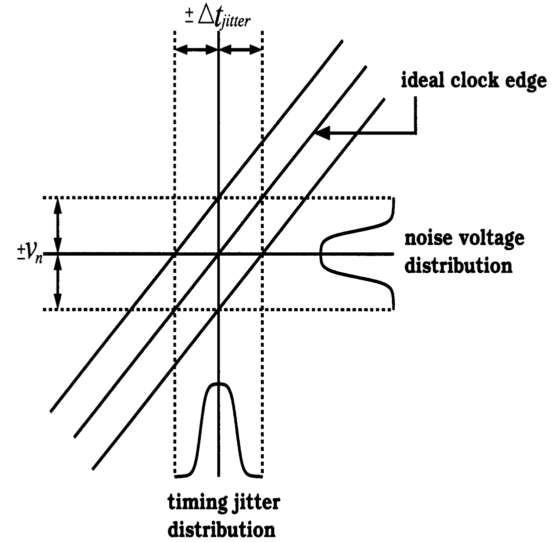

Fig. 3. Model of noise voltage.

When a noise voltage is imposed on an ideal clock edge, then this noise voltage causes a time shift of the clock edge. To calculate the jitter, the slew rate and induced noise voltage should be measured. The slew rate is measured using an oscilloscope. However, it is very difficult to measure the noise voltage caused by the radiated EMI for many reasons. For example, in the context of a ATE, the board in the head offers limited access for probing.

To obtain the noise voltage, Faraday's law is used in the proposed approach. Eq. (5) drives Faraday's law and a relationship between the H-field and the induced noise voltage can be established as follows:

$$V_{\mathrm{emf}} = -\frac{\partial \Psi}{\partial t} = -\frac{\partial(\int_s B \cdot S)}{\partial t} = -\frac{\partial \int_s \mu H \cdot S}{\partial t} \quad (5)$$

where Ψ is the magnetic flux, t is the time, V_{emf} is the induced voltage of the loop's ends, B is the magnetic flux density, S is the coupling area, H is the magnetic field intensity, and μ is the permeability.

If the H field from the dc-dc converter and the coupling area are known, then the noise voltage can be established, thus providing a solution for a measurement environment in the ATE. Note that (5) can be easily extended to the case of multiple radiated EMI sources (as applicable in our case due to multiple dc-dc converters).

2) Case 2: Just as the induced noise by the radiated EMI changes the node voltage of the testhead board, it may also change the jitter by propagating the noise voltage through the circuit gates. This voltage can be amplified or reduced depending on the noise propagation path of the circuits. To model this effect in an accurate fashion, the transfer functions of the noise propagation path must be developed.

This is expressed as

$$\Delta t_{\mathrm{jitter}} = f(v_n) \quad (6)$$

where $f(\cdot)$ is the transfer function of the noise propagation path and v_n is the noise induced by the radiated EMI.

From (4), (5), and (6), the jitter due to the radiated EMI is given by

$$\Delta t_{\mathrm{jitter}} = \frac{v_n}{S_R} = \frac{1}{S_R} \times \left(-\frac{\partial}{\partial t}\int_s \mu \mathbf{H} \cdot \mathbf{dS}\right) \text{ or } \Delta \mathrm{t_{jitter}} = \mathbf{f}(\mathrm{v_n}) \quad (7)$$

III. Experimental Setup

In this section, a methodology for measuring the jitter is proposed. This takes into account the model and analysis presented in the previous section. Moreover, to account for the rather compact nature and placement of the boards in the head of a ATE, a daughter board has been designed to aid in measuring the jitter; an extensive discussion of this methodology is also pursued.

To measure the jitter as affected by the radiated EMI on the testhead board, the following procedure is proposed.

1) **H-field measurement from the components of the testhead board.**
   To find a major radiated EMI noise source on the testhead board, the H-field is measured with a closed-field probe and a spectrum analyzer [7]. Based on the measured H-field, an external H-field is then applied to the testhead board to estimate the effects of the radiated EMI noise on the jitter. The measured results are used as reference values to validate the jitter model as presented in the previous section.
2) **H-field generation.**
   Using H-field and function generators, the H-field is forced along the test signal generation path which consists of the PLL, the clock distribution ICs, the timing generator IC, and the vernier IC.
3) **Jitter measurement.**
   By forcing the various H-fields to test the signal generation path, the jitter can be measured.
4) **Analysis.**
   The measured jitter is then compared with the calculated jitter and an error (if any) is recorded.

The four-step measurement procedure described above reflects the model and the analysis presented in the previous section, thus integrating into a few measurements the EMI induced noise and its effects on the jitter and its variations.

When measuring the jitter in testhead board, the following issues should be considered.

- **Connectivity:** When measuring the jitter, connections must be stable, or else consistent results cannot be guaranteed and experimental results are not trustworthy. If the timing margins are large, a small jitter is not critical. However, if the jitter requirement is in the picosecond region, a stable connection must be secured.
- **Ground noise:** Even though ground noise is not jitter, it can be regarded as such when timing is measured while ground noise is present. In this case, ground noise is derived from an unstable ground connection and an impedance mismatching. This occurs when the connections are made for jitter measurement and ground noise can change if the connection is unstable. Moreover, as ground noise is randomly changed, the measured results are much likely inconsistent.
- **Impedance matching:** As the testhead board is designed with a 50-Ω impedance matching transmission path, additional connections may impair impedance matching, thus resulting in an erroneous measurement. This unstable feature occurs when uncontrolled connections are made.

A daughter board has been used in our approach to overcome these problems, and this board is compatible with the testhead board and ATE operations. A circuit diagram of the daughter board which has been designed for the testhead board and jitter measurement in a ATE, is shown in Fig. 4 and its photography is shown in Fig. 5.

This circuit consists of a buffer circuit, a switching power supply module, several capacitors (power and coupling), and termination resistors.

In this figure, the input signal frequency is greater than 1 GHz and the power supply comes from the testhead board. The various components are described as follows.

- $C_{1,2}$ are ac coupling capacitance; $C_{3,4}, C_{5,6}$, and C_7 are used as power capacitors for the various power supplies.
- Some supply voltages come from the testhead board; The supply power for the buffer circuit is generated from the small switching power supply module on the board.
- $R_{1,2}$ are pull-down resistors, and their values are 187 Ω. $R_{3,4}$ are back-matching resistors whose values are 43 Ω; together with the internal 7-Ω resistance of the buffer, this accomplishes the 50-Ω impedance matching.
- As the board thickness is $0.063''$, the trace width to make a 50-Ω impedance is $0.110''$ [8].
- A MMCX connector has been used, because the space between the daughter board and the testhead board is very small.

IV. Experimental Results

To measure the H-field strength from the dc-dc converter, the following pieces of equipment are used in our experimental set-up: a closed field probe, a preamplifier and a spectrum analyzer.

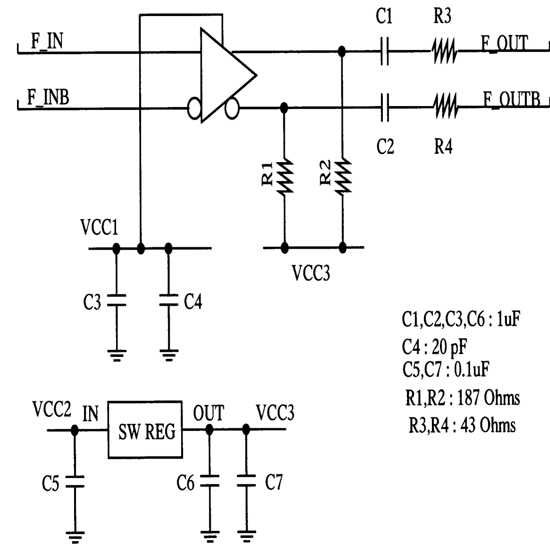

Fig. 4. Circuit diagram of the daughter board.

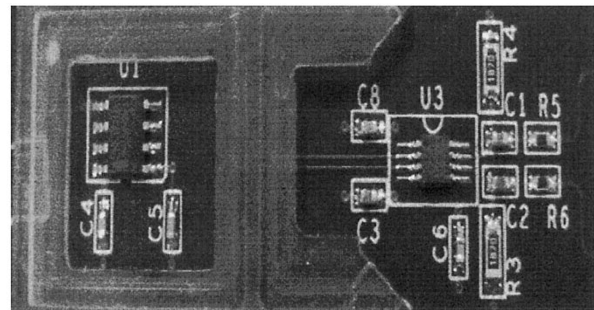

Fig. 5. Photography of the daughter board.

The measured results show that the peak of the H-field occurs at 200 kHz, which is the same as the switching frequency of the dc-dc converter. The experimental results obtained from our set-up are given in Table I.

Based on the measured results, the same values in dBμV for the H-fields are generated from an external H-field generator and applied to the testhead board to investigate its effects on the board. The experimental configuration for the measurement of the jitter is shown in Fig. 6.

After the experimental configuration is set up, an external H-field is forced to reveal the most sensitive part in the board. In the testhead board, all clock circuitry consists of fully differential clocking schemes, so the induced noise voltage from radiated EMI is tolerable. However, when the H-field is forced to the loop filter of the PLL, the measured jitter changes in proportion to the H-field strength.

Fig. 7 shows the loop filter of the PLL. In Fig. 7, R1, R2, C1, and $\mathrm{C_{in}}$ make a closed loop A whose size is $0.300'' \times 0.175''$. This area will be coupled with the external H-field such that it generates an induced voltage noise. This noise voltage is attenuated by the loop filter whose transfer function is given by

$$V_O = \frac{R_1 + Z_1 + SC_1R_1R_2 + SC_1R_2Z_1}{R_1 + SC_1{R_1}^2} \times V_a - \frac{Z_1}{R_1} \times V_b. \quad (8)$$

TABLE I
MEASURED H-FIELD FROM THE DC-DC CONVERTER

No.	Frequency[kHz]	Measured H-Field[dBμV]
1	198	62.28
2	198	52.04
3	204	61.58

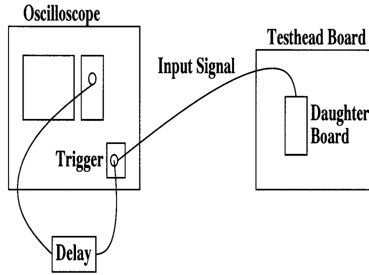

Fig. 6. Jitter measurement configuration.

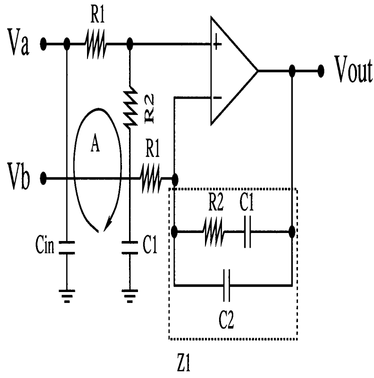

Fig. 7. Loop filter of phase-locked loop.

The output voltage of the loop filter generates a jitter because it changes the VCO input voltage. Using frequency modulation [10], this can be modeled as

$$y = \sin[2\pi f_{\text{clock}} \times t + 2\pi f(\text{VCO}) \times V_{\text{noise}} \times \sin(2\pi f_{\text{modul}} \times t)t] \quad (9)$$

where f_{clock} is the clock frequency, $f(\text{VCO})$ is the transfer function of the VCO, f_{modul} is the modulation frequency, and V_{noise} is the induced noise voltage.

The strength of the applied H-field and the measured RMS jitter are given in Table II.

Fig. 8 shows a 6.422 ps RMS jitter for a 96.33-dBμV external H-field at 500 kHz. In this figure, two peaks are observed because the signal is modulated by the frequency of the external H-field.

The discrepancy between theory and experimental results can be bounded to the following observations. 1) The considered H-field generaor is not the only externally electro-magnetic noise source. Various electrical equipments are required for the experiment, and their emissions may cause experimental error. 2) The noise voltage induced by radiated EMI may be larger than calculated result. In Fig. 7, the coupled area is formed by loop A. However, another loop near loop A may generate an additional induced noise voltage.

TABLE II
MEASURED JITTER AND CALCULATED JITTER USING THE MODEL [ps]

200[kHz]		
H-field [dBμV]	Measured Jitter	Calculated Jitter
78.53	2.509	2.316
84.58	2.997	2.426
90.51	2.734	2.574
92.35	2.986	2.646
500[kHz]		
87.15	2.457	2.258
92.95	3.226	3.178
95.98	4.210	3.750
96.33	5.311	4.589

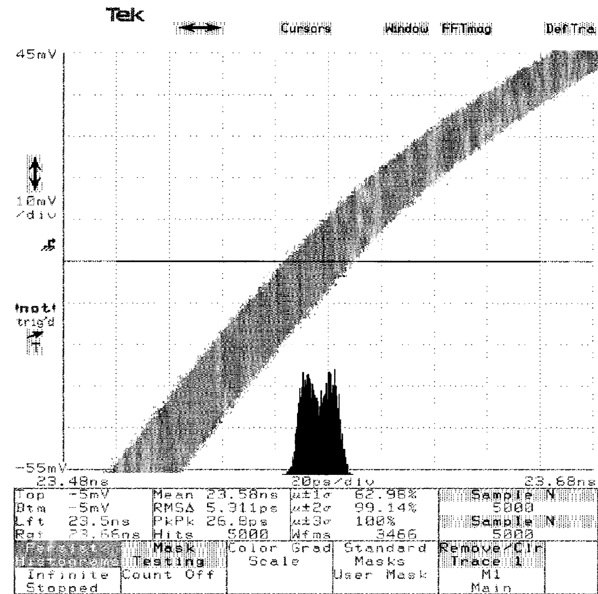

Fig. 8. Measured jitter with 96.33-dBμV, 500-kHz H-field.

V. CONCLUSION

The new generation of ATEs require high-frequency operation for testing high-performance devices-under-test with the appropriate signals; in these cases, jitter is a very critical measure that must be carefully considered. A new jitter measurement methodology which utilizes frequency modulation and a novel model for jitter prediction have been proposed in this paper. The proposed model takes into account the radiated electromagnetic induced noise (EMI) in the head of an ATE. It is well known that the dc-dc converter generates a high electromagnetic field, and it is a major EMI source; it has been verified using a spectrum analyzer in this experiment.

Due to the features in the operation of an ATE, the jitter was measured at the output of the testhead board using a daughter board. For measuring the RMS value of the jitter, a novel circuitry, which has been designed on a daughter board, is pro-

posed to circumvent ground noise and connectivity problems arising from the head environment.

When the H-field strength is applied and changed at the loop filter of the PLL, a jitter variation is observed; this follows a direct relationship with the applied H-field. This permits the measurement of the RMS jitter to verify the transfer function between radiated EMI and jitter variation.

The proposed model has been validated through an experimental setup. For a 96.33-dBμV external H-field at 500 kHz, the measured and predicted jitters are 2.457 ps and 2.258 ps, respectively; the measured and expected results show similar values in jitter.

It is anticipated that the framework provided by this research will be utilized to design ATEs and testhead boards that can operate at very high frequencies as applicable to today's ICs.

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Y. J. Lee (S'00) was born in Seoul, Korea, in 1968. He received the B.S. and M.S. degrees in electronic engineering from Yonsei University, Korea, in 1992 and 1994, respectively. He is currently pursuing the Ph.D. degree at Northeastern University, Boston, MA.

From 1994 to 2000, he was a Senior Design Engineer involved in micro-controller design, LCD controller design, and sound IC design at Samsung Electronics, Korea. Since 2000, he has been a Research Assistant in the Department of Electrical and Computer Engineering, Northeastern University. His research interests include high-speed, low-power VLSI circuit design, analog VLSI circuit design, and ATE system design.

T. Kane (M'95) received the B.S.E.E. M.S.PHYS. degrees from the University of Connecticut, Storrs, in 1994 and 1996, respectively.

He was with Thermawave, Fremont, CA, as a Field Applications Engineer involved in thin-film metrology equipment from 1997 to 2000. He is currently with LTX Corporation, Westwood, MA, as a Systems Analog Engineer. His current research includes ATE system design.

J.-J. Lim (S'02) received the B.S. degree from ChonBuk National University, Korea, in 1998. He is currently pursuing the M.S. degree in electrical and computer engineering at the Northeastern University, Boston, MA.

From January 1998 to December 2001, he was with Samsung Electronics, Korea, where he was responsible for the design of microcontroller and tester evaluation. His current interests include high speed circuits and low power systems.

L. Schiano (S'02) received the Laurea degree (*cum laude*) in electronic engineering from the University of Bologna, Bologna, Italy, in 2001. He is currently pursuing the Ph.D. degree in computer engineering at Northeastern University, Boston, MA.

From March 2001 to June 2002, he was a Fellow with the DEIS Department, University of Bologna. His research interests include IC testing, ATE design, and on-line testing.

Y.-B. Kim (SM'99) was born in Seoul, Korea, in 1960. He received the B.S. degree in electrical engineering from Sogang University, Seoul, Korea, in 1982, and the M.S. and Ph.D. degrees in computer engineering from the New Jersey Institute of Technology, Newark, and Colorado State University, Fort Collins, in 1989 and 1996, respectively.

From 1982 to 1987, he was a member of the technical staff at the Electronics and Telecommunications Research Institute, Korea. From 1990 to 1993, he was a Senior Design Engineer with Intel Corporation, involved in micro-controller chip design and Intel P6 microprocessor chip design. From 1993 to 1996, he was with Hewlett Packard Company, Fort Collins, as a member of the technical staff, involved in HP PA-8000 RISC microprocessor chip design. From 1996 to 1998, he was with Sun Microsystems, Palo Alto, CA, as an individual contributor, and involved in 1.5-GHz Ultra Sparc5 CPU chip design. From 1998 to 2000, he was an Assistant Professor in the Department of Electrical Engineering, University of Utah, Salt Lake City. He is currently a Zraket Endowed Professor in the Department of Electrical and Computer Engineering, Northeastern University, Boston, MA. His research focuses on high-speed, low-power VLSI circuit design and methodology.

F. J. Meyer (M'86) received the B.Sc. degree in computer systems engineering the Ph.D. degree from the Electrical and Computer Engineering Department, University of Massachusetts, Amherst, in 1984 and 1991, respectively. His dissertation was on fault-tolerant distributed algorithms and distributed system testing.

He is currently an Assistant Professor of Electrical and Computer Engineering, Northeastern University, Boston, MA. He was previously a Research Associate, Assistant Research Scientist, and Senior Lecturer of computer science at Texas A&M University, College Station. His research interests include yield modeling and assessment, nanocomputing, and digital design and test.

Dr. Meyer served as Program Co-Chair for the 2002 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT) and General Co-Chair for DFT 2003. He is currently an Associate Editor of the IEEE TRANSACTIONS ON COMPUTERS.

F. Lombardi (SM'02) received the B.Sc. degree (Hons.) in electronic engineering from the University of Essex, Essex, U.K., in 1977, the M.S. degree in microwaves and modern optics from the Microwave Research Unit, University College London, London, U.K., in 1978, as well as the Diploma in microwave engineering in 1978, and the Ph.D. degree from the University of London in 1982.

He is currently the Chairperson of the Department of Electrical and Computer Engineering and holder of the International Test Conference (ITC) Endowed Professorship at Northeastern University, Boston, MA. He was a faculty member at Texas Technical University, Lubbock, the University of Colorado, Boulder, and Texas A&M University, College Station. He received the Visiting Fellowship at the British Columbia Advanced System Institute, University of Victoria, Victoria, BC, Canada, in 1988, the TEES Research Fellowship from 1991 to 1992 and again from 1997 to 1998, and the Halliburton Professorship in 1995. He has been involved in organizing many international symposia, conferences, and workshops sponsored by organizations such as NATO and the IEEE, as well as Guest Editor in archival journals and magazines. His research interests are fault tolerant computing, testing and design of digital systems, configurable computing, defect tolerance, and CAD VLSI. He has extensively published in these areas and has edited six books.

S. Max (SM'85) was born in Baltimore, MD, in 1935. He received the B.E.E. degree from the College of the City of New York in 1957, and the M.S. and E.E. degrees from the Massachusetts Institute of Technology, Cambridge, in 1959 and 1961, respectively.

At Adage, Inc., he received a patent on an ADC design, and at Analogic, he was a Chief Engineer and received a patent on a differential amplifer design. In 1976, he and six others left Teradyne to form LTX Corporation, Westwood, MA. He is currently a Staff Scientist and LTX Fellow. He has published many papers in ITC and IMTC journals.

Dr. Max is a member of Tau beta Pi, Eta Kappa Nu, and Sigma Xi., and he is active in the IEEE TC-10 Standards Committee.