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# ASLIC: a low power CMOS analog circuit design automation

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## Abstract

This paper proposes an efficient automation platform that provides fast and reliable path to analog circuit design for desired specifications. Circuit heuristics and hierarchy are employed to aid efficient design flow. As a synthesis method, procedural planning of design equations is developed to improve accuracy. To cope with the low power requirements of recent analog design trend, automation flow of subthreshold analog circuit is developed based on weak inversion model. The proposed and developed tool is applied to several test cases. The results show that design time is reduced from weeks to seconds, and at the same time, a significantly accurate circuit behavior for the desired performance specification is obtained.

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## 1. Introduction

Analog design automation is one of the most important issues in the development of modern electronics history. For last few decades, we have experienced digital revolution. Analog functions have been replaced with digital equivalents at a rapid rate. With this onrushing trend, it seemed that everything could be conquered in all-digital world. However, there is a fundamental limit to this migration due to analog nature of the real world. Analog is a must-have technology to interface the external environment with digital signal processing. Moreover, analog circuits are

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1 recently regaining attention by researchers as a mainstream of circuit systems. For instance,  
2 analog signal processors outperform digital counterparts in applications where area, power, and  
3 high frequency operation are the major concerns. Nowadays, it is popular to integrate analog and  
4 digital circuitry together using System-on-Chip (SoC) concept. One of the main issues in designing  
5 mixed analog–digital systems is to minimize design cycle time for maximizing profit. To manage  
6 design complexity and time-to-market, extensive reuse in design knowledge is inevitable.

7 While digital synthesis tools have evolved in phase with digital revolution, analog portion of  
8 design automation has not been able to keep up with its demand. Despite that much efforts have  
9 been attempted in this area [1–19], there is not yet a satisfactory and practical tool that is generally  
10 accepted in the analog designer’s community. They failed to make research-to-industry transition  
11 due to inherent complexity in analog design process and difficulty to validate accuracy in  
12 production environment. The absence of analog automation tool comparable to digital  
13 counterpart constitutes a serious bottleneck in design cycle of mixed systems.

14 Historically, researchers developed two mainstreams of analog automation methodologies. One  
15 of the early approaches use optimization-based method [11–18], which optimizes a set of  
16 performance constraints characterized by complicated trade-offs and makes extensive use of  
17 detailed circuit simulator embedded in the inner loop of optimization engine. This mechanism  
18 works quite well for tuning purpose of the circuit that is already close to a good design. These  
19 techniques require many iterations to adjust transistor sizes, and the optimization engine needs to  
20 evaluate corresponding performance at each iteration cycle. This procedure is very time  
21 consuming and computationally expensive task. Second approach is equation-based method  
22 [2–10], which is based on inverse process of circuit analysis technique. Since sizing of a circuit is  
23 done mathematically, the automation process is much faster while accuracy is not as good as the  
24 first approach due to the simplified device equations and approximations.

25 The proposed automation tool ASLIC (Analog Synthesis for Low-power Integrated Circuit) is  
26 based on design equations and circuit heuristics. Therefore, fast design turn around time can be  
27 achieved. To improve the accuracy, procedural planning of design equations is proposed. Three  
28 types of operational amplifier synthesis examples are introduced for two stage op amp, buffered  
29 op amp, and subthreshold op amp. One of the major contributions of the proposed tool is  
30 subthreshold op amp design automation for low power. A good weak inversion model is  
31 employed and an effective design strategy is developed. Simulation results demonstrate that  
32 equation-based design procedure is very effective method for subthreshold analog circuits as well.  
33

## 35 2. Proposed synthesis frame work

37 The proposed frame work offers an efficient analog automation environment that outperforms  
38 the manual design flow. The synthesis procedure is entirely based on design equations and circuit  
39 heuristics, separating circuit simulation from the automation flow. Therefore, much faster design  
40 turnaround time is achieved compared to other tools embedding simulator in the design loop. One  
41 of the major penalty in equation-based approach is low accuracy resulting from the simplified  
42 models and approximations. In an effort to improve the accuracy of the predicted performance, a  
43 procedural design plan is developed to minimize unnecessary assumptions. Hierarchy is employed  
44 in order to effectively manage the design flow and reasonable size of libraries. The goal of this

1 frame work design is to support analog circuit synthesis. Currently CMOS operational amplifiers  
 2 are implemented into the tool. This platform provides effective management on equation-based  
 3 design mechanism and can be easily expanded for further development to implement other analog  
 4 functions. The frame work of this analog design automation environment is illustrated in Fig. 1.  
 5 Input interface accepts performance specifications and process technology file from the user.  
 6 Process dependent parameters are extracted from the specified technology file and used during the  
 7 synthesis procedure. This is one of the most important features in the automation tool that allows  
 8 process independent design, enabling easy process migration to future technology. Proposed  
 9 platform is composed of several modules. Circuit generator is the main automation engine, which  
 10 translates input specifications into sized circuit schematic. Library modules and parameter matrix  
 11 support the analog design process. The role of each component modules will be described in detail  
 12 in the following subsections. For output interface, a directory is created to store HSPICE netlist  
 13 of the sized circuit, test jigs, and user information sheet. User information sheet shows input  
 14 specifications and provides the computed design parameters for each transistors. The proposed  
 15 method provides frame work that can be applied to analog circuit automation. In this paper, op  
 16 amp design automation is demonstrated as a particular example. The proposed method  
 17 extensively uses heuristics and as a result, a very good first cut design is obtained without  
 18 optimization process, while recent approach using geometric programming [17] employs  
 19 optimization approach. Ref. [17] is based on fixed topology system that implements op amp  
 20 using only strong inversion model and their power consumption is in the order of milli Watt. On  
 21 the other hand, the proposed ASLIC uses hierarchy and topology selection process, which

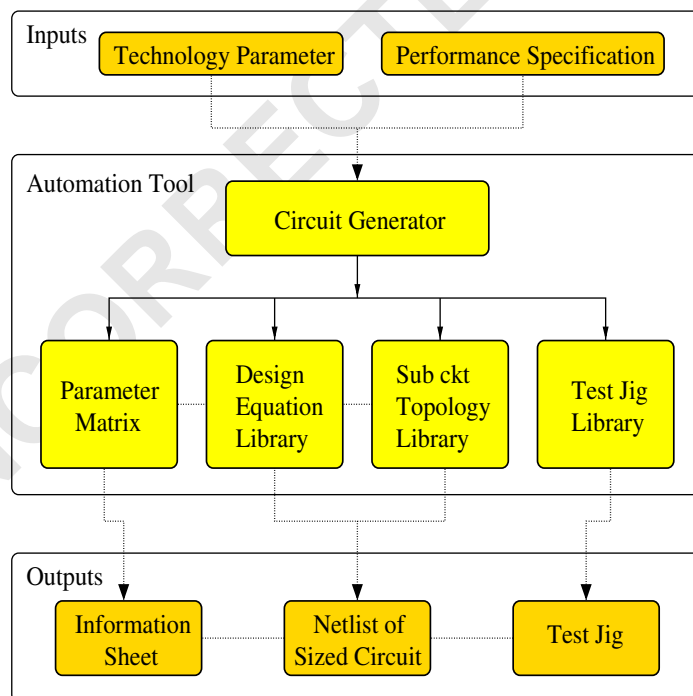


Fig. 1. Analog design environment.

provides a lot more flexibility and freedom for design range. Using ASLIC's weak inversion model, the power consumption in the order of micro Watt is achieved with smaller transistor sizes.

### 2.1. Circuit generator

Circuit generator shown in Fig. 2 is the main automation engine, which takes responsibility of translating input specifications into sized circuit schematic. This translation procedure is based on heuristics that generate appropriate circuit topology in the form of combination of sub-circuits and invoke corresponding design equations following the predefined procedural steps. If the automation tool is activated, the circuit generator asks the user process technology and performance specifications. This is implemented as the first step in the design flow. User specified information is extracted and stored into parameter matrix. Depending on this specifications, topology selection module determines the circuit topology heuristically by collecting proper sub-circuits from the library and combining them to build appropriate circuit architecture. Fig. 3 shows op amp architecture composed of various functional sub-blocks. For general purpose op amp, basic 2-stage op amp can be used without buffer stage and associated bias circuitry. Buffer stage should be included when the load capacitance is large and/or load resistance is small. If low power supply and micro-power consumption is required, subthreshold circuit design is given as an option. When this option is chosen, the topology selection module chooses 2-stage op amp architecture and subthreshold technique is used by design sequence module. Design sequence module then invokes design equations corresponding to each sub-circuits in the predefined order. After all the design parameters are calculated, netlist generation module writes HSPICE netlist of the selected topology by inserting calculated parameters. Proposed automation environment also provides test jigs for simulation and evaluation purposes. Test jig generation module connects a set of test jigs from the library with the designed circuit and test conditions such as power supply and swing ranges.

### 2.2. Hierarchy

Hierarchy [4,6] is employed for efficient management of the sub-circuit topology library and design equation library modules. In fixed-topology systems [17], each circuit has to be stored as a separate template even though sub-systems share the same topology and design knowledge. This is a waste in memory to store redundant topologies and it constitutes overhead in efforts to codify the associated design equations repeatedly. With a hierarchical organization, it is possible to cover

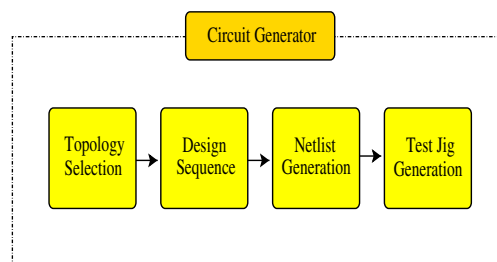


Fig. 2. Circuit generator.

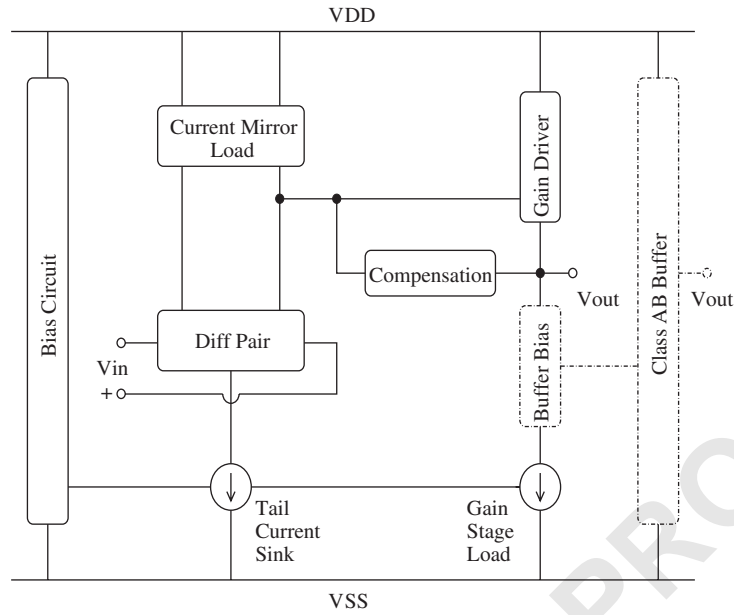


Fig. 3. Operational amplifier architecture.

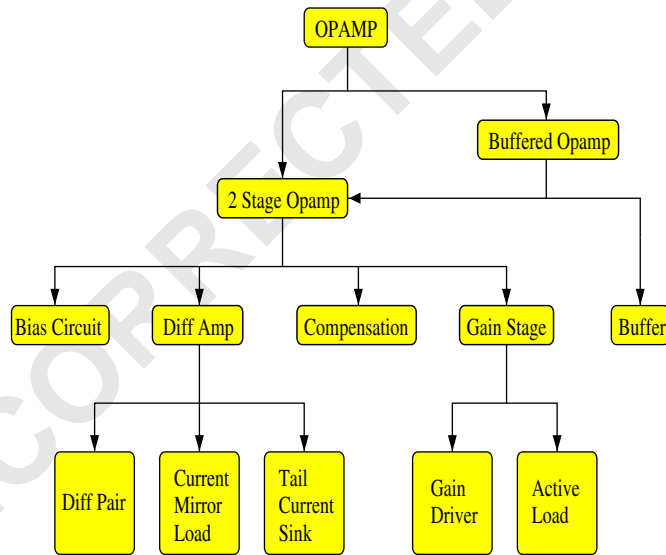


Fig. 4. Hierarchy of OP AMP design.

a wider range of design specifications using a smaller number of circuit architectures since one sub-circuit may be used in many different circuit systems. Therefore, high level of reuse and compact size of library is feasible using the hierarchy concept. The implemented hierarchical

1 structure for CMOS op amp is illustrated in Fig. 4. A circuit can be partitioned into smaller  
 2 blocks repeatedly until this process reaches the primitive circuit block which is defined as the  
 3 smallest combination of transistors that performs a unique function. For example, differential  
 4 pair and current mirror load are such primitive functional blocks. Those smallest sub-circuit  
 5 topologies are stored in the sub-circuit topology library in a hierarchical manner. Design  
 6 equations corresponding to each sub-circuit are also implemented hierarchically in the design  
 7 equation library. An example of differential amplifier organization with the libraries are shown in  
 8 Fig. 5.

### 2.3. Parameter matrix

9  
 10  
 11 Equation based tools employing hierarchy such as OASYS [4] and ISAID [6] use decomposition  
 12 method. They decompose user-given specifications at the top of the hierarchy into specifications  
 13 for each primitive circuit block prior to starting synthesis procedure. This decomposition allows  
 14 that the necessary information is assigned to the low level blocks independently of other circuit  
 15 blocks. After synthesis procedure, designed sub-circuits are combined with appropriate  
 16 connections to build a complete circuit. However, this decomposition method imposes a high  
 17 possibility of increasing error. High level specifications are not sufficient enough to be  
 18 transformed to lower level circuit blocks. Due to strong coupling present among analog sub-  
 19 circuits, it is difficult to estimate specifications for lower level blocks and to provide all the  
 20 conditions required to calculate design parameters. Frequently, the calculated values from one  
 21 sub-circuit are needed to correctly compute variables for other sub-blocks. With an incomplete  
 22 knowledge, it is inevitable to make assumptions or estimations for unknown variables to  
 23 decompose specifications and assign them to every sub-blocks. This causes high error rate when  
 24 sub-circuits are combined together, and many iterations might be needed to comply with the  
 25 overall performance expectation. Therefore, an interactive module called parameter matrix is

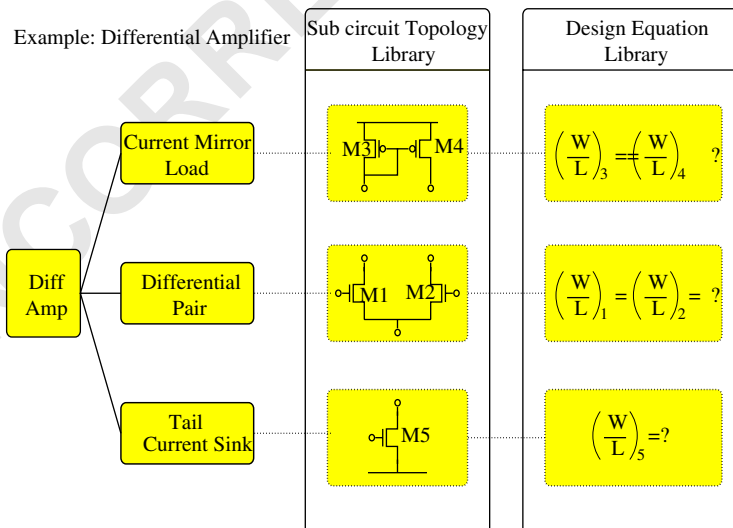


Fig. 5. Library structure.

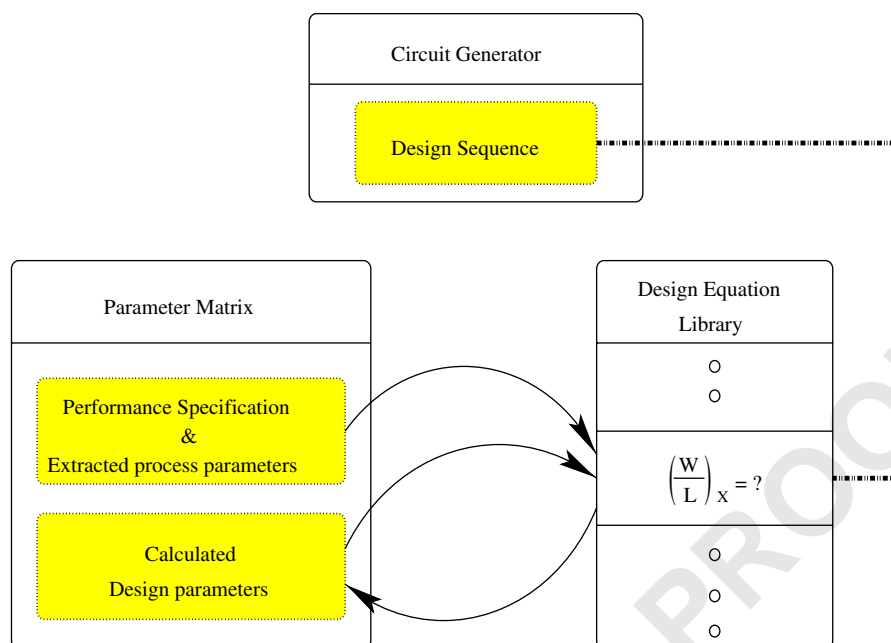


Fig. 6. Parameter matrix.

proposed instead of using specification decomposing technique. Parameter matrix contains two sections as shown in Fig. 6. The first storage element contains user-given information. Performance specifications and process parameters required for design equations are extracted and stored in this module at the beginning of automation cycle and set to read-only during the synthesis procedure. The second element is appendable memory that can be read and written into interactively during the design process. Orderly invoked design equations by the circuit generator can access both storage elements and refer to necessary information for that stage of computation. The design sequence module in the circuit generator is coded with procedural plans based on knowledge that makes decision on overall course of actions to take. Those plans attack the design task with right sub-problems step by step so that the information required for later stages can be provided from the earlier design steps. Good design process minimizes error caused by making assumptions for the variables not yet designed. Each computation stage selectively collects required information from parameter matrix. After each step, calculated variables are written into appendable memory element, and referred by following design stages.

#### 2.4. Test jigs

A set of test jigs [20] are provided to confirm various performances of designed op amps. Numerical simulator contains more elaborate models of device behavior, which does not rely on high level approximate model. Raw templates of test jig configurations are stored in the test jig library. The circuit generator adds test conditions based on specifications to those templates and writes produced test benches into the output directory created. Examples of test jigs implemented in the proposed automation tool are shown in Fig. 7.

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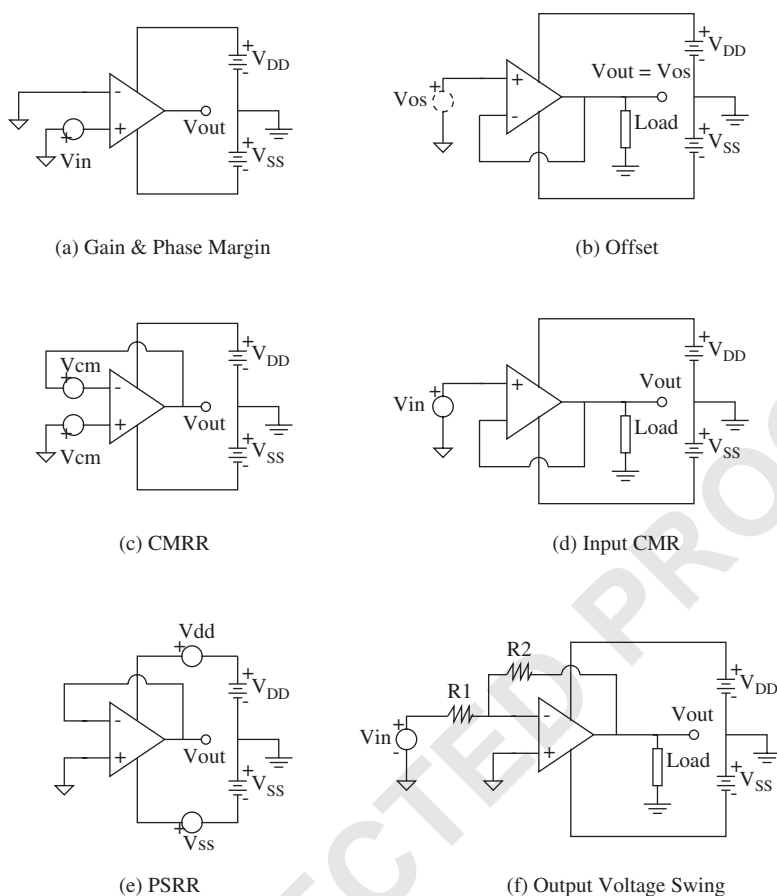


Fig. 7. Test jigs.

For most of test configurations, direct performance measurement is possible from the simulation results. However, some of them require post processing capability of simulator such as plotting the reciprocal of the simulated transfer function.

### 3. Operational amplifier synthesis

Synthesis method takes advantage of well studied analysis technique. Design equations can be transformed from analytic relationships between design parameters and the performance specifications. Even though many of design equations are inverse form of analytic equations, simply storing those basic relationships does not solve the problem completely. Real design problems are often so underconstrained that many heuristic choices must be made to generate a circuit design satisfying the desired performance specification. Those heuristic choices are making right assumptions to simplify design process and ordering design equations to minimize possible performance conflicts and to reduce unnecessary iterations.

Design equations are related with each sub-circuit topology, but variations may exist depending on the particular requirement of application. For instance, strong inversion model equations are used for general purpose op amps. However, if low power is a requirement, weak inversion model is employed and a separate set of design equations for the same sub-circuits are needed. Decision making on which model to use is provided as an option for the user. Multistage op amp is synthesized to demonstrate the efficiency of the proposed design flow in this section.

### 3.1. 2 Stage op amp synthesis procedure

The 2 stage operational amplifier implemented in the proposed tool is shown in Fig. 8. Synthesis procedure for 2 stage op amp is partly referenced from [21] with some modifications. Even though the design procedure introduced in [21] is excellent, blindly following those steps results in serious degradation of performance due to loose boundary conditions. Heuristic choices are made based on design experience to overcome those problems, especially for designing parameters of  $M_3$ ,  $M_4$  and  $M_5$ . A method to bias  $M_5$  and  $M_7$  are developed and reasoning of such design choices are explained in detail. In addition, the procedure is expanded for the design of  $R_z$  and bias circuitry. Design equations are based on strong inversion model because all the transistors operate in the saturation region.

*Step 1:* The synthesis procedure starts from choosing a device length to be used throughout the circuit design. Using a fixed value of device length for all transistors will keep  $\lambda$  constant, minimizing the effect of channel length modulation and reducing the effect of component mismatch.

*Step 2:* The value of compensation capacitor  $C_c$  should be selected such that phase margin of  $\Phi_M \geq 60^\circ$  is guaranteed. Placing the output pole  $P_2$  to be 2.2 times higher than the  $GB$  (gain bandwidth) permits a  $60^\circ$  phase margin, assuming that RHP (right half plane) zero  $Z$  is placed beyond ten times  $GB$ . This can be proved as following:

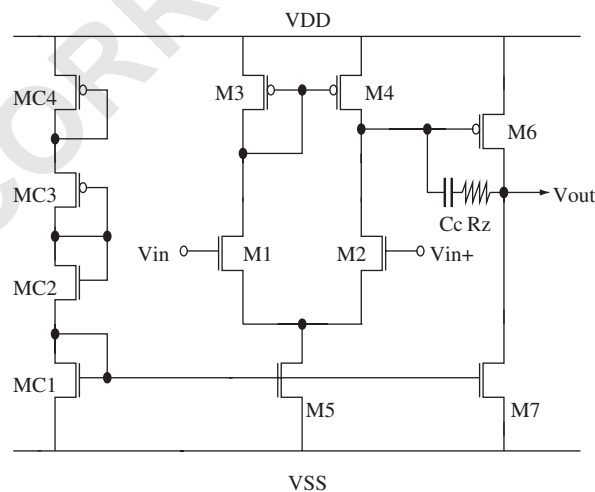


Fig. 8. 2 Stage operational amplifier with bias circuit.

$$\begin{aligned}
\Phi_M &= \pm 180^\circ - \text{Arg}[A(jw)F(jw)], \\
&= \pm 180^\circ - \tan^{-1}\left(\frac{w}{|P_1|}\right) - \tan^{-1}\left(\frac{w}{|P_2|}\right) - \tan^{-1}\left(\frac{w}{Z}\right) \\
&= 60^\circ.
\end{aligned} \tag{1}$$

Assuming unity gain frequency is  $GB$ , replace  $w$  by  $GB$ ,

$$\begin{aligned}
120^\circ &= \tan^{-1}\left(\frac{GB}{|P_1|}\right) + \tan^{-1}\left(\frac{GB}{|P_2|}\right) + \tan^{-1}\left(\frac{GB}{Z}\right), \\
&= \tan^{-1}(A_{v0}) + \tan^{-1}\left(\frac{GB}{|P_2|}\right) + \tan^{-1}\left(\frac{1}{10}\right).
\end{aligned} \tag{2}$$

Assuming  $A_{v0}$  is large,  $\tan^{-1}\left(\frac{GB}{|P_2|}\right) \approx 24.3^\circ$ , Eq. (2) becomes (3).

$$|P_2| \geq 2.2GB \text{ assuming } Z > 10GB. \tag{3}$$

Using above heuristics, the minimum value for the compensation capacitor  $C_c$  can be established.

$$C_c > 0.22C_L \tag{4}$$

*Step 3:* The tail current  $I_5$  can be determined based on slew rate or settling time requirements.

$$I_5 = SR \times C_c \text{ or } I_5 \simeq 10 \left( \frac{V_{DD} + |V_{SS}|}{2T_s} \right). \tag{5}$$

Then, DC current though  $M_1, M_2, M_3$ , and  $M_4$  are half of the tail current.

$$I_1 = I_2 = I_3 = I_4 = \frac{I_5}{2}. \tag{6}$$

*Step 4:* Next,  $M_3$  and  $M_4$  can be designed from the requirement of positive ICMR (input common mode range).  $|V_{GS3}| = V_{DD} - V_{in(max)} + V_{thn}$  can be used to determine aspect ratio of  $M_3$  and  $M_4$ . Due to the nature of the current mirror,  $S_3 = S_4$ .

$$S_3 = \left(\frac{W}{L}\right)_3 = \frac{2I_3}{k'_p(|V_{GS3}| - |V_{thp}|)^2}. \tag{7}$$

*Step 5:* If the value determined for  $S_3$  is less than one, there is a high possibility that the designed width is less than the minimum size allowable for the given technology, considering that device length is chosen close to the minimum length. Increasing both  $W$  and  $L$  could be a solution, however, this increases gate capacitance, which contributes to the mirror pole that may cause a degradation in phase margin.

Therefore  $S_3$  should be greater than 1. The upper limit for  $S_3$  can be defined such that the pole and zero due to  $C_{gs3}$  and  $C_{gs4}$  will not be dominant assuming  $P_3$  is greater than  $10GB$ . This upper limit can be set from the following:

$$|P_3| = \frac{g_3}{C_3} \geq 10GB \text{ where, } C_3 = C_{gs3} + C_{gs4}, \tag{8}$$

$$C_{gs3} = C_{gs4} = \frac{2}{3} C_{ox} W_3 L_3 = \frac{2}{3} C_{ox} L_3^2 \left(\frac{W}{L}\right)_3. \tag{9}$$

Substituting Eq. (9) into Eq. (8), with  $g_{m3} = \sqrt{2I_3k'_p(\frac{W}{L})_3}$ , the upper limit of  $(\frac{W}{L})_3$  can be obtained. So, the range of designable aspect ratio of  $M_3$  and  $M_4$  can be defined as,

$$1 \leq \left(\frac{W}{L}\right)_3 \ll \frac{2I_3k'_p}{\left(2\frac{2}{3}C_{ox}L_3^2(10GB)\right)^2}. \quad (10)$$

In the proposed tool,  $S_3$  is set to be 5 if the calculated  $S_3$  from Step 4 is less than one, and checks if this ratio does not violate the upper limit calculated from Eq. (10) such that the effect of the mirror pole is negligible.

*Step 6:* Next step is to design  $M_1$  and  $M_2$ . Requirements for the transconductance of the input transistors can be determined from the information of  $C_c$  and  $GB$ .

$$g_{m1} = GB \times C_c = g_{m2}. \quad (11)$$

The aspect ratio of the differential pair is the same ( $S_1 = S_2$ ) and can be calculated as,

$$S_1 = \left(\frac{W}{L}\right)_1 = \frac{g_{m1}^2}{k'_n I_5}. \quad (12)$$

*Step 7:* Enough information is now available to calculate the saturation voltage of transistor  $M_5$ . Using the negative ICMR,  $V_{DS5(sat)}$  can be computed.

$$V_{DS5(sat)} = V_{in(min)} - V_{SS} - \sqrt{\frac{I_5}{k'_n(\frac{W}{L})_1}} - V_{thn} \geq 100 \text{ mV}. \quad (13)$$

If the calculated value for  $V_{DS5(sat)}$  is less than zero, then the ICMR specification may be too stringent. If the value of  $V_{DS5(sat)}$  is less than 100 mV, it may result in a rather large  $S_5$ , which may not be acceptable. To solve this problem,  $I_5$  is to be reduced, or  $S_1$  is increased. The effects of these changes must be accounted for in the previous design steps. Iteration is required until the desired result is achieved.

However, big  $V_{DS5(sat)}$  is also problematic. To keep  $M_5$  at the saturation boundary, big bias voltage is required. This value of  $V_{bias}$  is also used to bias gain stage current sink load  $M_7$  to operate in the saturation region. As a result, output swing range can be seriously degraded. To prevent this problem,  $V_{DS5(sat)}$  range is set between 100 mV and 150 mV in the proposed tool. When the calculated  $V_{DS5(sat)}$  is larger than this range, it is set to 150 mV. This choice allows more room for ICMR range, however, it does not hurt performance specification.

With the choice of  $V_{DS5(sat)}$ , aspect ratio of  $M_5$  is calculated.

$$S_5 = \left(\frac{W}{L}\right)_5 = \frac{2I_5}{k'_n(V_{DS5(sat)})^2}. \quad (14)$$

Bias voltage then can be extracted as

$$V_{bias} = \sqrt{\frac{2I_5}{k'_n(\frac{W}{L})_5}} + V_{thn} + V_{SS}. \quad (15)$$

*Step 8:* Next step is to design gain stage. For a phase margin of  $60^\circ$ , the location of the output pole  $P_2$  was assumed to be placed at 2.2 times of  $GB$ . Based on this assumption, the

1 transconductance  $g_{m6}$  can be determined:

$$3 \quad g_{m6} = 2.2g_{m1} \left( \frac{C_L}{C_c} \right). \quad (16)$$

5 To complete the design of  $M_6$ , the following considerations should be taken into account. First,  $S_6$  can be obtained from the balance equation to achieve proper mirroring of the first stage current mirror load. This requires that  $V_{SG4} = V_{SG6}$  and  $|V_{GS}| = \frac{g_m}{k'(\frac{W}{L})} + |V_{th}|$ .

$$9 \quad S_6 = \left( \frac{W}{L} \right)_6 = S_4 \frac{g_{m6}}{g_{m4}}, \quad (17)$$

$$11 \quad I_6 = \frac{gm_6^2}{2k'_p S_6}. \quad (18)$$

13 At this point maximum output voltage specification must be checked:

$$15 \quad |V_{DS6(sat)}| = \sqrt{\frac{2I_6}{k'_p \left(\frac{W}{L}\right)_6}} \leq V_{DD} - V_{out(max)}. \quad (19)$$

17 If this requirement is not satisfied, then the current must be decreased or aspect ratio must be increased to achieve a smaller  $V_{DS6(sat)}$ . To make this adjustment, the required  $V_{DS6(sat)}$  by maximum output voltage with  $g_{m6}$  obtained from Eq. (16) can be used to design  $S_6$  and  $I_6$ . If these changes are made to satisfy the maximum output voltage specification, then the proper mirroring is no longer guaranteed.

$$23 \quad V_{DS6(sat)} = V_{DD} - V_{out(max)}, \quad (20)$$

$$25 \quad S_6 = \frac{g_{m6}}{k'_p V_{DS6(sat)}}, \quad (21)$$

$$27 \quad I_6 = \frac{g_{m6}^2}{2k'_p S_6}. \quad (22)$$

29 *Step 9:* The device size of  $M_7$  can be determined from the balance equation knowing that  $I_6 = I_7$ .

$$33 \quad S_7 = \left( \frac{W}{L} \right)_7 = S_5 \left( \frac{I_7}{I_5} \right). \quad (23)$$

35 Minimum output voltage specification must be checked:

$$37 \quad V_{out(min)} \geq V_{DS7(sat)} + V_{SS} = \sqrt{\frac{2I_7}{k'_n \left(\frac{W}{L}\right)_7}} + V_{SS}. \quad (24)$$

39 *Step 10:* RHP zero results from the feed forward path through the compensation capacitor. This tends to limit the  $GB$  that might otherwise be achievable if the zero were not present. To eliminate the effect of RHP zero, a nulling resistor  $R_z$  is inserted in series with the  $C_c$ . The  $R_z$  allows independent control over the placement of the zero:

$$R_z = \frac{1}{g_{m6}}. \quad (25)$$

*Step 11:* The first cut design of 2 stage op amp is now complete. Now it is time to check if the total amplifier gain and power consumption satisfy the given specifications:

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_4)I_6(\lambda_6 + \lambda_7)}, \quad (26)$$

$$P_{\text{diss}} = (I_5 + I_6)(V_{DD} + |V_{SS}|). \quad (27)$$

If gain is too low,  $I_5$  and  $I_6$  can be decreased or  $(\frac{W}{L})_1$ ,  $(\frac{W}{L})_2$  and  $(\frac{W}{L})_6$  can be increased. If power is too high,  $I_5$  and  $I_6$  should be reduced. However, the currents may violate the slew rate requirement and lower driving capability for the given load capacitance. Reducing currents may increase the aspect ratios to satisfy the input and output swing ranges. If micro Watt level of power consumption is required, the design procedure can be switched to the subthreshold voltage design technique.

*Step 12:* Bias-circuit design is given as an option. In the tool, two choices of bias-circuit topology are provided. The first choice is shown in Fig. 8 with MOS-only configuration.

For proper mirroring,  $I_{c1} = I_{c2} = I_{c3} = I_{c4} = I_5$ .

$$S_{c1} = \frac{2I_{c1}}{k'_n(V_{GS_{c1}} - V_{\text{thn}})^2} \text{ where, } V_{GS_{c1}} = V_{\text{bias}} - V_{SS}. \quad (28)$$

Since  $(V_{DD} - V_{SS}) = V_{GS_{c1}} + V_{GS_{c2}} + |V_{GS_{c3}}| + |V_{GS_{c4}}|$ ,  $V_{GS}$  of  $M_{c2}$ ,  $M_{c3}$ ,  $M_{c4}$  are set such that  $V_{GS_{c2}} = |V_{GS_{c3}}| = |V_{GS_{c4}}| = \frac{V_{DD} - V_{SS} - V_{GS_{c1}}}{3}$ .

$$S_{c2} = \frac{2I_{c2}}{k'_n(V_{GS_{c2}} - V_{\text{thn}})^2},$$

$$S_{c3} = S_{c4} = \frac{2I_{c3}}{k'_p(|V_{GS_{c3}}| - |V_{\text{thp}}|)^2}. \quad (29)$$

If bias-circuit is included in the design, power dissipation in Eq. (27) should be modified by adding current through the bias circuit.

### 3.2. Buffered op amp synthesis procedure

Buffered op amp implemented in the automation tool is shown in Fig. 9. A buffered op amp synthesis flow is developed to design the circuit that can drive both large capacitance and small resistance loads. Common-drain class AB output buffer configuration in Fig. 9 is chosen for the automation task.

**First stage design:** First stage (differential amplifier) design procedure is similar to that of 2 stage op amp. However, the parasitic capacitance at the output node of gain stage should be taken into account for  $C_c$  calculation in Step 1. This parasitic capacitance is unknown variable until the design of second and third stage are completed. Therefore, assumption on this value should be made. In the program, this value is estimated as  $C_L$  divided by ten. From the design experience,

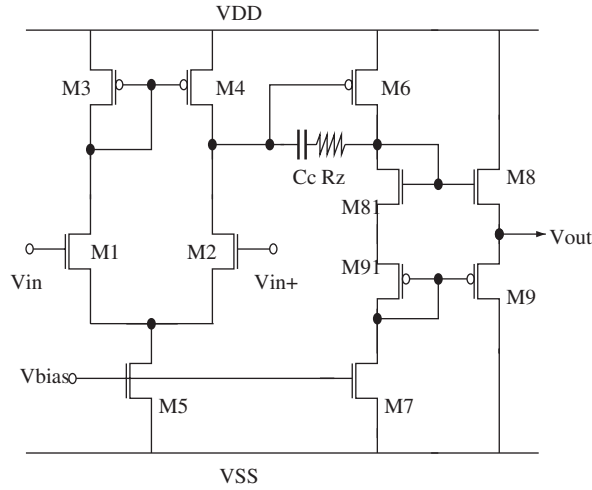


Fig. 9. Buffered OP AMP.

this assumption is acceptable for overall performance of the op amp. Design strategy from Steps 2 to 7 is identical to 2 stage op amp design.

**Second stage design:** Gain stage design of  $M_6$  and  $M_7$  is also similar. Minor modification on swing range at the output node of gain stage is needed for Steps 8 and 9. Let us define the voltage at the output node of the second stage to be  $V_o$  and the final output of the buffer stage to be  $V_{out}$ . To obtain swing range for  $V_o$ , threshold voltage drop must be considered. For  $V_{o(max)}$ , the body effect of  $M_8$  should be considered. In worst case, the source-body potential difference of  $M_8$  is  $V_{SB8} = V_{out(max)} - V_{SS}$ , and  $V_{th8}$  including body effect can be obtained. Then,  $V_{o(max)}$  can be calculated as

$$V_{o(max)} = V_{out(max)} + V_{th8}. \quad (30)$$

This value can be used for  $M_6$  design in Step 8. Parasitic capacitance estimation is still valid for this stage of computation.  $V_{o(min)}$  can be obtained similarly and this value should be used for  $M_7$  design in Step 9.

$$V_{o(min)} = V_{out(min)} - |V_{thp}| \quad (31)$$

**Buffer stage design:** The following design strategy is proposed for Class AB buffer stage. This buffer design procedure can be inserted between Steps 9 and 10 of 2 stage op amp synthesis.

*Step B1:* To implement floating batteries that provide a gate-source bias of the source follower buffer  $M_8$  and  $M_9$ ,  $M_{81}$  and  $M_{91}$  are used. Currents through  $M_{81}$  and  $M_{91}$  are provided by the constant current sink  $M_7$  such that  $I_{81} = I_{91} = I_7$ . Therefore, gate-source voltages of  $M_{81}$  and  $M_{91}$  are constant and they can operate floating batteries. Since  $M_{81}$  and  $M_{91}$  operates in the saturation region, the condition  $V_{GS81} > V_{thn}$  and  $|V_{GS91}| > |V_{thp}|$  should be satisfied. A parameter ( $\alpha > 0$ ) is introduced to determine the efficiency of the buffer. With smaller  $\alpha$ , higher efficiency can be achieved. Then, bias voltages of  $M_{81}$  and  $M_{91}$  can be defined as,

$$V_{GS81} = V_{thn} + \alpha, \quad (32)$$

$$|V_{GS91}| = |V_{thp}| + \alpha. \quad (33)$$

With above information, aspect ratio of  $M_{81}$  and  $M_{91}$  can be computed.

$$\left(\frac{W}{L}\right)_{81} = \frac{2I_{81}}{k'_n(V_{GS81} - V_{thn})^2} = \frac{2I_{81}}{k'_n\alpha^2}, \quad (34)$$

$$\left(\frac{W}{L}\right)_{91} = \frac{2I_{91}}{k'_p(|V_{GS91}| - |V_{thp}|)^2} = \frac{2I_{91}}{k'_p\alpha^2}. \quad (35)$$

*Step B2:* The maximum current that can source through  $M_8$  or sink through  $M_9$  can be obtained from the following relationship considering both capacitive and resistive load.

$$I_{out(max)} = SR \times C_L + \frac{V_{out(max)}}{R_L}. \quad (36)$$

$V_{GS8(max)}$  can be obtained when  $M_8$  is fully turned on and  $M_9$  is turned off. Similarly,  $V_{GS9(max)}$  can be obtained when  $M_9$  is fully turned on while  $M_8$  is turned off.

$$V_{GS8(max)} = V_{GS9(max)} = V_{thn} + |V_{thp}| + 2\alpha. \quad (37)$$

Eq. (37) is extracted from the fact that the bias voltage of  $M_{81}$  and  $M_{91}$  are given by Eqs. (32) and (33).

Then, aspect ratio of  $M_8$  and  $M_9$  can be computed as,

$$\left(\frac{W}{L}\right)_8 = \frac{2I_{out(max)}}{k'_n(V_{GS8(max)} - V_{thn})^2} = \frac{2I_{out(max)}}{k'_n(|V_{thp}| + 2\alpha)^2}, \quad (38)$$

$$\left(\frac{W}{L}\right)_9 = \frac{2I_{out(max)}}{k'_p(|V_{GS9(max)}| - |V_{thp}|)^2} = \frac{2I_{out(max)}}{k'_p(V_{thn} + 2\alpha)^2}. \quad (39)$$

Buffer design is now completed, and the rest of procedure from Step 10 can be followed. In Step 11, the same gain calculation can be used assuming that the source follower buffer stage gain is close to unity. In reality, the gain of source follower is less than one, however, this influence on overall gain is negligible. Power dissipation should be considered by including the current through the buffer stage. Adding bias circuit is optional, and the same strategy in Step 12 can be used.

### 3.3. Subthreshold op amp synthesis procedure

Synthesis flow of a conventional two-stage subthreshold op amp requiring micro power consumption is proposed as an example to show a low power analog circuit automation. Bulk-driven op amp could be an alternative for low power application, however, this technique is not as widely used as the one shown in Fig. 10. The tool implements the weak inversion model so that the op amp operates in subthreshold region achieving ultra low power consumption.

*Step 1:* The synthesis procedure starts from choosing a device length to be used throughout the circuit design. This will keep  $\lambda$  constant minimizing the effect of channel length modulation.

*Step 2:*  $C_c$  should be selected such that  $\Phi_M \geq 60^\circ$  is guaranteed:

$$C_c > 0.22C_L. \quad (40)$$

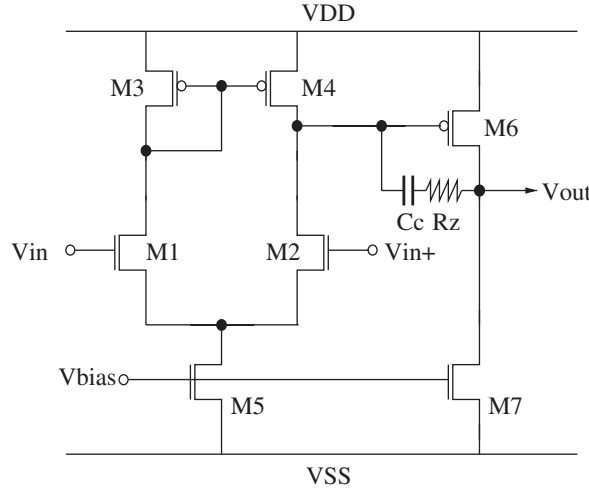


Fig. 10. Subthreshold OP AMP.

Step 3: The tail current  $I_5$  can be determined based on slew rate requirements:

$$I_5 = SR \times C_c. \quad (41)$$

Then DC current through  $M_1, M_2, M_3$ , and  $M_4$  are half of tail current.

Step 4:  $M_3$  and  $M_4$  can be designed from the positive ICMR.

$$S_3 = \left(\frac{W}{L}\right)_3 = \frac{2I_3}{k'_p(|V_{GS3}| - |V_{thp}|)^2}. \quad (42)$$

Designable aspect ratio of  $M_3$  is limited such that the effect of mirror pole is negligible.

$$1 \leq \left(\frac{W}{L}\right)_3 \ll \frac{2I_3 k'_p}{(2^{\frac{2}{3}} C_{ox} L_3^2 (10GB))^2}. \quad (43)$$

Step 5: The aspect ratio of differential pair are the same ( $S_1 = S_2$ ) and can be calculated as

$$S_1 = \left(\frac{W}{L}\right)_1 = \frac{I_1}{I_{D0} \exp\left(\frac{V_{GS1}}{\eta V_T}\right)}. \quad (44)$$

Typically,  $V_{GS} < V_{th} - 100 \text{ mV}$  when the MOSFET is operated in the subthreshold region.  $GB$  specification should be verified against the calculated values of  $g_{m1}$  and  $C_c$ :

$$g_{m1} = \frac{I_1}{\eta V_T}, \quad (45)$$

$$GB \leq \frac{g_{m1}}{C_c}. \quad (46)$$

Step 6: For a transistor to work as a constant current source in weak inversion,  $V_{DS} > 3V_T$ .

$$S_5 = \frac{I_5}{I_{D0} \exp\left(\frac{V_{GS5}}{\eta V_T}\right)}, \quad (47)$$

$$V_{in(min)} \geq V_{SS} + V_{DS5} + V_{GS1}. \quad (48)$$

Bias voltage then can be calculated as

$$V_{bias} = V_{GS5} + V_{SS}. \quad (49)$$

Step 7:  $S_6$  can be obtained from balance equation to achieve proper mirroring of the first stage current mirror load.

$$g_{m6} = 2.2g_{m1} \left(\frac{C_L}{C_c}\right), \quad (50)$$

Table 1  
The characteristics of subthreshold operational amplifier

Specifications	Value	Unit
Technology parameter	<i>tsmc_t17b_params_025.inc</i>	
$V_{DD}$	2	V
$V_{SS}$	0	V
Slew rate	7.2	V/ $\mu$ sec
Load capacitance	1	pF
Gain bandwidth	15	MHz
Gain	87	dB
Phase margin	45	degree
Gain margin	7	dB
CMRR	83	dB
Input CMR	0–1.9	V
Systematic offset	1	mV
PSRR	105	dB
Output swing	0.1–1.9	V
Power consumption	12	$\mu$ W
Device length	2	$\mu$ m

Table 2  
Subthreshold op amp size: Manual design vs. Automation

$\frac{W}{L}$	Manual design	Automation
$M_1$ & $M_2$	3	5.3661
$M_3$ & $M_4$	3	3.6742
$M_5$	7.5	18.6519
$M_6$	21	32.2228
$M_7$	24.5	81.7886

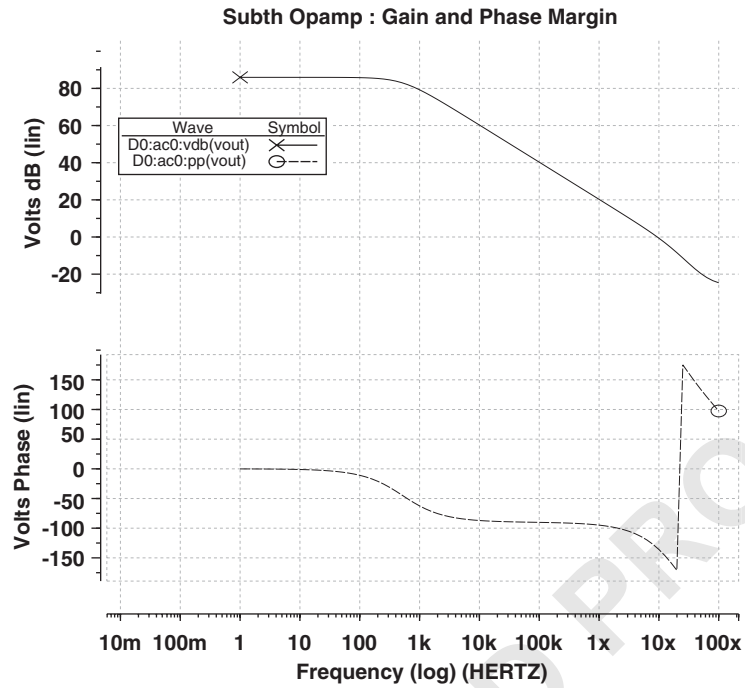


Fig. 11. Example : gain and phase margin.

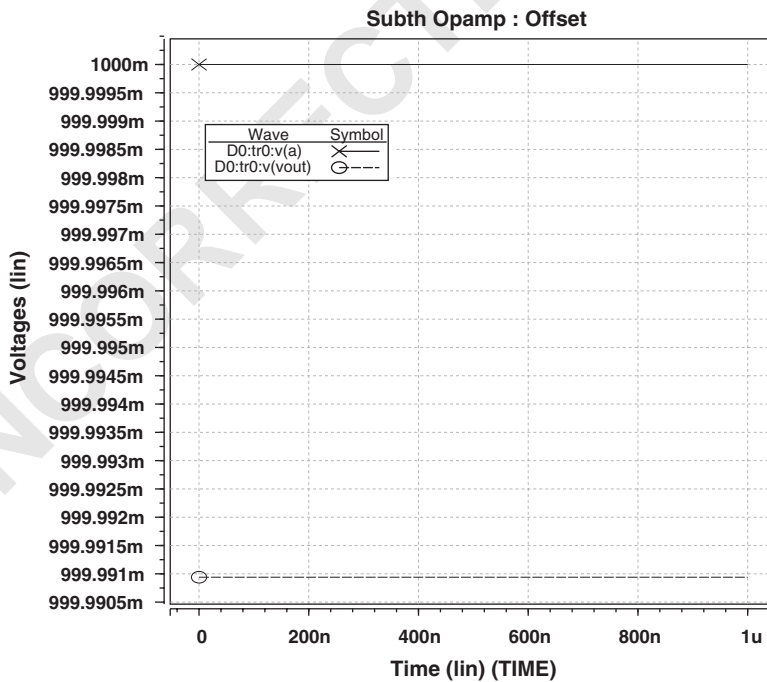


Fig. 12. Example: offset.

$$S_6 = \left(\frac{W}{L}\right)_6 = S_4 \frac{g_{m6}}{g_{m4}}, \quad (51)$$

$$I_6 = \frac{gm_6^2}{2k'_p S_6}, \quad (52)$$

$$V_{DS6(sat)} = \sqrt{\frac{2I_6}{k'_p \left(\frac{W}{L}\right)_6}} \leq V_{DD} - V_{out(max)}. \quad (53)$$

Step 8:  $M_7$  can be determined from the balance equation:

$$S_7 = \left(\frac{W}{L}\right)_7 = S_5 \left(\frac{I_7}{I_5}\right), \quad (54)$$

$$V_{out(min)} \geq V_{DS7} + V_{SS}. \quad (55)$$

Step 9:  $R_z$  eliminates the effect of RHP zero:

$$R_z = \frac{1}{g_{m6}}. \quad (56)$$

Step 10: Check the gain and power consumption.

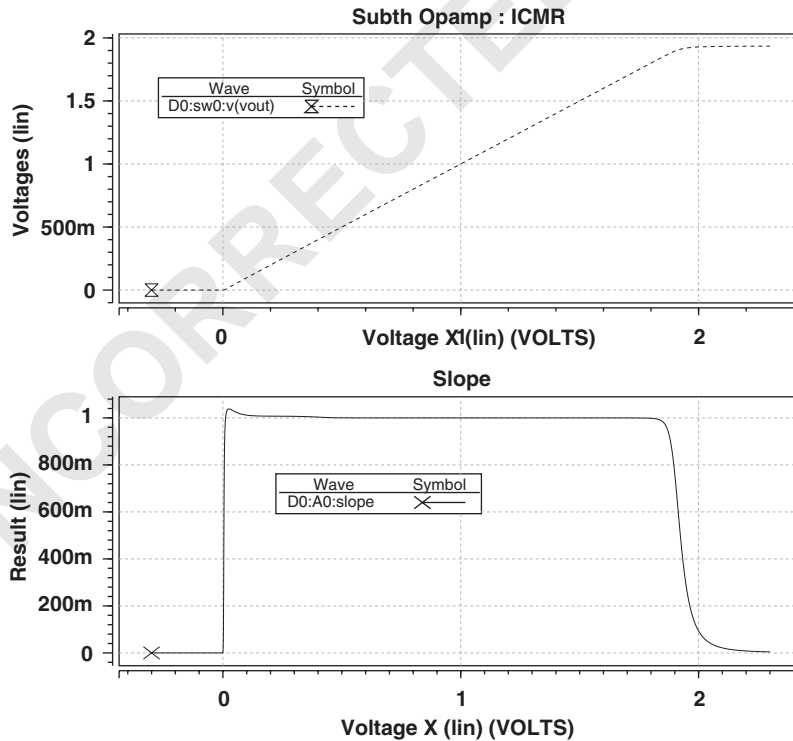


Fig. 13. Example: input common mode range.

$$A_{v0} = g_{m2}g_{m6}(r_{o2}||r_{o4})(r_{o6}||r_{o7}), \quad (57)$$

$$P_{\text{diss}} = (I_5 + I_6)(V_{\text{DD}} + |V_{\text{SS}}|). \quad (58)$$

#### 4. Application and performance comparison

As an application of the proposed tool, the automated subthreshold op amp is used in neuron circuit [22] and compared to the manual design case.

The simulated characteristics of manually designed subthreshold op amp are summarized in Table 1 and these performances are given as specifications for the automation task. Table 2 compares the transistor sizing of automated to that of manual subthreshold op amp design. Even though automated op amp takes larger area, design time can be significantly reduced. For example, the manual design of the subthreshold op amp may take a few weeks depending on designer's experience, while it takes less than 10 s using the proposed automation tool. Using the provided test jigs, performance of the automated circuit is verified. As shown in Figs. 11–17, performance of the automated subthreshold op amp is comparable to the manual design case. For instance, measured DC gain is 86 dB and phase margin measured when gain is 0 dB is  $46^\circ$  from Fig. 11. Offset can be obtained by subtracting  $V_{\text{out}}$  from  $V_{\text{in}}$  in Fig. 12. ICMR and output swing

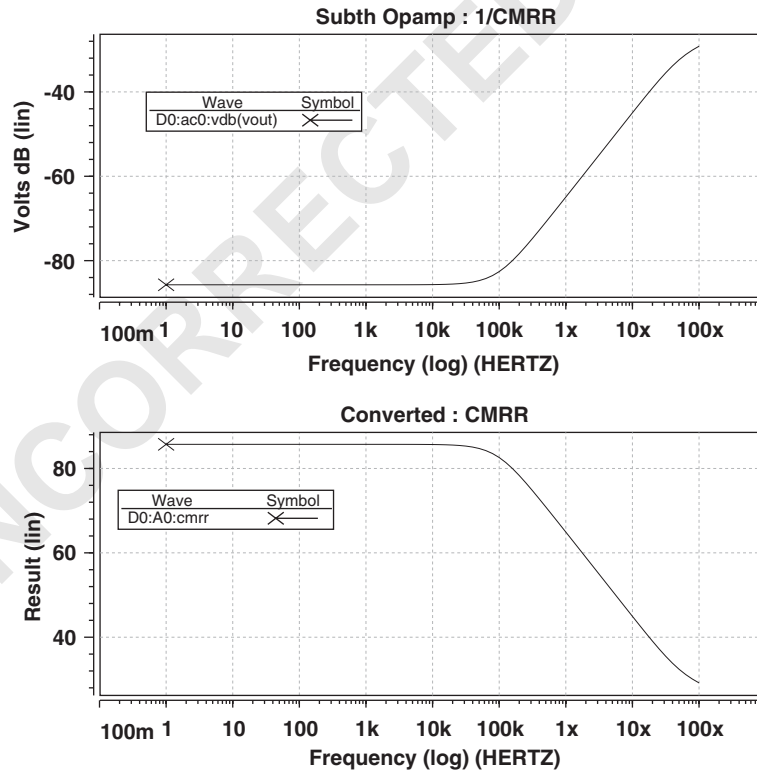


Fig. 14. Example: common mode rejection ratio.

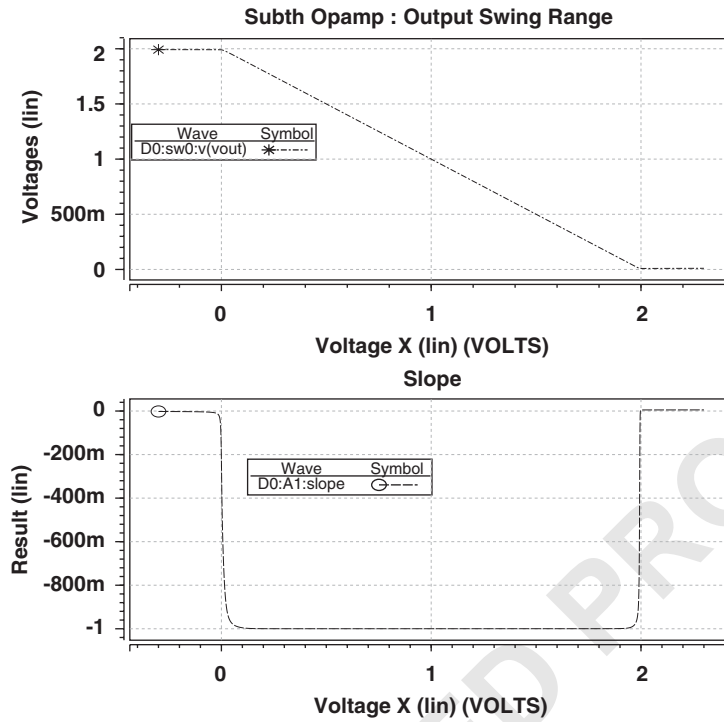


Fig. 15. Example: output swing range.

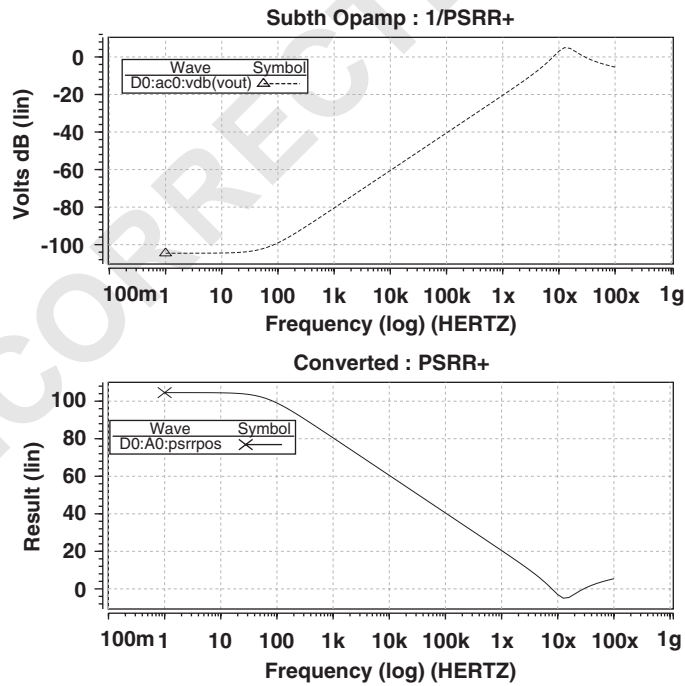


Fig. 16. Example: positive power supply rejection ratio.

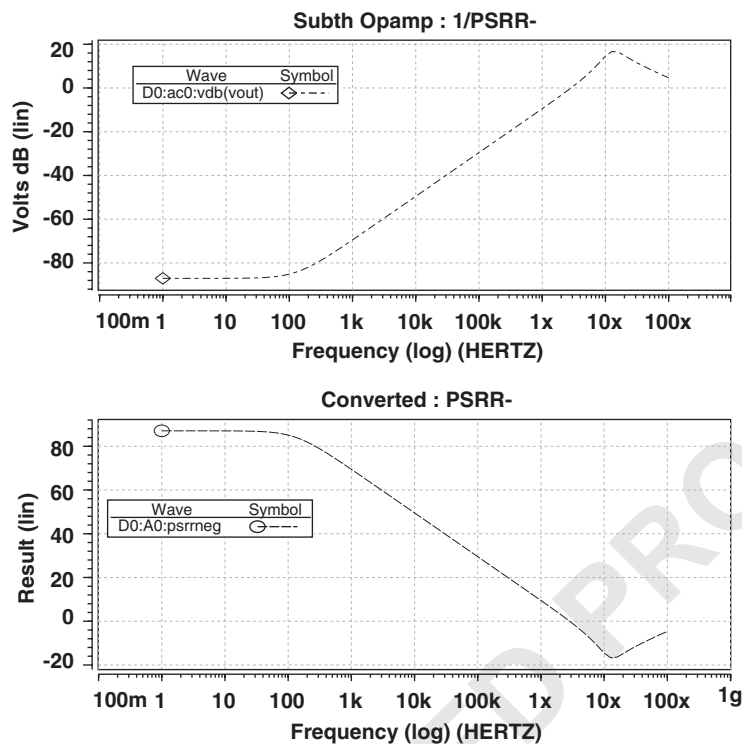


Fig. 17. Example: negative power supply rejection ratio.

ranges are measured from Figs. 13 and 15. Slope is plotted by taking derivative of the simulated transfer curve, where unity slope corresponds to ICMR and output swing ranges. CMRR (Common Mode Rejection Ratio) in Fig. 14, Positive PSRR (Power Supply Rejection Ratio) in Fig. 16, and Negative PSRR in Fig. 17 require post processing option of the simulator. Direct simulation results of those performance are shown in the upper graph, and their reciprocal is plotted in the lower graph.

Automated subthreshold op amp is used in a neuron circuit. Neuron model and its design mechanism are described in detail in [22]. Output waveforms of neuron circuit mimics the chaotic bursting behavior of the biological neuron. Fig. 18 shows the output of neuron circuit using manually designed op amp, and compared to the one of the synthesized neuron circuit. This application example shows that the proposed automation tool can effectively replace the complicated manual design flow without critical drawbacks.

It is difficult to compare the performance of various analog automation tools in a qualitative manner because they set different objectives for the level of automation and employ diverse approaches to achieve their goals. Synthesis time and rough error of various tools estimated by [23] are shown in Table 3. Even though this estimation may not be a fair comparison, it gives an overall idea where the proposed tool stands.

Since the proposed tool sets acceptable boundary for the performance rather than optimizing to an exact value, obtaining the better performance than given specification is not considered as an

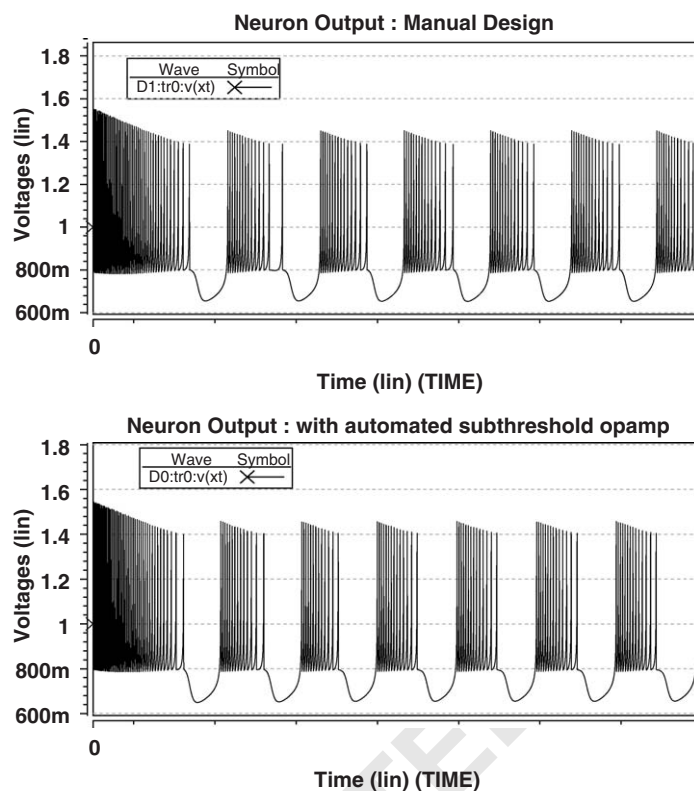


Fig. 18. Application: neuron circuit outputs.

Table 3

The error rate and synthesis time of various analog automation tools

Tool	Synthesis method	Error	Synthesis time
IDAC	Equation-based	15%	Few seconds
OASYS	Equation-based	25%	Few seconds
ISAID	Equation-based	14%	Not reported
	+ post optimization		
STAIC	Equation-based	24%	3 min
DELIGHT.SPICE	Optimization-based (circuit Simulator)	0%	18 h
MEALSTROM	Optimization-based (circuit Simulator)	0%	3.6 h
ASTRX/OBLX	Optimization-based (AWE + equations)	30%	11.8 h
OPASYN	Optimization-based (equations)	200%	1 min
ASLIC (proposed)	Equation-based	15–20%	Few seconds

1 error. Error is estimated based on average deviation of the calculated design parameters from the  
 2 simulation results. Estimation error of the proposed tool is about 15% for two-stage and buffered  
 3 op amps and 20% for subthreshold op amp. Synthesis takes only a few seconds of CPU time.

4 Since systems based on optimization technique usually aim at obtaining an exact performance  
 5 for give specification, achieving 0% error rate is possible. However, those systems require good  
 6 initial condition in many cases and optimization algorithm takes significant amount of time to  
 7 synthesize the circuit. On the other hand, equation based tools are much faster, although they do  
 8 not provide the exactly optimized performance due to simplified device model used during the  
 9 synthesis procedure.

## 11 5. Conclusion

12 The proposed automation platform provides fast and reliable path to analog circuit design for  
 13 the desired specifications. Effectiveness of the proposed tool is verified through simulation of the  
 14 provided test jigs. Using this approach, analog design time is reduced to few seconds, and a  
 15 sufficiently accurate circuit behavior for the desired performance can be obtained. The proposed  
 16 automation tool is applied to the neuron circuit design successfully.  
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