

Soft-Error Hardening Designs of Nanoscale CMOS Latches

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Abstract— As technology scales down in the deep sub-micron/nano ranges, CMOS circuits are more sensitive to externally induced phenomena to likely cause the occurrence of so-called soft errors. Therefore, the operation of these circuits to tolerate soft errors is a strict requirement in today's designs. Traditional error tolerant methods result in significant cost penalties in terms of power, area and performance, and the development of low-cost hardening designs for storage cells (such as latches and memories) is of increasing importance. This paper proposes new hardening designs for CMOS latches at 32nm feature size. Three hardening latch circuits are proposed; two of these circuits are Schmitt trigger based, while the third one utilizes a cascode configuration in the feedback loop. These new hardening latches are shown to have superior performance in terms of power-delay product as well as highest tolerance to soft errors (measured by the critical charge) than existing hardening latches. Extensive simulation results are provided using the predictive technology file for 32nm feature size in CMOS.

Index Terms: Hardening, Soft Error, Nano CMOS

I. INTRODUCTION

As nanotechnology is fast moving from explorative to industrial practice, the operation of nanoscale circuits has been extensively analyzed. However, the extremely high density of nanoscale circuits has resulted in the deterioration of many performance metrics, such as power and delay. Leakage current has substantially increased, gain has decreased, and sensitivity to process variation in manufacturing is considered to be almost unavoidable as the feature size is expected to reach 32 nm in the next few years. Moreover, the tremendous scaling of CMOS technology necessitates reliable operation in many circuit designs. Due to the lower V_{dd} and the smaller node capacitance, the amount of charge stored on a circuit node is becoming increasingly smaller, thus making circuits more susceptible to spurious voltage variations caused by externally induced phenomena such as cosmic ray neutrons and α -particles [1]. These energy particles travel through the silicon bulk and create minority carriers that may be collected by the source/drain diffusion, thus altering the voltage value of the nodes [2]. This is particularly deleterious for storage cells such as memories and latches because data integrity is affected. The occurrence of this type of event may result in transient faults (TFs) as widely reported in the technical literature. If a TF is latched by a sampling element (latch), then this may result in a so-called soft error (SE) [3]. The soft error

rate (SER) is defined as the rate at which a device (circuit or system) encounters on a predictive basis SEs. SER occurrence is expected to be significantly higher for deep submicron/nano CMOS [4].

Traditionally, soft errors have been a concern in high density logic circuits as they may seriously affect the overall operation of VLSI chips. Memories can be protected against TFs at a relatively low cost by using error detecting/correcting codes [5]. Coding based on parity or Hamming codes can offer full protection when a particle strike results in single errors at any memory word. Many error tolerant methods for soft errors occurring in latches of logic circuits have been proposed. However as geometries size decreases, a single particle may result in multiple errors. The cost in terms of area, speed, and power for protecting memories and latches from a TF causing multiple errors can be significant. Therefore, data integrity against TFs is of the utmost importance for general-purpose applications. For SEs due to TFs affecting a sampling element, hardening has been proposed for low-cost robust design of latches [6] - [10].

Hardening design approaches can be classified into two categories [10]. In the first approach, circuits are designed to be insensitive to TFs independently of both the size of the cell transistors and the capacitance of the cell nodes. In the second category, hardening is achieved in the design by increasing the capacitance of some nodes or the strength of their transistors. An example of first type of cell has been reported in [6] and is commonly known as DICE. The DICE cell uses twice the number of transistors of the standard storage cell to achieve immunity against TFs affecting any single node without requiring an increase in the size of some transistors, or the capacitance of some nodes. In a DICE cell, the node affected by TFs can be driven back to its previous state by other transistors. For the second category of hardening designs, approaches using Schmitt triggers and/or innovative feedback arrangements are utilized to protect storage cells from TFs [9] [11].

The objective of this paper is to propose new designs for hardening latch circuits in CMOS at the nano range of 32nm. These designs offer novel features compared with the ones found in the technical literature. Tolerance to soft errors is achieved due to a higher critical charge that is also complemented by higher performance metrics such as an improved power-delay product. Extensive simulation results are provided to assess and compare the effectiveness of the new designs with existing approaches. It is shown that the proposed circuits for latches are superior at the reduced feature size of 32 nm (using its

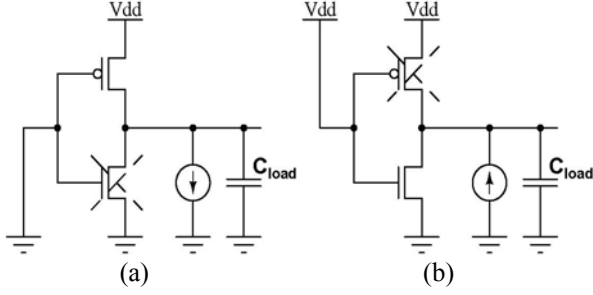


Figure 1. Equivalent circuits [14] used for simulation of (a) negative and (b) positive glitches

predictive technology file) in terms of power-delay product and critical charge.

This manuscript is organized as follows. Section II deals with modeling of soft errors and Section III reviews the designs of the hardening latches in the technical literature, followed by the proposed designs for hardening latches in Section IV. Simulation results for evaluating and assessing the proposed latch circuits with the ones found in the technical literature are provided in Section V. Section VI deals with a further latch circuit design that provides a critical charge improvement in its operation, followed by the conclusion in the last section of this manuscript.

II. SOFT ERROR MODELING

A. Soft error metric

Soft errors occur when the collected energy Q at a particular node is greater than the critical charge, Q_{crit} , i.e. Q_{crit} is the minimum charge that needs to be deposited at the sensitive node of a storage cell to change (flip) the stored bit. In the model proposed in [12] [13], the SER (Soft Error rate) is given by

$$SER \propto N_{flux} \times CS \times e^{-\frac{Q_{crit}}{Q_s}} \quad (1)$$

N_{flux} is the intensity of the neutron flux, CS is the area of the cross section of the node, and Q_s is the charge collection efficiency (that strongly depends on doping). Q_{crit} is proportional to the node capacitance and the supply voltage. In (1), Q_{crit} exhibits an exponential relationship with the soft error rate. Therefore, Q_{crit} has been widely used as metric for assessing soft error occurrence. The charges at some node due to cosmic ray neutrons or α -particle hits generate a large transient current at that node. Therefore, a critical charge generated on some node can be modeled as a current pulse for HSPICE simulation. Fig. 1 shows the soft error occurrence model of [14]; this model is also used in this paper for simulation. In this figure, with no loss of generality and correctness, soft errors (resulting in a signal glitch) occur at an inverter. Fig.1 (a) shows the case in which the normal output value for the inverter is high and soft errors occurring at the NMOS transistor generate a negative pulse, whereas Fig.1 (b) shows the case in which the normal output value for the inverter is low and soft errors occurring at the PMOS transistor generate a positive pulse. If it is also assumed that the duration time of the transient pulse is 0.1ns, then the current source in Fig. 1 is also turned on for 0.1ns.

III. EXISTING HARDENING LATCHES

In this section, a brief review of existing hardening designs for latches is presented.

A. Reference latch

Existing hardening latch designs fall in the second hardening category as described previously. Fig.2 shows a widely used latch circuit. In this paper, this circuit is referred to as the reference latch. D denotes the input node, CLK and NCLK are the system clocks, node In1, lo1 and nq are the internal nodes belonging to the latch feedback loop, and Q is the latch output node. When CLK is high and NCLK is low, the feedback loop is not conductive and the latch is transparent. When CLK is low and NCLK is high, the input is disconnected and the previous data on node nq is retained by the feedback loop made of I1, I3 and T2 as shown in Fig.2.

As reported in [13], the critical charge, Q_{crit} , is estimated only at specific nodes having a low Q_{crit} . Such nodes can be experimentally or intuitively identified. Once they are identified, current pulses that model charge generation (shown previously in Fig. 1) are applied to these nodes [14]. Experimental results show that the value of Q_{crit} at node In1 is the lowest among nodes In1, nq, and lo1. Furthermore, this is only one tenth of the Q_{crit} of the other two nodes.

B. Existing Hardening Latches

The addition of gate capacitance to a critical node is one of the common methods to harden CMOS devices. Hardening latch designs based on this approach have been proposed in [9] and [11]. A soft error masking latch using the Schmitt trigger circuit (SEM-latch) has been proposed in [11]. The Schmitt trigger has a larger hysteresis property in voltage so that it can mask a transient pulse on

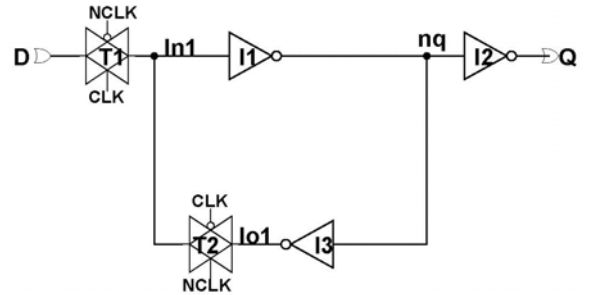


Figure 2. Normal latch as reference latch

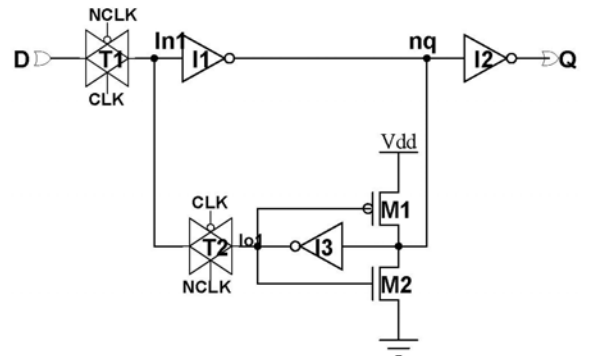


Figure 3. A Schmitt trigger based hardening latch

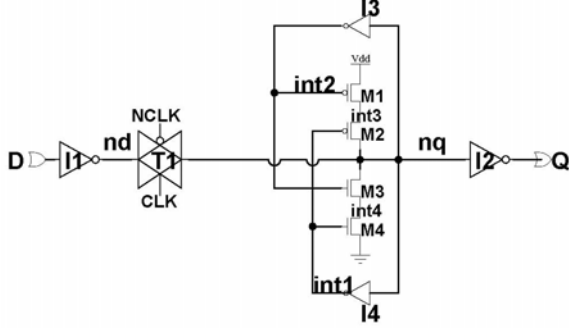


Figure 4. A split internal node low-cost latch

the input. Meanwhile, it also increases the critical charge of node In1. As shown in Fig.3, transistors M1 and M2 are added to the reference latch to make a Schmitt trigger. When CLK is high and NCLK is low, the operation of the SEM-latch is the same as the reference latch of Fig.2. When CLK is low and NCLK is high, transistors M1 and M2 make an inverter in parallel with I1. The equivalent gate capacitance at node In1 is increased, thus also increasing the critical charge at node In1. A split internal node low-cost latch (SIN-LC latch) has been proposed in [9]. As shown in Fig.4, rather than adding node capacitance, the SIN-LC latch utilizes an alternative feedback approach to harden the node. There are two inverter stages from the input of the reference latch to the output in Fig.2. Therefore, inverters I1 and I2 are added to the SIN-LC latch of [9] for fair comparison with the reference latch design. The feedback inverter of the SIN-LC latch is split into two inverters I3 and I4. Nodes int2 and int1 (i.e. the outputs of inverters I3 and I4) are connected to a series of transistors, M1-M3 and M2-M4. When CLK is low and NCLK is high, the split feedback loop can correctly hold the data on node nq by improving the critical charge at node nq. A transient pulse on node int1 or int2 will not change the data as the serially connected transistors are separately driven by int2 and int1. Therefore, TFs on node int2 or int1 will only move the node nq to a high impedance state without changing its logical value. Meanwhile, the critical charges of the nodes int3 and int4 can be increased by sizing up M1 and M4, respectively. For the SIN-LC latch, the node with the lowest critical charge is given by node nq. The increase of the conductance of the transistors M1-M4 can also significantly increase the critical charge of node nq. However, it affects the input-output delay, thus worsening its performance due to conflicts between the transistors M1-M4 and the latch input driver [9].

IV. PROPOSED HARDENING LATCHES

In this section, two new designs of hardening latches are proposed.

A. Modified SEM-Latch

The Schmitt trigger configuration used in the SEM-latch is shown in Fig.3. This design can mask a transient pulse on the input node D when CLK is high because a Schmitt trigger can suppress the glitches on the input.

When CLK is low, the additional transistors M1 and M2 provide a higher gate capacitance to slightly increase the critical charge on node In1. However, a TF will still propagate when a larger transient pulse strikes the node

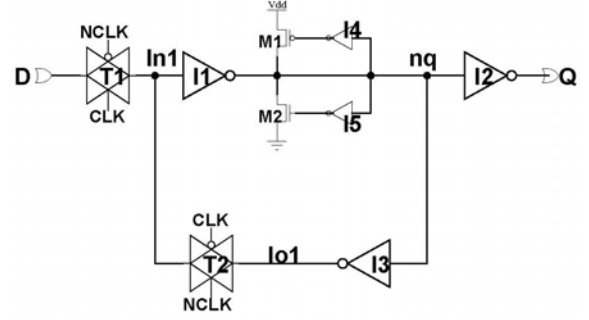


Figure 5. Modified soft error masking latch design

In1 and the positive feedback loop from M1 and M2 (together with inverter I1) amplifies the transient pulse. Thus, a TF causes a SE on the latch. The SEM-latch provides little improvement to the critical charge on node In1. A modification of the SEM-latch design can, however, provide a significant improvement in critical charge. This new design is shown in Fig.5; the positive feedback transistors M1 and M2 in Fig. 3 are replaced by inverters I4, I5 and transistors M1, M2. In the modified soft error masking latch, the feedback scheme is retained and the positive feedback from node In1 is removed. Therefore, the modified SEM-latch can still suppress the pulses on the input node D and node In1, while improving the critical charge on node In1. Simulation results show that the critical charge of the modified SEM-latch is 2.63fC at 32nm CMOS feature size, 0.9V power supply and room temperature, while the critical charge of the SEM-latch is 2.33fC. Therefore, a 13% critical charge improvement is achieved.

B. Alternative Schmitt trigger latch

Similarly to the reference latch in Fig.2, the node In1 of both the SEM-latch and modified SEM-latch is also connected to an inverter. An alternative hardening Schmitt trigger (ST) based latch is proposed in Fig. 6. In the ST latch, node In1 is connected to a Schmitt trigger that consists of six transistors [15]. When node In1 is low, node nq is high, M6 is on, and node int2 is charged. If a strike on a node goes from low to high, to change the state of node nq, the charge at node int2 needs to be discharged first. A similar scenario occurs when there is a negative pulse striking node In1. Therefore, this Schmitt trigger can provide better tolerance capabilities (robustness) to soft errors due to the charge at nodes int1 and int2. For the latch operation, when CLK is high and NCLK is low, the

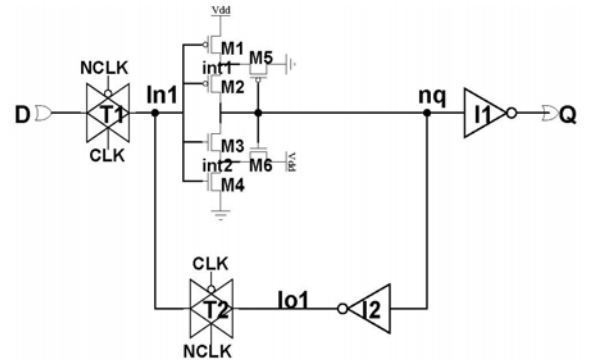


Figure 6. Proposed Schmitt trigger based latch

feedback loop is not conductive and the latch is transparent. The proposed latch will be slower due to the hysteresis property of the Schmitt trigger. When CLK is low and NCLK is high, the feedback loop (that consists of the Schmitt trigger inverter and a normal inverter I2) retains the data and the Schmitt trigger configuration provides better tolerance capabilities (robustness) to soft errors.

V. LATCH ASSESSMENT AND COMPARISON

Four hardening latches based on different Schmitt trigger configurations have been discussed in previous sections. Simulations have been performed to investigate the performance and the critical charge of these different hardening latches.

A. Performance

Fig.7 shows the basic timing diagram of a latch. CLK and NCLK are the system clock, D is the data input and Q is the data output. D_{C-Q} is the propagation delay of the latch from the clock signal CLK to the output Q. D_{D-Q} is the propagation delay of the latch from the data signal D to the output Q. T_{setup} is the minimum time between a change in the data signal and the trailing edge of the clock signal such that the new value of D can propagate to the output Q of the latch and stored in the latch during the non-transparent phase. Comparison of the performance of the different latches is based on simulation of the switching characteristics of each latch for different values of data setup as proposed in [16], i.e.

$$D = T_{setup} + D_{C-Q}. \quad (2)$$

For T_{setup} and D_{C-Q} , the max delay between positive and negative transitions (i.e. the larger value between a high to low transition and a low to high transition) is selected as metric for latch performance.

B. Critical charge

As mentioned above, the critical charge, Q_{crit} , is estimated only at specific nodes (i.e. those having low Q_{crit}). For critical charge, a lower Q_{crit} between positive and negative transient pulses is selected as the critical charge of a latch.

Experimental results show that the nodes that have the lowest Q_{crit} in the reference latch, the SEM-latch, the Modified SEM-latch, and the ST latch are the same, i.e. node ln1 in all circuits has the lowest Q_{crit} . Comparison of

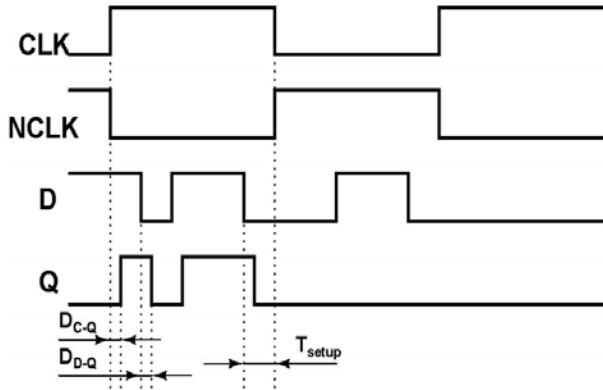


Figure 7. Timing diagram of a level-sensitive latch

TABLE I.
CRITICAL CHARGE, PERFORMANCE, POWER COMPARISON BETWEEN
SCHMITT TRIGGER BASED HARDENING LATCHES

Latches	Q_{crit} (fC)	Power Consumption (nW)	T_{setup} (ps)	D_{C-Q} (ps)	D (ps)
Reference latch	1.62	189.0	9	44.48	53.48
SEM-latch	2.33	206.7	19	49.19	68.19
Modified SEM-latch	2.63	217.7	20	50.75	70.75
ST latch	3.00	212.9	16	54.40	70.40

these four latches on critical charge, performance, and power consumption is presented in Table 1. Simulations have been performed on these four Schmitt trigger based latches with equivalent sized transistors at 32nm CMOS feature size, 0.9V power supply, and room temperature. From Table 1, it is shown that by utilizing a Schmitt trigger configuration in the latches, the critical charge of the latch increases 43%, 62%, and 85% for the SEM-latch, the Modified SEM-latch, and the ST latch, respectively, while the delay and power performance degrade at a smaller penalty.

C. Power-delay product and critical charge plot

High soft error tolerance must be achieved at low power and performance cost. The power-delay product is an often used measure for logic circuits; it is also used in this paper to establish the power and performance cost of the hardening latches. For the reference latch, the SEM-latch, and the ST latch, the critical charge can be increased by increasing the gate capacitance at node ln1. For the SIN-LC latch, the increase in conductance of transistors M1-M4 can significantly increase the critical charge of node nq. In the Modified SEM-latch, the source and drain capacitances increase of the transistors M1 and M2 will increase the critical charge on node ln1. All of these techniques result in an increase of both power consumption and propagation delay of the hardening latches, thus degrading the power-delay product, which is a very important metric for digital CMOS circuit. Therefore, it is necessary to investigate the relationship between the power-delay product and the critical charge on the different latch circuits. In this paper, the power-delay product of a latch is defined as follows:

$$Power - delay = Power \times D_{C-Q}. \quad (3)$$

Transistor sizing can have a significant impact on the critical charge of a CMOS circuit [17]. In the reference latch and the SEM-latch, the transistors of the inverter I1 are increased. For the Modified SEM-latch in Fig.5, the transistor sizes of M1 and M2 are increased. For the ST latch in Fig.6, an increase in sizing of the transistors M1-M4 is required. For the SIN-LC latch, the transistors M1-M4 are also increased to have a higher critical charge value at node nq. By increasing gate sizing, the power-delay product will increase too. Fig. 8 shows the relationship between the power-delay product and the

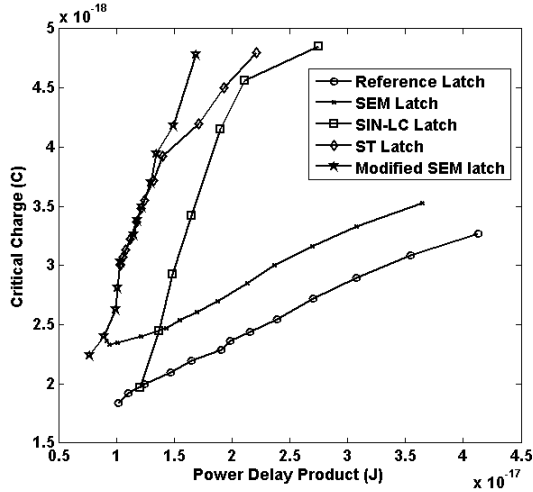


Figure 8. Plot of power-delay product vs critical charge for different latch designs

critical charge on the reference latch, the SEM-latch, the Modified SEM-latch, the SIN-LC latch, and the ST latch. As shown in Fig.8 the SEM-latch utilizes a parallel additional inverter to the existing feedback loop during the non-transparent state, so it has a similar slew rate in the plot. Compared to the SEM-latch, the Modified SEM-latch, the ST latch, and the SIN-LC latch achieve a significantly larger value of critical charge at a lower power-delay product. As shown in Fig.8, the proposed ST latch and the Modified SEM-latch are the latch configurations that provide the highest critical charge at a given power-delay product. Therefore, these two latches achieve the best soft error tolerance at the lowest cost. However, compared with the Modified SEM-latch (that has 16 transistors); the proposed ST latch (with only 14 transistors) has also the smallest transistor count among all hardening latch designs. Layout design based on MOSIS deep sub-micrometer design rules [18] shows the proposed ST latch has only 10% area increase compared with the reference latch in Fig.2, and 4.7% area increase compared with SEM-latch shown in Fig.3.

VI. IMPROVEMENT OF CRITICAL CHARGE

In the ST latch shown in Fig.6, the feedback loop consists of an inverter I2 and a clock-controlled transmission gate T2. An alternative configuration of the feedback loop is shown in Fig.9, in which both latches work exactly the same using a digital cascode

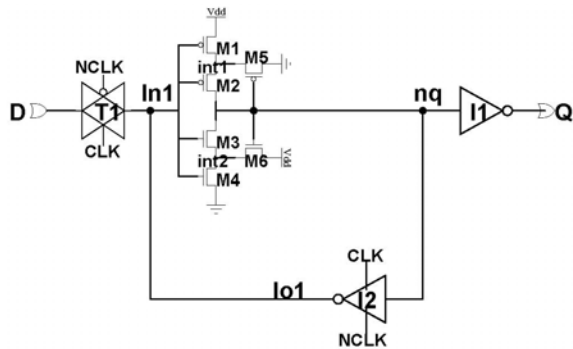


Figure 9. Cascode feedback Schmitt trigger (Cascode ST) latch

configuration. When the CLK is high and NCLK is low, the latch is transparent, the feedback loop is on and the latch retains the data when the CLK is low and NCLK is high. However, the feedback configurations in Fig.6 and Fig.9 are different from the operation of exiting the metastable state at the data-retaining phase. In a hardening latch design, a maximum gain-bandwidth product of the positive feedback loop is required to exit the metastable state because the loop has a better immunity to a TF. For the feedback configuration in Fig.6, the feedback inverter can be treated as an ordinary common source (CS) amplifier. Therefore, the Miller capacitance is larger because it is amplified by the small-signal gain of the CS stage that is usually large. The cascode configuration reduces the Miller effect because the gain is nearly one. As reported in [19], the cascode configuration provides a better capability to exit the metastable state than the transmission gate configuration due to the reduced Miller effect that will degrade performance when used for a small-signal amplifier. Simulation results show that a ST latch with a cascode feedback (Cascode ST Latch) achieves a critical charge of 3.34fC at 32nm CMOS feature size, 0.9V power supply, and room temperature,

TABLE II.
CRITICAL CHARGE, PERFORMANCE, POWER COMPARISON BETWEEN TWO DIFFERENCE FEEDBACK CONFIGURATIONS

Latches	Q_{crit} (fC)	Power Consumption (nW)	T_{setup} (ps)	D_{C-Q} (ps)	D (ps)
ST latch	3.00	212.9	16	54.40	70.40
Cascode ST latch	3.44	209.6	16	53.90	69.90

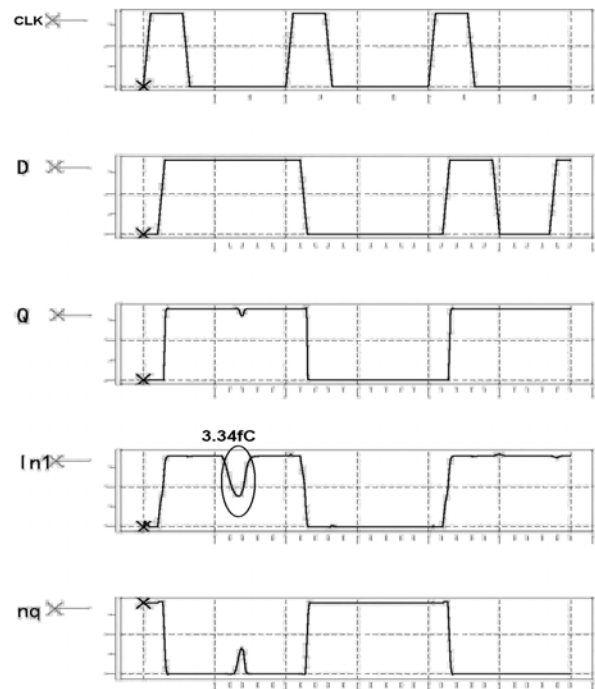


Figure 10. Timing diagram of the modified ST latch

compared to 3.00fC of a ST latch with a transmission gate feedback. When CLK is high and NCLK is low, the latches in Fig.6 and Fig.9 operate similarly, and there is not too much difference between the power and delay performance of the ST latch and the Cascode ST latch. Table 2 shows the comparison between these two latches.

Fig.10 shows the simulated timing diagram of the cascode feedback ST latch of Fig.9. When CLK is high and NCLK is low, the feedback loop is cut off and the latch is transparent to the input signal D. When the CLK is low and NCLK (NCLK is the complementary signal of CLK, which is not shown in Fig.10) is high, the transmission gate T1 is off and the feedback loop retains data. A transient charge of 3.34fC is applied to node In1, and simulation results show that the feedback loop retains the correct data. Compared to the ST latch in Fig.6, the cascode ST latch achieves an 11% critical charge improvement without any power and performance loss.

VII. CONCLUSION

This paper has presented new designs for hardening latch circuits in nano-CMOS. Single event upset is modeled in HSPICE to determine soft error susceptibility of a memory element. Novel configurations for latches have been proposed, analyzed, and simulated using the predictive technology file at 32nm [20] for tolerance to soft errors. Three novel designs of hardening latches have been proposed; two of them are based on a Schmitt trigger circuit while the last one utilizes a cascode configuration. In all cases, simulation has shown that the proposed designs have excellent tolerance to soft errors and high performance (as established through a power-delay product versus critical charge plot). These designs outperform the existing latch configurations of [8] [9] [11], and provide excellent performance at the reduced feature size of 32nm.

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