

Performance Evaluation of CNFET-Based Logic Gates

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Abstract— As the physical gate length of current devices is reduced to below 65 nm, effects (such as large parametric variations and increase in leakage current) have caused the I-V characteristics to be substantially depart from those commonly associated with traditional MOSFETs, thus impeding the efficient development and manufacturing of devices at deep sub-micro/nano scales. Carbon Nanotube Field Effect Transistors (CNFETs) have received widespread attention, as one of the promising technologies for replacing MOSFETs at the end of the Technology Roadmap. This paper presents a detailed simulation-based assessment of circuit performance of this technology and compares it to conventional MOSFETs; the designs of different logic gates and the full adder circuit are simulated under the same minimum gate length and different operational conditions. It is shown that the power-delay product (PDP) and the leakage power for the CNFET based gates are lower than the MOSFET based logic gates by 100 to 150 times, respectively. The CNFET based logic gates demonstrate good functionality even at a 0.3V power supply (while MOSFET based gates fail at 0.5V).

Carbon Nanotube Field-Effect Transistors (CNFETs); Fan-out; Power; Delay; Power Delay Product (PDP); Temperature

I. INTRODUCTION

As per Moore's law, the number of transistors of an integrated circuit is increasing exponentially by almost doubling every two years. Technology scaling has been pursued aggressively to meet the density and sustain the IC predicted by Moore's law. Since 2006, the gate length of a MOSFET device has entered the deep submicron/nano region at the 65 nm feature size. Today, 45 nm technology is reality, and 32 nm has been predicted as feature size in the near future [1]. As the physical gate length is reduced to below 65 nm, many device-level effects (such as large parametric variations and exponential increase in leakage current) have substantially affected the I-V characteristics of traditional MOSFETs, thus resulting in major concerns for scaling down the feature size of these devices. A possible approach to meet the challenges of nano scale CMOS consists of utilizing new circuit techniques together with alternative technologies to replace conventional silicon and the current MOSFET-based technology. Recently, there have been tremendous advances in carbon nanotube (CNT) technology for nano-electronics applications.

The Carbon Nanotube Field Effect Transistor (CNFET) is one of the most promising devices among emerging technologies. The CNFET offers many potential advantages with respect to silicon-based technology. Its operation principles and device structure are similar to CMOS, and therefore the mature design infrastructure of this latter technology can be utilized, together with its fabrication process. As reported in the technical literature, the CNFET has been experimentally demonstrated to have excellent current capabilities; an estimate of the performance of CNFETs at single device level in the presence of process related effects and imperfections at 32 nm feature size (using the CNFET SPICE model) has been provided in [2][3]. In this paper, a performance assessment and comparison against bulk nano CMOS are pursued at circuit level for delay and low power applications. The same gate length is utilized for the transistors of these two technologies. Different logic gates and the often used benchmark circuit of a full adder are used to investigate the performance of this new technology.

In this paper circuit simulation uses a 32nm CNFET HSPICE model that includes non-ideal effects for the CNFET [4][5] and the 32nm BSIM PTM (predictive technology model) for the Si MOSFET [6]. Logic gates such as the inverter, NAND, NOR, and the Full Adder (FA) are investigated for performance, energy efficiency, and leakage current under various operational conditions by considering fan-out, power supply voltage and temperature.

II. CNFET DEVICE SIZING

The inverter is the fundamental logic gate for digital circuit design. Many of the basic principles employed in the design and analysis of an inverter can be also applied to complex logic gates/circuits such as NOR, NAND, XOR, and FA. To compare the performance of the MOSFET and CNFET, the P-transistor/N-transistor ratio of the MOSFET and CNFET inverters should be established. In general for Si CMOS, a PMOS/NMOS ratio of 2 or 3 is used because the NMOS mobility is about 2 or 3 times higher than for the PMOS transistor. A 3:1 (PMOS:NMOS) ratio is used in this simulation because at this value, the voltage transfer characteristic (VTC) of the MOSFET inverter shows a more symmetrical shape for the 32nm technology (as shown in Fig. 1). However for CNFETs, a PCNFET /NCNFET ratio of 1 is

used because the NCNFET and PCNFET have the same current driving capabilities with same transistor geometry [3]. In CMOS design, the width of the MOSFET is adjusted to change the PMOS/NMOS ratio. However in a CNFET, the number of tubes is the design parameter (such as the W/L ratio in conventional design) for changing the current and resistance. Therefore, in this paper, when the width of the CNFET is increased, the number of tubes is increased.

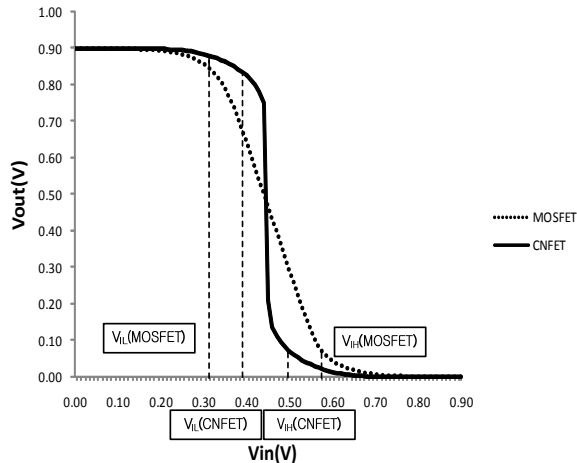


Figure 1. Voltage Transfer Characteristic (VTC) for 32nm MOSFET and 32nm CNFET at 0.9V power supply voltage.

The Voltage Transfer Characteristic (VTC) curves of the 32nm MOSFET and 32nm CNFET are shown in Fig. 1, for minimum size MOSFET and CNFET inverters' functionality. The curve is symmetric and the logic threshold voltage (V_{inv}) is in the center ($V_{inv}=V_{out}=V_{in}=V_{DD}/2$). Even though the amount of current of a CNFET is smaller than for the minimum sized MOSFET at 32nm, the CNFET can have a steeper curve in the transition region (due to the higher gain than the MOSFET [3]). This contributes to a 22.5% improvement in Noise Margin (NM); this improvement in performance is still preserved at a reduced power supply voltage, as shown in Fig. 2.

III. POWER DELAY PRODUCT

Due to the increased demand for high-speed computation and complex functionality in high density mobile circuits, reductions in delay and power consumption are very challenging. The propagation delay is mostly determined by the speed at which the energy can be stored on the gate capacitors of the transistors of an IC. A faster energy transfer requires a higher power consumption, thus operating at a faster speed. For a technology and gate topology, the product of the power consumption and the propagation delay is generally constant [7]. The performance of the MOSFET and the CNFET can be compared using the Power Delay Product (PDP) as metric.

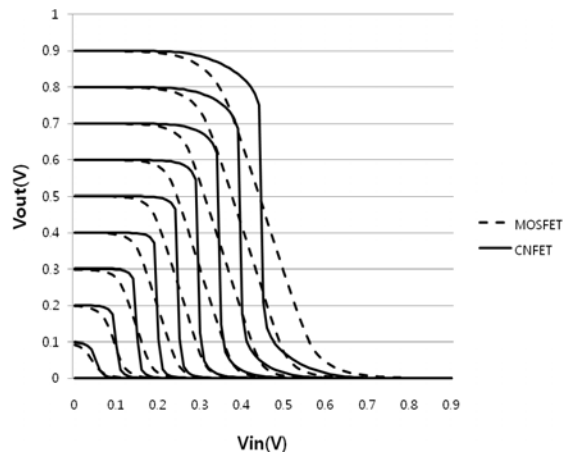


Figure 2. Voltage Transfer Characteristic (VTC) for 32nm CNFET and 32nm MOSFET as function of power supply voltage.

Fig.3 shows the Power Delay Product (PDP) of the 32nm MOSFET and CNFET based logic gates; the PDP of the 32nm MOSFET is about 100 times higher than for the 32nm CNFET. The difference becomes more pronounced (about 1000 time) for the FA. In general, if the fan-out is increased, the delay of the driving gate and the power consumption are also increased to drive the increased capacitive load, thus resulting in an increase of the PDP as shown in Fig.4. Even though the PDP of a CNFET based gate is also increased as the fan-out increases, the load dependent slope is almost the same as for the corresponding MOSFET gate. Therefore, the overall PDPs of the CNFET gates are much lower than for the MOSFET gates.

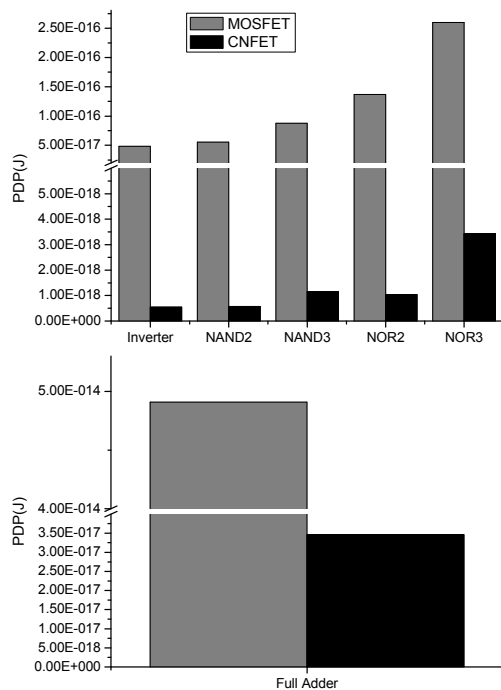


Figure 3. Power Delay Product (PDP) for 32nm MOSFET and 32nm CNFET, at $V_{dd}=0.9V$

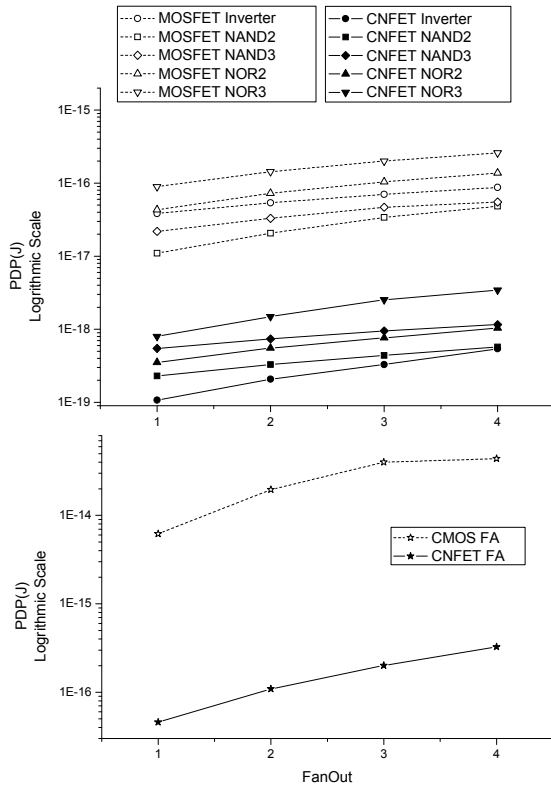


Figure 4. Power Delay Product (PDP) for 32nm MOSFET and 32nm CNFET, at $V_{dd}=0.9V$

IV. LEAKAGE

Power consumption can be classified into three types, i.e. short circuit current, static power consumption and dynamic power consumption. The short circuit current can be reduced using appropriate circuit techniques; however, as process dimensions shrink further into the nanometer ranges, traditional methods for dynamic power reduction are becoming less effective due to the increased impact of static power. In nanometer MOSFET circuits, the main components of static power are sub-threshold, gate tunneling, and reverse-biased junction band to band tunneling leakage current [8][9][10][11][12]. For a CNFET, the main leakage component is the band to band tunneling leakage because the leakage current is controlled by the full band gap of the CNTs and band to band tunneling. The other leakage currents are relatively small and can be reduced by new techniques such as utilizing high-k dielectric materials [13][14][15][16]. Figure 5 shows the average leakage power for 32nm MOSFET and CNFET gates and FA. For logic gates, the average leakage power of the MOSFET is 150 times larger than the CNFET based gates; especially for the FA, the leakage power of the MOSFET becomes 250 times bigger than for the CNFET.

Another advantage of a CNFET based gate is the low power supply operation. When the supply voltage is reduced to 0.5V, the MOSFET based FA does not operate any more, while

the CNFET based FA still operates till the supply voltage is reduced to 0.3V. Figure 6 shows the average leakage power of the MOSFET and CNFET gates when the supply voltage is reduced until the FA fails. It shows that even though the average leakage power of the MOSFET gates is reduced as the supply voltage decreases, the overall leakage power is greater than for the CNFET FA. This leakage power advantage of the CNFET technology is also retained at high temperature operation as shown in Fig. 7. As temperature is increased, the average leakage power of the CNFET FA increases too. However, the total leakage power is significantly smaller than the leakage power of the MOSFET gates.

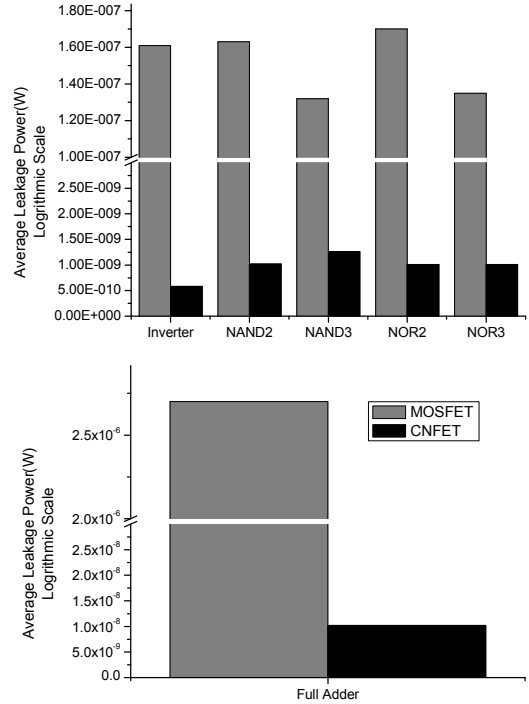


Figure 5. Average Leakage Power for 32nm MOSFET and 32nm CNFET, at $V_{dd}=0.9V$.

V. CONCLUSION

The Carbon Nanotube Field Effect Transistor (CNFET) is one of the most promising devices among emerging technologies to extend and/or complement a traditional Si MOSFET. In this paper, delay and leakage power consumption of the Si MOSFET and CNFET have been assessed and compared using the same minimum gate channel length for various logic gates and the full adder circuit. Simulation results have shown that the PDP and the leakage of the MOSFET logic gates are 100 and 150 times higher than for the CNFET logic gates, respectively. For the full adder, the difference in these figures of merit for these two technologies becomes larger. Finally, this paper has demonstrated the advantages offered by CNFET gates under different operational conditions such as extremely low power supply voltage and high temperature. The quantitative results of this paper have confirmed that the CNFET technology is a viable solution to replace conventional

bulk MOSFET technology and in particular it has made possible to estimate the delay and power benefits that can be attained by utilizing CNFETs versus today's MOSFETs.

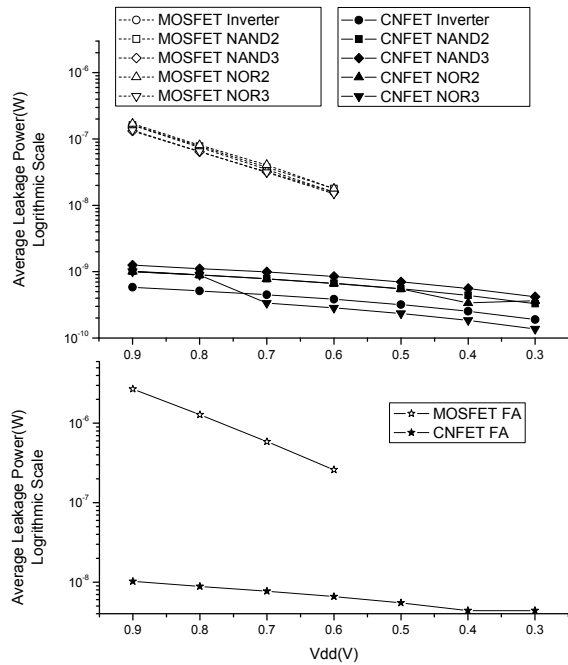


Figure 6. Average Leakage Power for 32nm MOSFET and 32nm CNFET versus supply voltage.

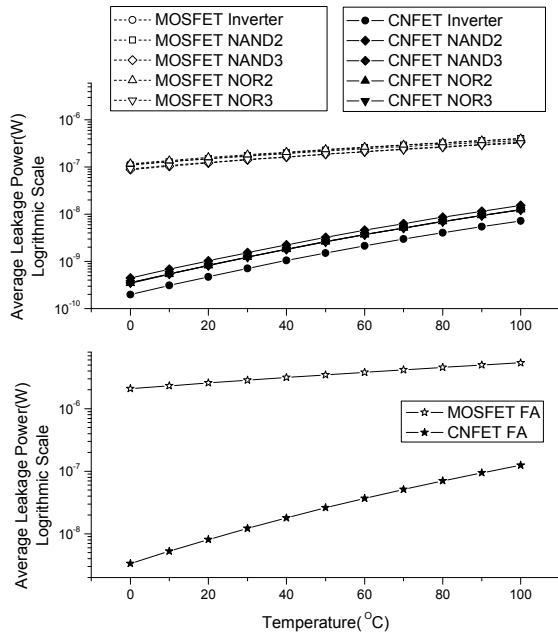


Figure 7. Average Leakage Power for 32nm MOSFET and 32nm CNFET versus temperature.

VI. REFERENCE

- [1] M. Horowitz, E. Alon, D. Patil, "Scaling, Power, and the Future of CMOS," *IEDM*
- [2] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, and M. Radosavljevic, "Benchmarking nanotechnology for high-performance and low-power logic transistor applications," *IEEE Trans. Nanotechnol.*, vol. 4, no. 2, pp. 153-158, Mar. 2005.
- [3] J. Deng, "Device modeling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45 nm node and carbon nanotube field effect transistors," Doctoral Dissertation, Stanford University, 2007.
- [4] J. Deng, and H.-S. P. Wong, "A Circuit-Compatible SPICE model for Enhancement Mode Carbon Nanotube Field Effect Transistors," Proc. Intl. Conf. Simulation of Semiconductor Processes and Devices, pp. 166 - 169, Sept., 2006.
- [5] I. Amlani, et al., "First Demonstration of AC Gain From a Single-walled Carbon Nanotube Common-Source Amplifier," Proc. Intl. Electron Devices Meeting, Paper 20.7, Dec., 2006.
- [6] <http://www.eas.asu.edu/ptm/latest.html>
- [7] J. M. Rabaey, et al, "Digital Integrated Circuits: A Design Perspective," Second Edition, Prentice Hall, 2007
- [8] K. K. Kim, "PVT Variation-Aware Power Management System for SoC Design Based on Nanometer MOSFET Technology," Doctoral Dissertation, Northeastern University, 2007.
- [9] S. G. Narendra, A. Chandrakasan, "Leakage in nanometer CMOS technologies (Series on Integrated Circuits and Systems)," Springer, Nov. 2005.
- [10] K. Roy and S. C. Prasad, "Low-power cmos vlsi circuit design," John Wiley & Sons Inc., 2000.
- [11] A. P. Chandrakasan and R. W. Brodersen, "Low power cmos digital design," Kluwer Academic Publishers, 1995.
- [12] A. Chandrakasan, W. J. Bowhill, and F. Fox, "Design of high-performance microprocessor circuits," The Institute of Electrical and Electronics Engineers, Inc., New York, 2001.
- [13] J. Guo, A. Javey, H. Dai, S. Datta, and M. Lundstrom, "Predicted performance advantages of carbon nanotube transistors with doped nanotubes as source/drain," Condense Matter, cond-mat/0309039: <http://arxiv.org/abs/cond-mat/0309039>, 2003.
- [14] Radosavljevic et al., "Drain Voltage Scaling in Carbon Nanotube Transistors," Applied Physics Letters, 2003. 83 (12) 2435-2437.
- [15] G. Chakraborty et al, "Study of the tunnelling initiated leakage current through the carbon nanotube embedded gate oxide in metal oxide semiconductor structures," 2008 Nanotechnology 19 255401 (7pp).
- [16] J. Guo, A. Javey, H. Dai, and M. Lundstrom, "Performance analysis and design optimization of near ballistic carbon nanotube FETs," *IEDM tech. digest*, pp. 703--706, 2004.