A Low Power 8T SRAM Cell Design technique for CNFET

Young Bok Kim, Yong-Bin Kim, Fabrizio Lombardi
Dept. of Electrical and Computer Engineering
Northeastern University
Boston, USA
{youngbok, ybk, Lombardi}@ece.neu.edu

Young Jun Lee
NextChip Corp.
Seoul, Korea
yjlee@nextchip.com

Abstract— **In this paper, a new SRAM cell design based on Carbon Nanotube Field-Effect Transistor (CNFET) technology is proposed. Carbon nanotube with their superior transport properties, excellent thermal conductivities, and high current handling capacities has proved to be a promising alternative device to the conventional CMOS. The proposed SRAM cell design on CNFET is compared with SRAM cell designs implemented with the conventional CMOS and FinFET in terms of speed, power consumption, stability, and leakage current in this paper. The HSPICE simulation and analysis show that the dynamic power consumption of the proposed 8T CNFET SRAM cell's is reduced about 48% and the SNM is widened up to 56% compared to the conventional 6T CMOS SRAM structure at the expense of 2% leakage power and 3% write delay increase.**

Keywords-CNFET, carbon nano tube, SRAM, low power

I. INTRODUCTION

An estimated 70% of the transistors in a billion-transistor superscalar microprocessor are expected to be used for memory arrays, especially for large L2 and L3 SRAM data caches. Therefore, it is essential to develop a low power SRAM design technique for the new device technology such as CNFET.

As one of the promising new transistors, Carbon Nanotube File Effect Transistor (CNFET) avoids most of the fundamental limitations of the traditional silicon MOSFETs. With ultra long (~1µm) mean-free-path (MFP) for elastic scattering, ballistic or near ballistic transport can be obtained by intrinsic CNT under low voltage bias to achieve the ultimate device performance [1].

Efforts have been made in recent years on modeling and simulating CNT related devices such as CNFET [2] and CNT interconnects [3] to evaluate the potential performance at the device level. However, the dynamic performance of a complete circuit system, consisting of more than one CNFETs and interconnects, differs from that of a single device.

In this paper, as a circuit level design of CNFET, a novel low power 8T SRAM cell design is proposed and its performance and viability are demonstrated by performing various simulations. The performance, power consumption, stability, and leakage currents of the 6T and 8T SRAM cell based on CNFET are compared with those of the conventional CMOS and FinFET based SRAM cell designs to show the viability of the CNFET based SRAM cell design.

In section II, the characteristics and physical features of CNFET are explained, and the mechanisms of the read and write operations of the proposed 8T CNFET SRAM cell are explained and the schemes for deciding the number of nanotubes of each CNFET are described in section III. In section IV, the simulation results are presented to compare the performance and viability of the CNFET technology with those of other technologies, followed by the conclusion in Section V.

II. CNFET TECHNOLOGY

CNTs are sheets of grapheme rolled into tubes. Depending on their chirality (i.e., the direction in which the grapheme sheet is rolled), the single-walled CNTs can either be metallic or semiconducting. Semiconducting nanotubes have attracted widespread attention of the electron device and circuit designers as a promising channel material for high-performance transistors [4],

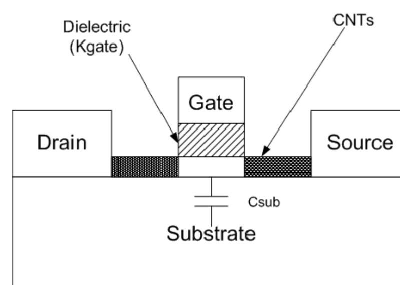

Figure 1. CNFET Structure

A typical structure of a MOSFET-like CNFET device is illustrated in Fig 1. The CNT channel region is undoped, and the other regions are heavily doped, acting as both the source/drain extension region and/or interconnects between two adjacent devices.

Carbon nanotubes are high-aspect-ratio cylinders of carbon atoms. The electrical properties of the single wall carbon

nanotube (SWNT) offer the potential for molecular-scale electronics. A typical semiconducting single-wall carbon nanotube is 1.4nm in diameter with 0.6 eV bandgap (inversely proportional to the diameter). Recent carbon nanotube field effect transistors (CNFETs) have a metal carbide source/drain contact [8] and a top gated structure (Fig. 1) with thin gate dielectrics [9]. The contact resistance and subthreshold slope are comparable to the silicon FET. Note that the silicon FET current drive is typically measured in current per unit device width (e.g. µA/µm). Since the nanotube diameters are fixed, it is assumed the CNFET is constructed as an array of carbon nanotubes which occupy equal lines and spaces

III. PROPOSED 8T CNFET SRAM CELL

A. Write/Read Operations

In the proposed 8T SRAM, the write and read bits are separated. While bit and bit-bar lines are used for writing data in the traditional 6T SRAM, only the WRITE_BIT in Figure 2 is used in the proposed SRAM cell to write for both "0" and "1" data. The writing operation starts by disconnecting the feedback loop of the two inverters. By setting 'W_bar' signal to "0", the feedback loop is disconnected. The data that is going to be written is determined by the WRITE_BIT voltage. If the feedback connection is disconnected, SRAM cell has just two cascaded inverters. WRITE_BIT transfers the complementary of the input data to Q2, cell data, which drives the other inverter (P2 and N2) to develop Q_bar. WRITE_BIT have to be pre-charged "high" before and right after each write operation. When writing "0" data, negligible writing power is consumed because there is no discharging activity at WRITE_BIT. To write '1' data at Q2, The WRITE_BIT have to be discharged to ground level, just like 6T SRAM cell. In this case, the dynamic power consumed by the discharging is the same as 6T SRAM. The write circuit does not discharge for every write operation but discharges only when the cell writes "1" data, and the activity factor of the discharging WRITE_BIT is less than "1", which makes the proposed SRAM cell more power effective during writing operation compared with the conventional ones.

All the Read_Bit lines are pre-charged before any READ operation. During read operation, transistor N5 is turned on by setting W_bar signal high and the READ_ROW(RD) is "high" to turn on N6. When Q2="0", the N4 is off making the READ_BIT voltage not change from the pre-charged value, which means the cell data Q2 holds "0". On the other hand, If Q2= "1", the transistors N4 and N6 are turned on. In this case, due to charge sharing, the READ_BIT voltage will be dropped about 100~200mV, which is enough to be detected in the sense amplifier

B. Carbon nanotube configuration

The operation of writing "1" is stable because NMOS transistor N3 can pass "0" faithfully.

On the other hand, when writing "0", WRITE_BIT is pre-charged high (V_{DD}) and N5 is turned off. The node voltage at Q1 is less than V_{DD} due to the threshold voltage drop between the gate and source of the transistor N3. To compensate this voltage drop, the transistor N2 and P2 must be designed as a low-skew inverter to ensure Q2 to be solid ground level to represent "0" state.

A low-skewed inverter has a weaker PMOS transistor. If the PMOS CNFET have only one tube, the current is minimum.

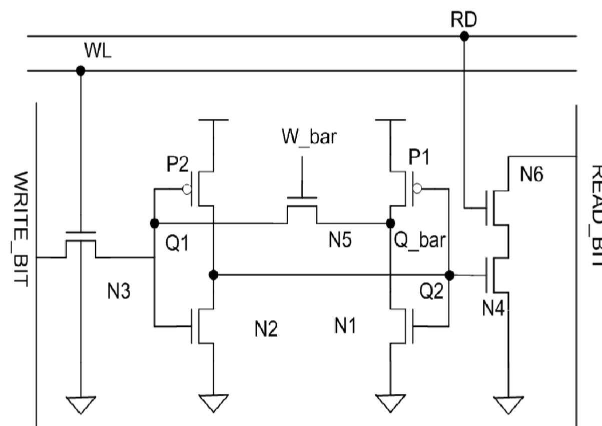

Figure 2. The proposed 8T SRAM structure

Let's suppose that the cell stores "0" at Q2 and "1" at Q_bar after WL(Word Line) is deactivated and W_bar is activated. In this case, the voltage at Q1 is less than V_{DD} due to the threshold voltage drop across the gate and source of the transistor N5. The degraded voltage at Q1 may turn on the transistor P2 slightly causing short circuit current through transistors P2 and N2. To overcome this problem, the low skewed inverter (N2 and P2) mentioned for writing "0" case is justified again and the V_{th} of the transistor N5 needs to be controlled low to reduce the voltage difference between Q_bar and Q1.

To implement a low skewed inverter with transistors N2 and P2, transistor ratio of N2 to P2 should be at least 2 to have a solid ground level at Q2. However, by increasing the number of tubes, the P2 and N2 area sizes can be same. That is, if P2 has only one tube and N2 has 2 tubes, then the current ratio N2/P2 can be more than 2. This means that the inverter transistor sizes N2/P2 can be smaller than 2 by controlling the number of tubes. Transistor ratio N3/P2 of 1.3, N1/P2 of 3, and low V_{th} of the transistor N5 guarantees a stable READ operation when Q_bar stores "0".

However, if the similar approach to N2/P2 sizing is used to optimize transistor ratios among N1, N3 and P2, the transistor sizes can be further reduced. If N3 has only one tube, N1 has two tubes and P2 has one tube, the transistor N1 needs to be only 1.5 times larger than transistor P2 to satisfy the relationships among N1, N3, and P2. Combining the threshold voltage controllability of the CNFET varying the diameter of tubes and transistor sizing techniques, the proposed 8T SRAM cell can accomplish low power consumption due to smaller node capacitance and tuning V_{th} at the minimal cost of the area overhead.

IV. SIMULATION RESULTS

In this paper, total 8 different SRAM cells are designed; Each 6T SRAM and 8T SRAM cells are designed using tied FinFETS (front and back gates of the FinFETS are tied together), independent double gates FinFETS(front and back gates are independently controlled), CMOS and CNFET.

The 6T independent gate FinFET SRAM (6T-Ind) is implemented by using independent gate control which connects the back gates of the NMOS (PMOS) transistors to GND (V_{DD}) to reduce the leakage current .

An independent-gate FinFET operates in the dual-gate mode (DGM) when both gates are biased to induce channel inversion. Alternatively, an independent-gate n-FinFET (p-FinFET) operates in the single-gate mode when one of the gates is deactivated by connecting the gate to ground (V_{DD}). Disabling one of the gates in the single-gate mode (SGM) increases the absolute value of the threshold voltage compared to DGM. Therefore, it is possible to modulate the threshold voltage of the FinFET by biasing the two gates independently [7]. And the proposed 8T SRAM (8T-Ind) configuration is that back gate of PMOS connected to the V_{DD} and front and back gates of N1, N2, N6 are tied together and back gate of N3, N4 are connected together.

A. Simulation setup

The technology parameters for the FinFETs are; channel length (L) = 32nm, fin height (Hfin) = 32nm, fin thickness (tsi) = 8nm, oxide thickness(tox) = 1.6nm, channel doping = 2 x 1020 cm-3 ,source/ drain doping = 2 x 1020 cm-3, work functions (N-FinFET) = 4.5eV , work functions (P-FinFET) = 4.9eV.

The technology parameters for the CNFETs are : physical channel length = 32.0nm, 10nm (this value used in simulations for performances with V_{DD} variations), the length of doped CNT drain-side/source-side extension region = 32.0nm , fermi level of the doped S/D tube. = 0.6 eV, the thickness of high-k top gate dielectric material = 4.0nm, chirality of tube = (19,0), Pitch = 10nm, Vfbn, Vfbp (flatband voltage for n-CNFET and p-CNFET) = 0.0eV, 0.0eV , physical gate length = 32.0nm, The mean free path in intrinsic CNT = 200.0nm, the length of doped CNT source/drain extension region. = 32.0nm, the mean free path in p+/n+ doped CNT = 15.0nm, the work function of Source/Drain metal contact = 4.6eV, CNT work function = 4.5eV.

The minimum transistor sizes used for those technologies are W=48nm and L = 32nm for bulk CMOS, Hfin =32nm and L = 32nm for FinFET, and L=32nm and the number of tubes =1 for CNFET.

The HSPICE using the Predictive Technology Model (PTM) model and Stanford University CNFET model is used to simulate the performance of the proposed 8T SRAM and the conventional 6T SRAM cells designed with CMOS, FinFET, and CNFET transistors. Table 1 shows the summarized results to compare the proposed 8T CNFET SRAM characteristics to the conventional 6T SRAM cells implemented using other technologies.

B. Dynamic Power Consumption

The proposed 8T SRAM achieves 48% writing power saving while maintaining the cell performance, read/write delay, and stability of the conventional cell. The power saving comes from the fact that the cell keeps WRITE_BIT "high" instead of discharging when it writes "0", which reduces the activity factor of the WRITE_BIT.

TABLE I Summarized simulation results

6T vs 8T Carbon Nano Tube, FinFET, CMOS SRAM performances								
	6T Carbon	8T Carbon	6T-Tied FinFET	6T-ind FinFET	8T-Tied FinFET	8T-Ind FinFET	6T-CMOS	8T-CMOS
Dynamic Power	4.42E-07	2.28E-07	1.42E-06	1.41E-06	6.78E-07	6.73E-07	2.01E-06	1.18E-06
Leakage Power	6.24E-09	6.34E-09	7.32E-08	6.02E-08	7.52E-08	6.42E-08	1.13E-07	1.14E-07
Write Delay(ps)	6.3	6.6	28.3	30.3	27.3	29.3	35.3	36.3
Read Delay(ps)	7.25	7.16	22.25	25.1	23.16	25.7	25.1	23.16
SNM(mv)	198	254	123	164	198	202	124	162

While conventional 6T SRAM always discharges one of the bit lines to write a data into the cell, the proposed 8T SRAM discharge the WRITE_BIT only when it writes “1”. As the probability of writing ‘0’ gets higher, the power dissipation due to the bit line discharging is reduced comparing to the conventional case.

CNFET shows about 5 times less power consumption compared to CMOS.

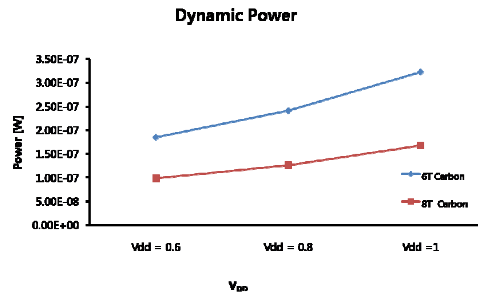

Figure 3. The Dynamic Power consumption with V_{DD} variation

Fig. 3 shows the dynamic power consumption of the CNFET 8T SRAM cell for different V_{DD}. As shown in the Fig. 3, the power saving of the 8T SRAM on CNFET becomes greater as V_{DD} increases since the dynamic power difference between the 6T SRAM and the proposed 8T SRAM increases exponentially as V_{DD} increases.

C. Leakage Power Consumption

Table 1 and Figure 4 show the leakage power of the 6T and 8T CNFET SRAM cell. The proposed 8T SRAM cell design shows slightly higher leakage power because it has one more leakage current path than the conventional SRAM cell. The READ_BIT, N4, N6 constitutes an additional leakage current path. However, N4, N6 has a stack effect that reduces the sub-threshold leakage current a bit. As a result, the leakage current through the READ_BIT, N4, and N6 path is relatively small. The difference of the leakage current in all of the four configurations is less than 2%.

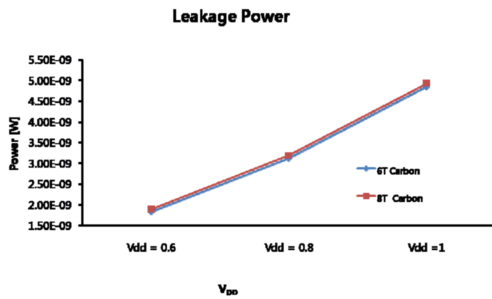

Figure 4. The Leakage Power consumption with V_{DD} variation

D. Cell Stability

Figure 5 shows the Static Noise Margin (SNM) difference between the conventional 6T SRAM and the proposed 8T SRAM. Static Noise Margin is the standard metric to measure the stability in SRAM bit-cells [11]. The static noise margin of SRAM cell is defined as the minimum DC noise voltage necessary to flip the state of the cell. The voltage transfer curves (VTCs) of the back-to-back inverters in a bit-cell are used to measure SNM [11]. Separating the Read and Write bit offers wider SNM during read operation as shown in Figure 4. When reading the stored data, only READ_BIT affects inv1 (N1/P1) output voltage. Consequently, this fact makes the cell hard to flip. And Table 1 shows CNFET have the highest SNM because of the relatively higher Vth and lower leakage current than CMOS and FinFET based SRAM cells.

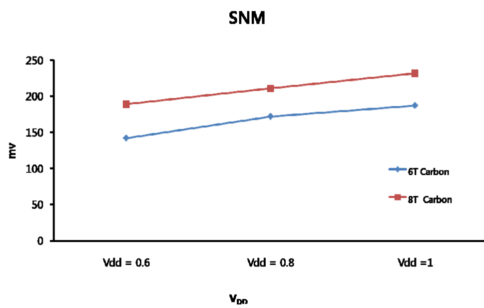

Figure 5. SNM for 6T and proposed 8T CNFET cell with V_{DD} variation

The READ access time at the cell level is determined by the time taken for the bitlines to develop a potential difference of at least 100mV.

The read time depends on the READ path's transistors' sizes. The proposed 8T SRAM cell's READ delay is almost same as the conventional cells since the transistor sizes are very similar.

For write operation, the write delay is defined as the time from the 50% activation of the WL to the time when Q_bar becomes 90% of its full swing. The write delay is approximately equal to the propagation delay of the inv2 (N2/P2) and inv1. Because the inv1 is only driving the diffusion capacitor of N5, it is desirable to reduce the input capacitance of the inv1 as much as possible to reduce the load capacitance on inv2. The proposed 8T SRAM is slightly slower than 6T SRAM in writing operation because of this reason.

Because the device performance based on intrinsic CV/I gate delay metric [12] is 6 time for nFET and 14 times for pFET higher than CMOS, the speed of the write and read operation in CNFET is about 5~ 6 times faster than CMOS and FinFET technologies.

V. CONCLUSION

This paper proposes a new 8T SRAM using CNFET. The new SRAM cell cuts off the feedback connection between the two back-to-back inverters in the SRAM cell when data is written and separates the write and read port with 8 transistors. The proposed technique saves dynamic power by reducing discharging frequency during write operation. Compared to 6T SRAM structure, the proposed 8T SRAM saves power up to 48% and obtains 56% wider SNM during read operation at the minimal cost of 2% leakage power and 3% delay increase. As the cells are more frequently accessed, the dynamic power saving is linearly increased.

This paper also compares CMOS, FinFET and CNT 6T and 8T SRAM cells using HSPICE simulations. The result demonstrates 3~7 times less dynamic power consumption, 11~17 times less leakage power consumption, 5~6 times faster read and write operations, and 1.6 wider SNM than the conventional designs.

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