

A New SRAM Cell Design Using CNTFETs

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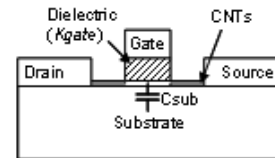
Abstract—As CMOS devices scales to the nano ranges, increased short channel effects and process variations considerably affect device and circuit designs. Novel devices are been proposed to address these problems. As a promising new transistor, the Carbon Nanotube Field Effect Transistor (CNTFET) avoids most of the fundamental limitations of the traditional CMOS devices. In this paper, the MOSFET-like CNTFET is reviewed and shown as a promising device for high-performance and low-power memory designs. A 6T SRAM cell based on CNTFET is designed and simulated to show the improvements in stability, performance, and sensitivity on process variations compared to the CMOS 6T SRAM design.

Keywords—Carbon Nanotube Field Effect Transistor; SRAM design; high performance; low power

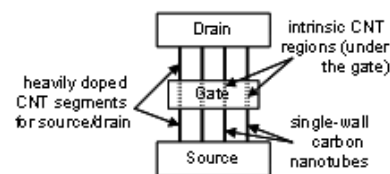
I. INTRODUCTION

As semiconductor devices and integrated circuits continue to scale down into nanometer ranges, the semiconductor industry is starting to face several difficult challenges. Scaling has resulted in increased short-channel effects, reduced gate control, exponentially rising leakage currents, severe process variations, and unmanageable power densities. The scaling of CMOS technology has progressed rapidly for three decades, but may soon come to an end because of the increased short channel effects and power-dissipation constraints. Therefore, alternative technologies to bulk silicon transistors are being explored. Ultrathin body devices such as FinFETs have received increasing attention in recent years [1]. However, it is also important to investigate new materials and devices to replace silicon in nanoscaled transistors. Carbon nanotube transistors, for example, are especially promising because their unique one-dimensional band-structure suppresses backscattering and makes near-ballistic operation a realistic possibility [2].

Carbon nanotube field effect transistors (CNTFETs) utilize semiconducting single-wall CNTs to assemble electron devices similar to MOSFETs, and fabrication of CNTFETs has been reported in recent years. With an ultralong ($\sim 1\mu\text{m}$) mean free path (MFP) for elastic scattering, a ballistic or near-ballistic transport can be obtained with an intrinsic carbon nanotube (CNT) under a low voltage bias to achieve improvements in performance [3]. Also, a CNTFET has a significantly smaller off current; therefore the power consumed when the transistor is off is greatly reduced in CNTFET designs. These properties make CNTFET one of the promising new devices to extend or complement tradition silicon technology for high performance and low power designs.



(a)



(b)

Figure 1. Schematic diagram of a carbon nanotube transistor: (a) cross section view; (b) top view [3].

For the foreseeable future, static random access memory (SRAM) will likely remain as the embedded memory technology of choice for many microprocessors and systems on chips (SoCs) due to the speed advantage and compatibility with standard logic processes. With the advent of SoC, the design of high performance and power efficient SRAM structures has become highly desirable. CNTFET's ballistic transport and the low off-current properties have made it a good candidate for high-density high-performance SRAM designs. Furthermore, the MOSFET-like CNTFET model is reported to be scalable down to 10nm channel length, a substantial improvement compared with the available MOSFET model (with a minimum channel length of 32nm). Therefore, a SRAM design with CNTFET requires a significantly less area than its CMOS counterpart.

II. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

Single-wall Carbon nanotube (or SWCNT) consists of one cylinder only, and are the most promising type for use as a transistor. An SWCNT can act as either a conductor or a semiconductor depending on the angle of the atom arrangement along the tube. This is called the *chirality* vector and is represented by the integer pair (n, m) . The diameter of the CNT can be calculated as follows [3]:

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi} \sqrt{n^2 + m^2 + nm} \quad (1)$$

where $a_0 = 0.142\text{nm}$ is the inter-atomic distance between each carbon atom and its neighbor. In this paper, the same

chirality vector of all CNTs is assumed (i.e. (19, 0)), and the diameter of the simulated CNT is 1.49 nm. Fig.1 shows the schematic diagram of a CNTFET [3]. Similar to the traditional silicon device, the CNTFET has also four terminals. A dielectric film is wrapped around a portion of an undoped semiconducting nanotube, and a metal gate surrounds the dielectric. Heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance during the on-state [4]. As the gate potential increases, the device is turned on or off electrostatically via the gate.

A. Threshold Voltage

The *threshold voltage* is defined as the voltage required to switch on a transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap that is an inverse function of the diameter [3]:

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aV_\pi}{eD_{CNT}} \quad (2)$$

Where $a = 2.49 \text{ \AA}$ is the carbon atom distance, $V_\pi = 3.033 \text{ eV}$ is the carbon π - π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter. Since D_{CNT} of a (19, 0) CNT is 1.49 nm, the threshold voltage of a CNTFET using (19, 0) CNTs as channels is 0.289 V from Equation (2). Simulation results confirmed this threshold voltage.

B. Current-Voltage Characteristics

The current-voltage (I-V) characteristics of the ballistic CNTFET are in close relation to the band structure of a CNT. The energy band of the CNT consists of many sub-bands. As the drain bias of the CNTFET increases, the drain Fermi level is depressed to traverse a sub-band minimum and the current increase occurs between the drain and source. When the drain Fermi level is below the lowest sub-band bottom, the current saturates [5].

Fig.2 shows the I-V characteristics of the ballistic CNTFET with different channel lengths, at the power supply of 0.9V and room temperature. The I-V

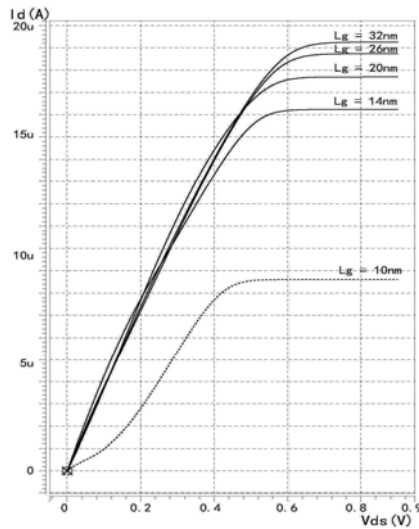


Figure 2. Current-voltage (I-V) characteristics of a ballistic CNTFET

characteristics of the CNTFET are similar to that of the MOSFET, which makes the CNTFET a good candidate for current MOSFET based VLSI designs. The current of the CNTFET can be increased by increasing the number of tubes in a CNTFET. As shown in Fig.2 the current level of the CNTFET decreases with channel length (when the channel length is very short) due to the energy quantization in the axial direction (as limited by optical phonon scattering). For high-performance, an area efficient design must be considered and a channel length of 20nm is selected as appropriate.

III. SRAM DESIGN

A. Traditional 6T SRAM Design

Fig.3 shows a six-transistor (6T) SRAM cell as the core storage element of the most register file and cache designs [6]. It consists of cross-coupled inverters as storage elements and two pass gates as a combination read/write port. With the aggressive scaling in CMOS technology, substantial problems have already been encountered when the 6T SRAM cell configuration is utilized at an ultra-low power supply. This cell shows poor stability at very small feature sizes; therefore, a SRAM design with higher stability and density is desired, and a MOSFET-like CNTFET can be a good candidate to meet for this objective.

B. Read Operation

Prior to the read operation, BL and BLB in Fig.3 are precharged to a high level. When the wordline signal WL is high, the access transistors MN1 and MN2 are turned on, and the data stored in the SRAM is read. A read-upset problem is present during the read operation, and this may change the data stored in the SRAM cell. The read-upset problem is as follows. Assume that the cell is currently storing a "1" so that q is "1" and nq is "0". When WL is high, MN1 and MN2 are on and the voltage at node nq will rise. A careful sizing ratio between MN4 and MN2 is required to limit the voltage at node nq to be lower than V_{th} so that the stored logic value will not change during the read operation. In the traditional CMOS design, the MN4/MN2 ratio should be greater than 1.28. For a CNTFET SRAM design, simulations have been performed to establish the sizing ratio of the MN4 and MN2. The gate and source of MN2 are connected to V_{dd} , and the gate of MN4 is also connected to V_{dd} as voltage on q is "1". Simulation results are shown in Fig.4. The cell ratio of the two CNTFETs is defined as the number of the tubes in two CNTFETs. The CNTFET with a channel length of 20nm has similar requirements to the CNTFET with 32nm channel length. As mentioned above, the threshold voltage of the (19, 0) CNTFET is 0.289V, so the

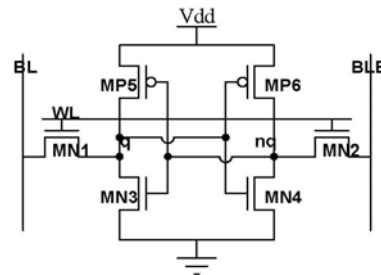


Figure 3. Traditional 6T SRAM cell

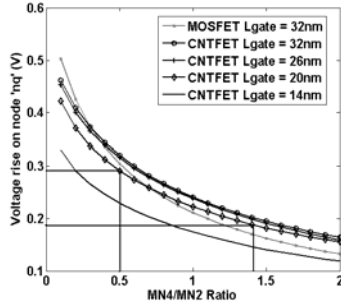


Figure 4. MN4/MN2 ratio vs. voltage rise on nq for SRAM cells

MN4/MN2 ratio should be kept greater than 0.5. However, for fair comparison, the MN4/MN2 ratio used in this paper for the CNTFET SRAM design is greater than 1.4 to control the low state voltage to be no greater than the threshold voltage of a 32nm MOSFET (which is 0.18V).

C. Write Operation

During the write operation, the wordline WL is high to allow the data on bitlines BL and BLB to be written into the SRAM cell. To guarantee that a SRAM cell can be written, the pull up transistor should not be very strong. Assume the SRAM cell is storing a “1” and the system is trying to write a “0” into the SRAM cell. The node *q* in Fig.3 is going to be low, so the pass gate MN1 must be much more conductive than the PMOS MP5. In the traditional CMOS design, the MP5/MN1 ratio should not be greater than 1.6. For a CNTFET SRAM design, simulations have been performed to establish the sizing ratio between MP5 and MN1. The bias voltage on the gate of MP5 is kept below V_{th} , and the bias voltage on the gate of MN1 is V_{dd} . Fig.5 shows the simulation results. A MP5/MN1 ratio of less than 1.6 can pull node *q* below 0.289 V, which is the threshold voltage of a CNTFET with (19, 0) nanotubes. Similarly as in the read operation, the MP5/MN1 ratio used in this paper for the CNTFET SRAM design is greater than 1 to ensure that the write voltage on node *q* is not greater than the threshold voltage of a 32nm MOSFET (i.e. 0.18V).

Therefore, for the CNTFET based SRAM cell design, the transistor size ratios among the pull up FET, the pull down FET, and the access transistors are MP5/MN1 = 0.5 and MN4/MN2 = 1.5. P-type CNTFETs with one tube are used as MP5 and MP6, while n-type CNTFETs with three tubes are used as MN3 and MN4. The number of tubes

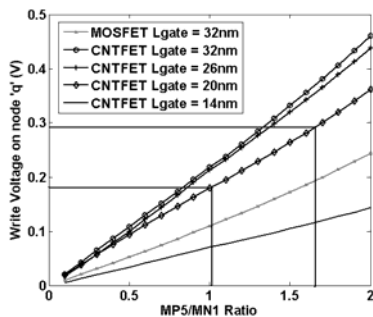


Figure 5. MP5/MN1 ratio vs. write voltage on q for SRAM cells

used for MN1 and MN2 is two. As the distance between the two adjacent tubes within the same device is 20nm and the channel length chosen in this paper is also 20nm, the dimension of pull up transistor MP5, pull down transistor MN3, and pass gate transistor MN1 are 20/20nm, 60/20nm, and 40/20nm, respectively. Compared to the smallest CMOS device at 32nm feature size, a CNTFET based SRAM cell accomplishes a significant saving in area.

IV. SIMULATION RESULTS

HSPICE simulations are performed using the Stanford CNTFET model and the Berkeley Predictive 32nm CMOS model to compare the performance of the CNTFET and CMOS SRAM cells. For the CMOS SRAM cell used for comparison, the transistor widths of MP5, MN3, and MN1 are 80nm, 160nm, and 120nm, respectively [7].

A. Read Stability

The *stability* of a SRAM cell is usually represented by the SNM (*Static Noise Margin*) that is defined as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored bit [8]. When the 6T SRAM cell configuration is utilized at a low power supply (such as 0.6V), a very low SNM is achieved. Furthermore, process variations (such as on gate length) lower the SNM of a CMOS 6T SRAM cell. For the CNTFET, only diameter variations have a significant impact on device performance while gate length variations do not significantly affect its stability. Monte Carlo simulations have been performed on CNTFET and CMOS 6T SRAM cells to investigate the impact of the gate length variations on the SNM at the power supply voltage of 0.6V and room temperature. As simulation results show in Fig.6, the CNTFET SRAM cell has a larger SNM compared to the CMOS SRAM cell due to its stronger pull up device and ballistic transport property. Also, the CNTFET SRAM design shows less sensitivity to geometry variations than the CMOS SRAM design.

B. Write Time and Access Time

Write time and access time are two important metrics for assessing the performance of a SRAM cell. In this paper, the *write time* is defined as the time required for changing the cell contents after the wordline is turned on

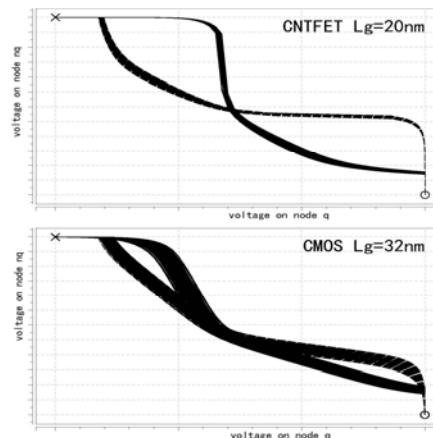


Figure 6. SNM of CNTFET and CMOS SRAM cells

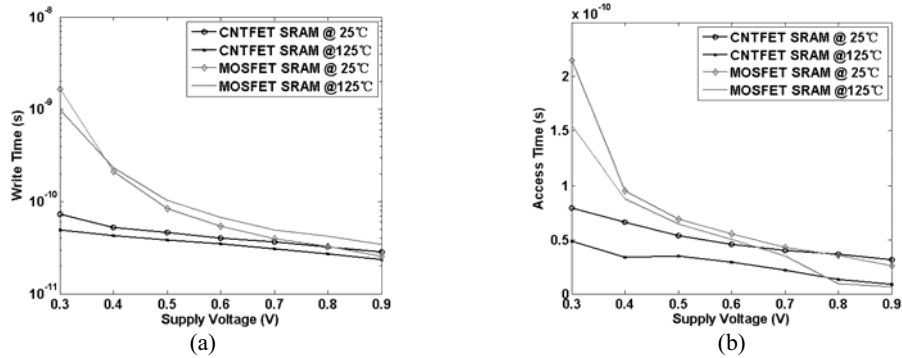


Figure 7. Write time and access time of CNTFET and CMOS SRAM cells

while the *access time* is the time required for developing 50mV bitline differential voltages after the wordline is turned on during read operation [9]. As the simulation results show in Fig.7, the write time and the access time of the CNTFET and CMOS SRAM cells are very close when the supply voltage is approximately 0.9V. However, as the power supply voltage decreases, the delay of the CMOS SRAM cell increases very fast due to the reduced electric field. In these cases, the delay of the CNTFET SRAM cell increases slowly due to the ballistic transport of the CNT. Therefore, as the power supply voltage is reduced, the CNTFET turns out to be an excellent candidate for high-performance VLSI designs.

C. Power Consumption

The CNTFET has a significantly higher on-off current ratio compared to the MOSFET in the deep sub-micron range. Therefore, the standby power of the CNTFET SRAM is very low compared to its CMOS counterpart. Simulation results show that the standby power consumption of the CNTFET SRAM cell is 1.753nW at a power supply of 0.9V and room temperature while the power consumption of the CMOS SRAM cell is 81.63nW, i.e. this is 46 times larger than the value for the CNTFET SRAM cell.

D. Write-ability

The *write-ability* of the SRAM cell provides a metric of the capability to write to the cell. The write-trip-point defines the maximum bitline voltage needed to change the cell's content. The higher the bitline voltage, the easier it is to write to the cell. Simulations have been performed to investigate the write-ability of the CNTFET and CMOS SRAM cells at 0.9V power supply and room temperature. For the CMOS SRAM cell, the write-trip-point is 0.37V while the write-trip-point of the CNTFET SRAM cell is

0.28V. Due to the symmetrical electron-hole transport in CNT, the driving strength of the pull up CNTFET is higher than its PMOS counterpart. Hence, it is harder to write a data into a CNTFET SRAM cell.

Table I summarizes the simulation results of the two SRAM cells at 0.9V power supply and room temperature.

V. CONCLUSION

This paper has investigated the use of MOSFET-like CNTFET in the conventional CMOS SRAM design. The design constraints of CMOS SRAM design (such as encountered at 32nm feature size) have been applied to CNTFETs, and the ratio of CNTFET SRAM cells has been established for best performance. Simulation results show that the CNTFET based SRAM design achieves improvements in stability, power consumption, sensitivity of process variations and performance, especially at a low power supply. Through a detailed technology assessment, this paper demonstrates that the CNTFET design is a viable candidate for memory design in the nano scales.

REFERENCES

- [1] S.A. Tawfik, Zhiyu Liu, V. Kursun, "Independent-gate and tied-gate FinFET SRAM Circuits: Design guidelines for reduced area and enhanced stability," *Microelectronics*, 2007. ICM 2007. International Conference on, pp. 171 - 174, Dec. 2007.
- [2] A. Rahman, Jing Guo, S. Datta, M.S. Lundstrom, "Theory of ballistic nanotransistors," *Electron Devices*, IEEE Transactions on, vol. 50, no. 10, pp. 1853 - 1864, Sept. 2003
- [3] Stanford University CNFET Model website, <http://nano.stanford.edu/model.php?id=23>.
- [4] J. Appenzeller, "Carbon Nanotubes for High-Performance Electronics—Progress and Prospect," *Proceedings of the IEEE* Volume 96, Issue 2, pp. 201 - 211, Feb. 2008.
- [5] K. Natori, Y. Kimura, T. Shimizu, "Characteristics of a carbon nanotube field-effect transistor analyzed as a ballistic nanowire field-effect transistor," *Journal of Applied Physics*, vol. 97, pp. 034306-1-7, 2005.
- [6] A. Chandrakasan, W.J. Bowhill, F. Fox, "Design of High-Performance Microprocessor Circuits," IEEE Press, 2000.
- [7] Berkeley Predictive Technology Model website, <http://www.eas.asu.edu/~ptm/>.
- [8] E. Seevinck, F.J. List, J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *Solid-State Circuits*, IEEE Journal of Volume 22, Issue 5, pp. 748 - 754, Oct 1987.
- [9] J. P. Kulkarni, K. Kim and K. Roy, "A 160mV Robust Schmitt Trigger based Subthreshold SRAM," *IEEE Journal of Solid State Circuits*, vol. 42, no. 10, pp. 2303 - 2313, Oct. 2007

TABLE I.
CNTFET AND CMOS SRAM CELL COMPARISON

Feature	CNTFET L _g =20nm	CMOS L _g =32nm
SNM (V)	0.227	0.085
Write time/Access time (ps)	29.75/31.59	25.62/25.79
Standby power (nW)	1.753	81.62
Write-trip-point (V)	0.28	0.37