

# An All-Digital Phase-Locked Loop with Fast Acquisition and Low Jitter

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**Abstract**— An all-digital phase-locked loop that achieves fast acquisition and low jitter was developed for high-speed clock generation. By employing a time-to-digital converter (TDC), the frequency difference is precisely measured and converted to the control word of the digital oscillator. Using this feature, the ADPLL has a faster lock-in time than previous digital phase-locked loops. The ADPLL was implemented using a 0.9V 32nm practical transistor model (PTM). The simulation results show that the proposed ADPLL achieves 5 and 10 reference cycles of frequency and phase acquisitions at 700 MHz with peak to peak jitter < 53ps.

**Keywords**—Time-to-digital converter ;DCO; ADPLL;

## I. INTRODUCTION

Phase-locked loops are widely used in many communication systems to clock and data recovery or frequency synthesis [1-4]. Cellular phones, computers, televisions, radios, and motor speed controllers are just a few examples that rely on PLLs for proper operation. With such a broad range of applications, PLLs have been extensively studied in literature.

Traditionally, a PLL is made as an analog building block including a phase frequency detector, a charge pump, a loop filter, a voltage controlled oscillator, and a frequency divider. However, integrating an analog PLL in a digital noisy system-on-chip (SoC) environment is difficult. The digital switch noise coupled with power through power supply and substrate induces considerable noise into noise-sensitive analog circuits. In addition, the analog PLL is sensitive to process parameters and must, therefore, be redesigned for each new technology. Although many approaches have been developed to improve the jitter performance, it often results in long lock in time and increasing design complexity.

With the increasing performance and decreasing cost of digital VLSI design technology, all-digital phase-locked loops (ADPLL) have become more attractive. Although ADPLL won't have the same performance as its analog counterpart, it provides a faster lock-in time and better testability, stability, and portability over difference process.. Based on the phase lock algorithm, there have been two kinds of ADPLL structures are widely used. The first order ADPLL structure separates the lock-in process into frequency acquisition and phase acquisition, which provides a theoretically infinite lock-

in range but comparatively longer lock-in time and poor jitter performance [5,6]. The second order ADPLL, as its analog counterpart, provides a better jitter performance and faster lock-in time at the cost of a limited lock-in range [7,8].

In this paper, a new ADPLL that is able to provide large lock-in range, faster lock-in time, and better jitter performance is presented. The new ADPLL also separates the lock-in process into frequency and phase acquisition. However, a time-to-digital converter (TDC) is used to measure the frequency difference precisely so that fewer reference cycles are needed in the frequency lock-in process compared to the previous blind fast or slow comparison. In the phase acquisition, a shift register is used to adjust the fine control bits of the DCO, which assures a better jitter performance and fast acquisition time. Every reference cycle consists of 2 DCO clock cycle, one for measurement and the other for updating the control bits. The new ADPLL is implemented using 32nm practical transistor model (PTM). The simulation results show 5 cycles of frequency acquisition and 10 cycles of phase acquisition at 700MHz with jitter < 53ps.

## II. ARCHITECTURE OVERVIEW

The block structure of the new ADPLL is shown in Fig. 1. There are four major building blocks, namely the TDC and algorithm block, the control, the DCO, and the edge detector with shift register. Unlike the previous ADPLL designs, the clock signals to all the logical blocks are generated from the DCO clock output. The timing sequence of clock signals is carefully designed to meet the time margin.

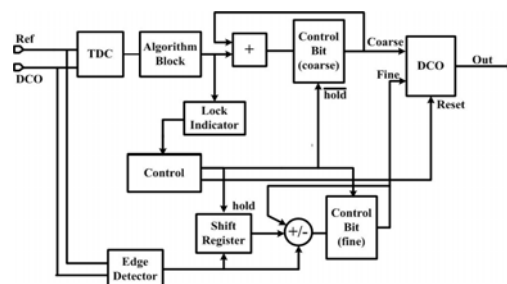


Figure 1. ADPLL block diagram

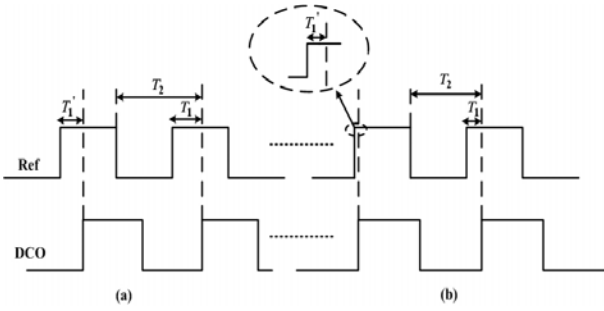


Figure 2. Principle of frequency acquisition.

Phase lock begins with frequency acquisition. In this mode, a time-to-digital converter measures the time difference between the reference clock and the DCO clock. As shown in Fig. 2a, it converts time difference into the digital word  $T_1$  and  $T_2$ , which are respectively the time difference between DCO clock's rising edge and the reference clock's rising and falling edges. As a result, the frequency difference can be defined as follows:

$$\Delta T = (T_1 - T_1') + (N - 2)T / 2 \quad (1)$$

$$T = 2(T_2 - T_1) \quad (2)$$

$N$  is the reference clock's low-to-high or high-to-low transition number during one DCO clock period from a 4-bit counter.  $T_1'$  is the stored value of  $T_1$  in the previous DCO period.

Compared to other frequency acquisition approaches, the DCO needn't to be reset at the beginning of every reference cycle for the initial phase alignment, which reduces the design complexity. However, as shown in Fig. 2b, due to the non-zero setup time, the last transition of reference clock may be neglected if the time difference  $T_1'$  is smaller than the register's setup time. This has to be taken into consideration in the design of TDC and will be discussed in counter design.

The corresponding coarse control bits are then generated by the algorithm block and applied to the DCO. Since the DCO has a good linearity, this acquisition approach takes fewer reference cycles compared to previous blind fast or slow comparison. When the frequency is locked, the control bits are stored in the coarse bit register and the lock indicator triggered the control to switch from the frequency acquisition into the phase acquisition.

In the phase acquisition mode, the DCO is first reset by the reference clock in order for the initial phase alignment. The edge detector generates an "ahead" or "behind" signal based on the rising edges of the reference clock and DCO clock. The output of the shift register is shifted to the left by 1 bit every cycle. The fine control bits are then added or subtracted by the output from shift register based on the generated signal. When the phase polarity is changed, the shift register and the fine bits are reset to the initial value and the phase acquisition is completed. The edge detector keeps comparing the phase difference and updating the fine control bits in order to maintain the phase lock. The fine resolution of the DCO as well as the bit shift strategy provides a fast phase lock-in time and better jitter performance.

A. Digitally-Controlled Ring Oscillator

The digitally controlled oscillator is the core part of ADPLL. The ADPLL controls the DCO frequency by arithmetically increasing or decreasing the DCO control word. An Schmitt trigger inverter based ring oscillator with 12 bits of tuning codes is shown in Figure 3. The DCO consists of two coarse cells and a fine cell. The coarse cells have tuning codes of 2 bits with PMOS array or NMOS array in form of thermometer code, which could provide a better duty cycle performance and linearity. Three stage constant delay chains are used to increase the operating range. The fine cell has tuning codes of 6 bits by only NMOS array in the form of thermometer code as shown in Fig. 4c. The thermometer code could minimize the jitters. Since they are grouped per 2 bits, the conversion circuit size is also minimized. Moreover, the Schmitt trigger based DCO circuit provides the same tuning range with smaller capacitance loading, which is beneficial for power consumption reduction. It has a good robustness to process, voltage, and temperature variations and better linearity comparing to the conventional design.

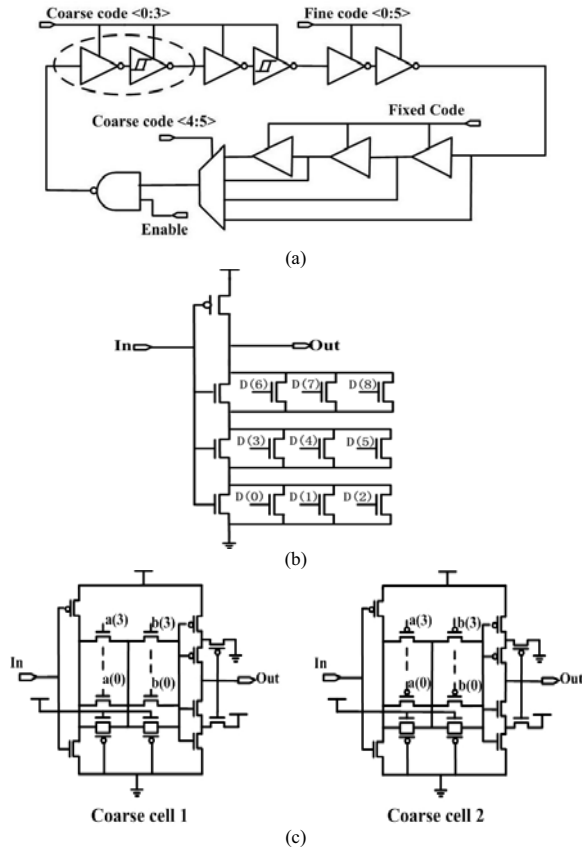


Figure 3. Digitally controlled ring oscillator. (a) DCO block diagram, (b) Fine delay cell, (c) Coarse delay cell.

**B. Time-to-digital converter**

The TDC used in this paper is composed of two parts: an integer counter that counts the reference clock edges within one DCO clock period and a fractional counter that quantizes the residual phase difference.

The block diagram of the fractional TDC structure is shown in Fig. 4. It consists of 16 delay blocks and two decoders. The resolution of the TDC is the delay of a single buffer, which minimizes the delay mismatch compared to the delay of a single inverter. The reference clock wave propagates through a chain of  $8 \times 16$  delay elements whose outputs are sampled by  $8 \times 16$  flip-flops at the rising edge of each DCO clock.

The decoding process is shown in Fig.5. The 16 bits output of the delay block are decoded into the higher 4 bits of  $T_1$  &  $T_2$ . At the same time, the 8 bits output of each delay block is also decoded into a series of lower 3 bits of  $T_1$  &  $T_2$ . Based on the output of decoder1, the proper set of  $T_1$  (0:2) &  $T_2$  (0:2) is selected. As is shown in Fig. 5, the transition takes place in the 2<sup>nd</sup> and 6<sup>th</sup> blocks. As a result, the decoded output of those two blocks is select as the lower 3 bits of  $T_1$  and  $T_2$ . The separation of the decoder into two parts has greatly reduced the design complexity.

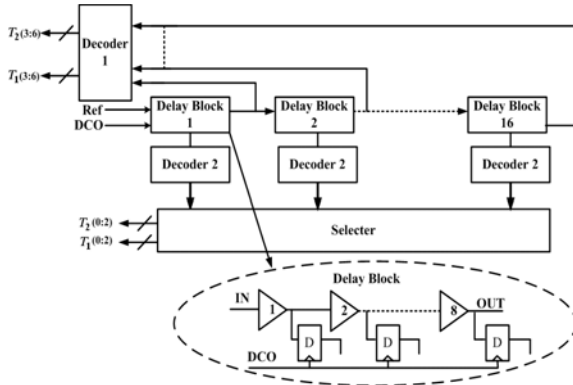


Figure 4. Block diagram of fractional TDC structure

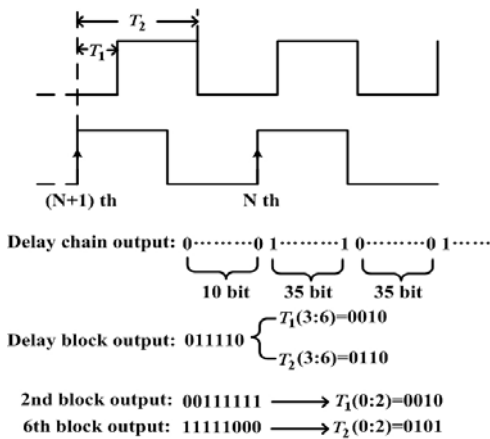


Figure 5. Decoding process of the TDC

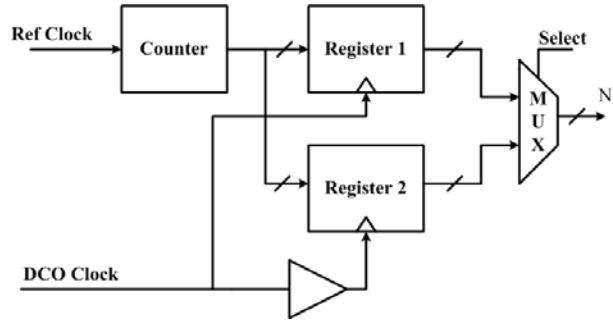


Figure 6. Block diagram of integer counter

As is mentioned above, the non-ideal setup time may result in an incorrect transition number  $N$  if  $T_1$  is less than the setup time. The proposed integer counter design that is designed to solve this problem is shown in Fig 5. By use of a delay buffer in the clock path, register2 is able to detect the closest rising edge of the reference clock while register1 can't. The select signal is the XOR output of the first delay block. When the rising edge of DCO clock is slightly behind the edge of reference clock, the transition will take place in the first delay block. As a result, the XOR output of this delay block will generate a logic high signal and the output of register2 will be selected. Apparently, when DCO clock edge is slight ahead or  $T_1$  is large enough, the XOR output of delay block 1 is logic low and the output of register1 is selected. This illuminates another possible error that register2 may stored value of  $N+1$  instead of  $N$  when DCO clock edge is slight ahead of reference clock edge.

**C. Algorithm Block**

The algorithm block takes the output of  $T_1$ ,  $T_2$ , and  $N$  from TDC and generates the corresponding adjusting digital control word as shown in Fig 5. The comparator first compares the two input digital word and sets the larger value as  $T_2$  while the other as  $T_1$ . In order to calculate the difference between  $T_1$  and its previous value  $T'_1$ , an extra register is required. The clock signal of this register is delay by a single buffer, so that in every cycle when the difference is calculated, the current value is stored and will be used as  $T'_1$  in the next cycle. This value together with the output from the multiplier as  $(N-2)T/2$  generates the coarse bits applied to the DCO.

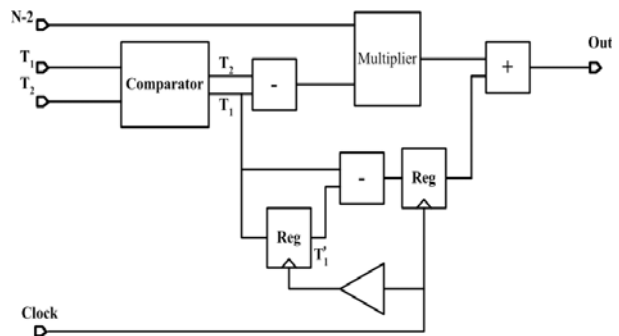


Figure 7. Block diagram of algorithm unit

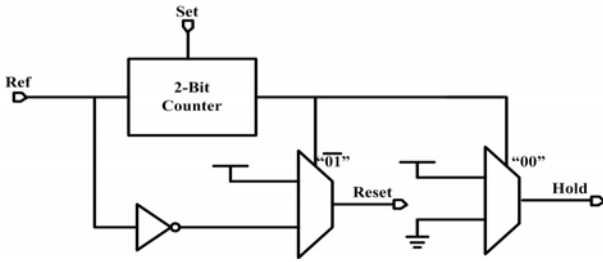


Figure 8. Block diagram of control unit

#### D. CONTROL BLOCK

Fig. 8 shows the block diagram of the control unit used in the ADPLL design. It consists of a 2-bit counter and two MUX blocks. When the frequency acquisition is completed, the reference clock is counted by the counter. As the output switches to "01" output, the DCO is reset by the reference clock. At the same time, the hold signal sets the coarse bits unchanged during the phase acquisition and the shift register begins to shift by every reference clock. The counter stops counting at "11" in order to avoid unexpected reset of the DCO again.

#### IV. SIMULATION RESULTS

The proposed APDLL structure is designed and simulated using 32nm CMOS Predictive Transistor Model. The resolution of the TDC, which is the delay of a single buffer used in the delay chain, is 20ps. The 12 bit digitally controlled oscillator has a coarse resolution close to 10ps and fine resolution close to 1ps with a tuning range from 570 MHz to 800 MHz.

The coarse and fine control word response with reference clock frequency @ 700MHz is shown in Fig. 9. It takes 5

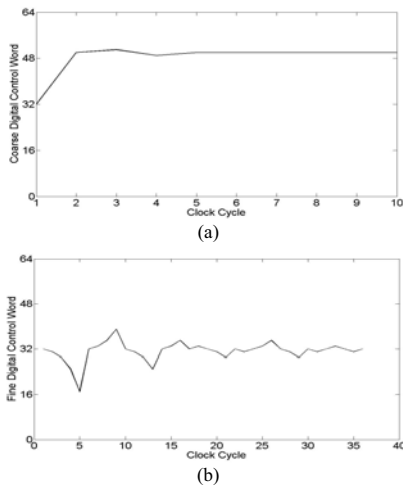


Figure 9. Measured digital control word response of the ADPLL. (a) Coarse control word response. (b) Fine control word response.

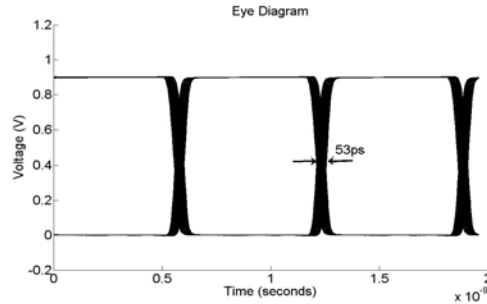


Figure 10. Output clock jitter (DCO @ 700MHz).

clock cycles for the frequency acquisition and 10 cycles for the phase acquisition. Fig. 10 depicts output clock jitter at 700MHz relative to the reference clock. From the eye diagram the peak-to-peak jitter is 53ps. To enable minimum peak-to-peak jitter, a better resolution of the TDC is necessary.

#### V. CONCLUSION

A new ADPLL structure with fast acquisition time and low peak-to-peak jitter is presented. This ADPLL is designed and implemented using 32nm CMOS Predictive Transistor Model with a frequency range of 570 MHz to 800 MHz at 0.9-v supply voltage. Instead of blind fast or slow comparison, the TDC measures the exact frequency difference. Due to the good linearity of the frequency response of DCO, the lock-in time is greatly reduced. It takes 5 cycles for frequency acquisition and 10 cycles for phase acquisition at 700 MHz with a peak-to-peak jitter less than 53ps. It would seem to be useful in various clock control systems for all-digital implementations.

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