

A 11-Transistor Nanoscale CMOS Memory Cell for Hardening to Soft Errors

Sheng Lin, Yong-Bin Kim, and Fabrizio Lombardi

Abstract—This paper proposes a new hardening design for an 11-transistors (11T) CMOS memory cell at 32 nm feature size. The proposed hardened memory cell overcomes the problems associated with the previous design by utilizing novel access and refreshing mechanisms. Simulation shows that the data stored in the proposed hardened memory cell does not change even for a transient pulse of more than twice the charge than a conventional memory cell. Moreover it achieves 55% reduction in power delay product compared to the DICE cell (with 12 transistors) providing a significant improvement in soft error tolerance. Simulation results are provided using the predictive technology file for 32 nm feature size in CMOS.

Index Terms—Memory design, nanotechnology, radiation hardening.

I. INTRODUCTION

The tremendous scaling of CMOS technology necessitates reliable operation for many circuit designs. Due to the lower V_{dd} and the smaller node capacitance, the amount of charge stored on a circuit node is becoming increasingly smaller, thus making circuits more susceptible to spurious voltage variations caused by *externally induced phenomena* such as cosmic ray neutrons and α -particles [1]. These energy particles travel through the silicon bulk and create minority carriers that may be collected by the source/drain diffusion, thus altering their voltage value [2]. This is particularly deleterious for storage cells such as memories and latches because data integrity is affected [13]. Moreover, a single event transient may affect multiple nodes in a circuit through charge sharing. However, in this paper, we focus on hardening a cell design against a single-node strike. The occurrence of this type of event may result in transient faults (TFs) as widely reported in the technical literatures. If a TF is latched by a sampling element (latch), then this may result in a so-called soft error (SE) [3].

Recently, new techniques have been advocated for soft error tolerance. Among them, *hardening* has been proposed for low-cost design to tolerate SEs and TFs in memories and latches [4]–[8]. Hardened design approaches can be classified into two broad categories [8]. In the first approach, the storage cells are designed to be *insensitive* to TFs, so independent of both the size of the cell's transistors and the capacitance of the cell's nodes. These approaches have the advantage of *technology independence*, but they may incur in a high design overhead due to the additional circuitry. In the second category, hardening is achieved in the design by increasing the capacitance of some nodes, or the strength of the transistors through a novel design. Such an approach must be scaled with the feature size of the employed technology and may result in unwanted penalties with respect to performance (i.e., an increase in delay) and power dissipation.

An example of the approach in the first category has been reported in [4] and is commonly known as DICE. The DICE cell uses twice the number of transistors of the standard storage cell (i.e., 12T versus 6T) to achieve tolerance against TFs affecting any single node. However, its design does not require an increase in the size of the transistors or the

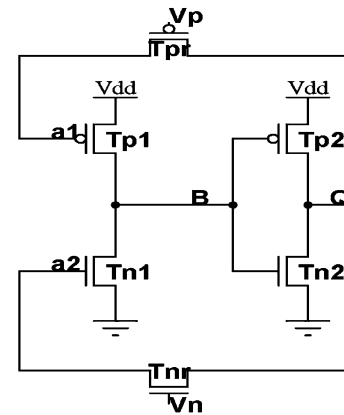


Fig. 1. Hardening approach proposed in [8].

capacitance of some nodes. In the DICE cell, the node that is affected by TFs can be driven back to its previous state by other transistors. For the second category of hardened designs, approaches using Schmitt triggers and/or innovative feedback arrangements are utilized to protect storage cells (such as latches) from TFs [7], [9].

II. REVIEW AND ISSUES

Fig. 1 shows the basic cell for the hardening approach proposed in [8]. This belongs to the first category of hardened designs described previously in Section I. Three basic principles are applicable to the design of this cell: 1) the feedback loop of the cell is blocked to keep the transient pulse from propagating along the loop; 2) the gates of the nMOS and pMOS transistors of the inverters are separated to harden those nodes left unprotected by the first principle; and 3) the regeneration principle should be introduced to avoid the loss of stored information.

A traditional storage cell configuration uses two back to back inverters, producing a positive feedback loop to make a bistable circuit. For the radiation hardened latch design in Fig. 1, the feedback loop is blocked to prevent the transient pulse from propagating along the loop. As shown in Fig. 1, transistors Tpr and Tnr are used to block the transient pulse affecting node B or node Q. Therefore, the transient pulse cannot be propagated to nodes a1 and a2, which are the gates of transistors Tp1 and Tn1. Furthermore, the gates of transistors Tp1 and Tn1 are separated to harden nodes a1 and a2. As ionizing particles striking the nMOS transistor produce only negative current pulses and ionizing particles striking a pMOS transistor produce only positive current pulses, a particle striking node a2 can turn transistor Tn1 off, but it can never turn it on. Similarly, a particle striking node a1 can turn transistor Tp1 off, but it can never turn it on. Turning Tp1 or Tn1 off can only bring the output of the first inverter to the high impedance state, thus leaving unaffected the previous state at node B. Therefore, TFs on nodes a1 and a2 are also blocked. The gate control voltages Vp and Vn are applied to the transistors Tpr and Tnr to restore the values by the leakage current on nodes a1 and a2 as proposed in [8]. To increase the leakage current of Tpr and Tnr, the voltages $V_p = V_{dd} - d$ and $V_n = d$ (where d is equal to a few tenth of V_{dd}) are applied to the gates of Tpr and Tnr, respectively [8]. However, the leakage current also decreases significantly as the drain source voltage decreases. Assume the voltage at a1 and a2 is V_{dd} and a negative strike occurs on node a2. Simulation by HSPICE shows that for 0.9 V power supply the node a2 can be promptly restored to 0.2 V due to the large voltage difference between source and drain. However, the voltage at node a2 increases slowly after the voltage reaches 0.2 V due to the reduced drain source

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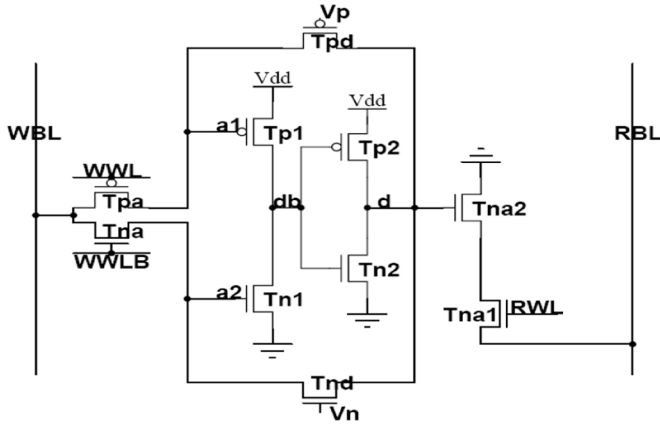


Fig. 2. Hardened memory cell proposed in [8].

voltage difference. Therefore, the voltage at node a2 can be only driven to approximately 0.25 V instead of 0.9 V. Similarly, the voltage for “0” data at node a1 can be only driven back to approximately 0.65 V (high state) if a positive strike occurs on node a1 and (storing a logic “0”). Therefore, the dc voltages at Vp and Vn are unable to restore the node voltage after the nodes are struck by a transient pulse. To fully restore the voltages at nodes a1 and a2, the periodic signals $V_p = R_n'$ and $V_n = R_n$ have been also utilized as proposed in [8]. The periodic signal Rn is “0” for most of the time and it takes the value of “1” for a short time to restore the value of node a2. The signal Rn' is used in a similar fashion.

As shown in Fig. 2, a hardened memory cell has also been proposed in [8] by implementing the hardened memory cell structure of Fig. 1. However, this memory cell suffers from two problems. The first problem is that nodes a1 and a2 could easily lose their state due to the leakage current from write bitline WBL, since the feedback loop from node d to a1 and a2 is cut off by the two pass transistors, Tpd and Tnd. Then, the high leakage current from a2 to WBL or from WBL to a2 can possibly change the state of the memory cell. For the memory cell shown in Fig. 2, after writing a “0” into the memory cell, the voltage at node a2 is 0. If WBL goes back to “1” and the access transistors are off, a high leakage current is present on the access transistors Tpa and Tna, and the voltage on node a2 increases. At this time, a positive strike may happen at node a1 to drive node db to a high impedance state. A voltage rise on node a2 will change the data stored in the memory cell.

The second problem of this memory cell is the signal distribution network of Vp and Vn since $V_p = V_{dd} - d$ and $V_n = d$ (where d can be equal to a few tenth of V_{dd}) or the periodic signals $V_p = R_n'$ and $V_n = R_n$, must be applied to every single memory cell as mentioned before. The signal generation and distribution are very costly, and they result in an additional load to the overall memory, thus degrading its performance.

For hardening design, the scheme shown in Fig. 1 can be still utilized even for a different memory cell configuration to overcome the problems described previously. This is described in more detail in Section III.

III. PROPOSED HARDENED MEMORY CELL

Based on our preliminary work [14], a new hardened memory cell is proposed in this paper to overcome the problems described previously. Its design is shown in Fig. 3 and solves the problems described previously for the design of [8].

The proposed hardened cell is derived and improved from the fast hardened latch in [8] by removing the switches in the feedback loop. As mentioned in Section III, the hardened memory proposed in [8] has

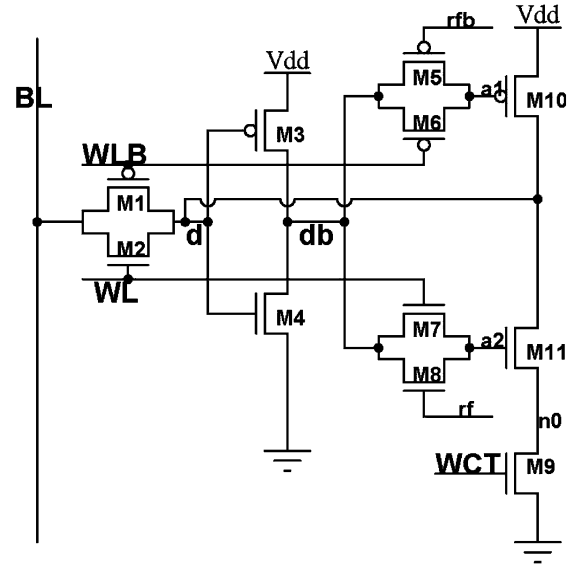


Fig. 3. Proposed hardening memory cell.

two problems which affect the correct operation of the cell. The feedback configuration in the fast hardened latch in [8] is found to be better suitable for hardened memory cell than the feedback in the hardened memory in [8]. The basic storage element used in the proposed hardened memory cell relies on the hardening scheme [8] of Fig. 1. In the hardened memory cell of Fig. 3, the feedback loop in the memory cell is cut off by the transistors M5, M6, M7, and M8, i.e., a transient pulse cannot be propagated along this loop back to its starting point. At the unprotected nodes a1 and a2, the gates of the pMOS and nMOS transistors are separated from the hardened nodes a1 and a2. Signal regeneration at a1 and a2 is controlled by the transistor M5 and M8, and will be described in more detail below.

In the proposed hardened cell, the access pass gates (M1 and M2) are connected to node d instead of nodes a1 and a2 to prevent the high leakage current from BL to change the data stored in the memory cell. For the memory cell in Fig. 2, the leakage current from WBL can easily change the data. In the proposed memory cell of Fig. 3, however, the access transistors are connected to node d, thus not allowing nodes a1 and a2 to be affected by the leakage current on BL. In this case, a TF on a1 or a2 will not change the data stored in the memory cell. A nMOS write control transistor is added to the proposed memory cell for the write operation. As discussed in [11], a single ended SRAM cell operates correctly when writing “0” as data, but it may encounter problems when writing a “1”. Therefore, a write control transistor is added between M11 and ground and the WCT signal is generated by the write select signal [11]. When the column is selected, the WCT signal is low and the pull down transistor does not affect the write operation. As for the unselected columns, the WCT signal is high to maintain the latch function. With the new write control transistor, the proposed hardened memory cell consists of eleven transistors, which is one transistor less than the DICE configuration.

The refresh signals rf and rfb are connected to the gates of M8 and M5 to regenerate the states at nodes a1 and a2. As described in Section II, the voltages $V_p = V_{dd} - d$ and $V_n = d$ on transistors Tpd and Tnd of Fig. 2 are unable to restore the voltages at nodes a1 and a2, and this also causes a high standby power consumption for the memory cell. Therefore, the periodic refresh signals $V_p = R_n'$ and $V_n = R_n$ must be used to regenerate the states on nodes a1 and a2. As the read wordline is always connected to the memory cell, then these two signals can be used to control the pass gate transistors to

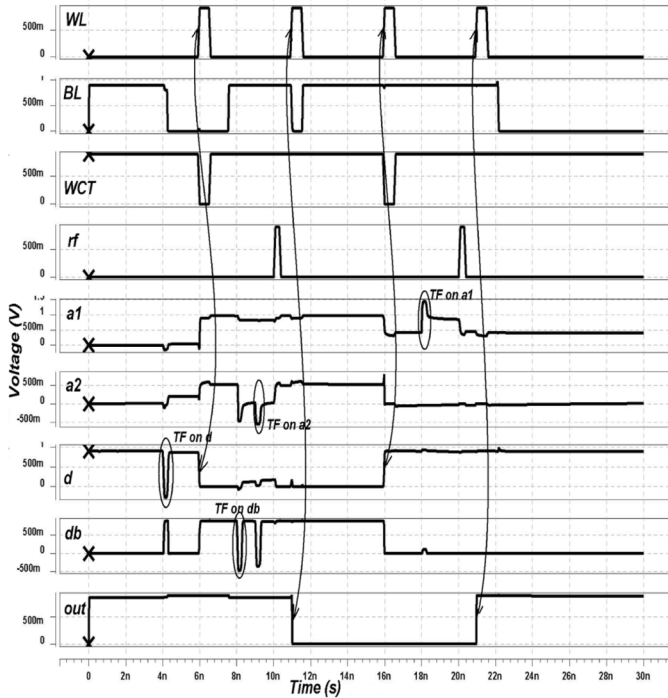


Fig. 4. Simulation results for the proposed hardened memory cell when transient faults occur on the nodes of the cells.

block the feedback loop. As shown in Fig. 4, when WL is high and WLB is low, the transistors M7 and M6 are on, and the cell acts as a normal memory element. When WL is low and WLB is high, the transistors M7 and M6 are off, and the feedback loop is cut off. The refresh signals, rf and rfb, are generated by the read select signal. When a column is selected for read, the rf and rfb signals are generated at each column by a complementary pulse generator to refresh the data at the nodes a1 and a2 and ensure that the correct signal is read by the bitline. The memory design proposed in this paper successfully addresses both problems described previously for the cell of [8].

As the access transistors M1 and M2 are used for both (read and write) operations, the refresh transistors M5 and M8 and the refresh signals rf and rfb ensure a correct read operation. As shown in Fig. 4, when the memory stores “0” as data, a2 is “1”. Consider the scenario in which a TF occurs on node a2 prior to the read operation thus driving node a2 to a “0” state. As discussed in Section II, the state of node a2 needs to be restored. Otherwise during the read operation, M6 and M7 are on. The “0” state on node a2 will change the data on nodes db and a1 to the “0” state, resulting in data change on d to a “1” (its correct value is “0”). If there is no refresh prior to the read operation, an error occurs during the read operation if a TF strikes on node a2. Therefore, the refresh signals rf and rfb generated by the read select signal are connected to M8 and M5 to refresh the memory cell before the read operation. The refresh operation is performed by a pulse generator circuit locally sited at every column to provide the refresh signal; once the column is accessed for a read operation, the refresh signal is generated to refresh the memory cells. Simulation results using HSPICE show that adding the refresh transistors and the refresh circuit to the proposed hardened cell will only increase the average power consumption by 0.8% per single cell during the read access operation. The power dissipation of this pulse generator circuit (consisting of a dozen transistors) is very small and therefore negligible compared to the entire memory array. It is important to note that the read column select signal

for generating rf and rfb must arrive earlier than the read wordline. This condition is always valid in the proposed design.

IV. EVALUATION

In this section, different figures of merit as related to critical charge, power dissipation, and delay are assessed to compare the proposed memory cell with other schemes found in the technical literature.

A. Critical Charge

A normal (unhardened) back to back inverter memory at 32 nm feature size has been simulated at 0.9 V power supply and room temperature. Under these conditions, the critical charge Q_{crit} of a normal (6T) memory cell is 3.96 fC. Simulations have been performed on the proposed hardened memory cell using same sized transistors. A 10 fC charge (i.e., a value more than twice the Q_{crit} for a normal 6T memory) is applied to nodes d, db, a1, and a2 (note that only a positive strike on node a1 and only a negative strike on node a2 can occur) as shown in Fig. 4. Since the feedback loop is blocked, a TF on node d or db will not propagate to its starting point, so the stored data will be unaffected. If there is a strike on node a1 or a2, the output of the first inverter will be at the high impedance state and the data on nodes d and db can not be changed. When the periodic refresh signal arrives, the voltage on node a1 or a2 is then restored to its previous state. Simulation results show that the data stored in the proposed hardened memory cell does not change even when a transient pulse with a charge higher than 10 fC is applied to the nodes. Same as the DICE cell, the proposed design presents complete immunity for any transient on a single node regardless of the strength of the transient fault. Therefore, this design is hardened and excellent tolerance to soft errors is accomplished.

B. Area, Power, and Delay

The proposed hardened memory has eleven transistors compared to a conventional memory that has only six transistors (6T). The additional transistors consume more power depending on the choice of technology. In the proposed hardened memory cell, the write operation can be slowed down due the transistors for blocking the feedback loop. In the proposed memory cell design of Fig. 3, the size of the access transistors is therefore increased to improve performance. Fig. 5 shows the write delay of the proposed 11T hardened memory cell, the DICE cell (12T), and the 6T conventional memory cell. The width of the access transistors M1 and M2 in Fig. 3 is twice the width of the access transistors of the DICE cell and a 6T conventional memory cell. As shown in Fig. 5, both the write “0” and the write “1” delays of the proposed 11T hardened memory cell are the fastest. However, this results in an increase of power consumption. Therefore, the power-delay product of the hardened memory cells (as an important metric for digital CMOS circuits) must be also investigated for the different memory cells. Table I shows the number of transistors, the total transistor width, and the area of the conventional 6T memory cell, the proposed 11T hardened memory cell, and the 12T hardened DICE memory cell at 32 nm CMOS technology (using the predictive model data of [12] and MOSIS deep submicrometer rules [15]). Layouts of the DICE cell and the proposed 11T cell are shown in Fig. 6. For fair comparison, the total width of the 11 transistors of the proposed cell is set to be the same as the DICE configuration (with 12 transistors). As shown in Table I, the area of the 11T cell is slightly smaller than the DICE cell; the hardened memory cell of [8] is also included in this comparison. For the entire memory array, a pulse generator circuit is needed for each column; the complexity of this circuit is very small (nearly a dozen transistors) compared to the memory array. Two routing paths (in parallel with the bitline) are needed for the rf and rfb signals of Fig. 4. However, as there

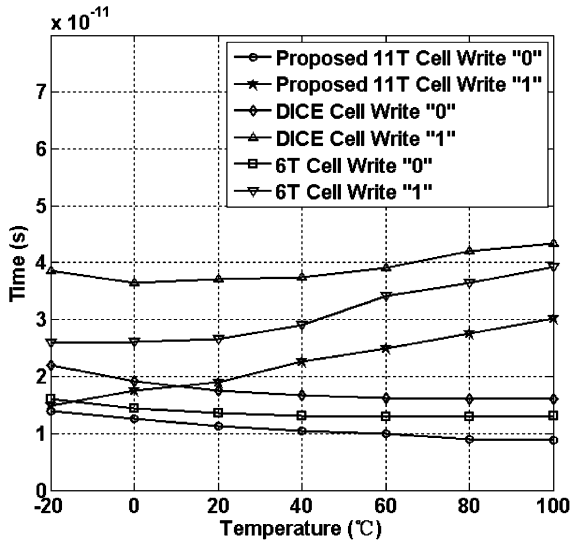


Fig. 5. Write delay of memory cells at different temperatures.

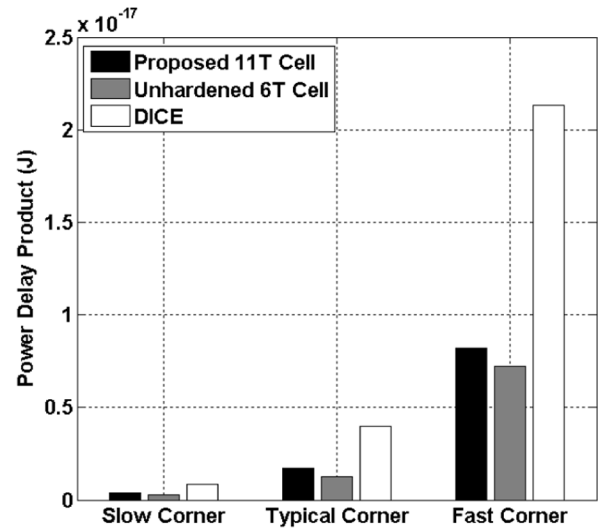


Fig. 7. PDP of memory cells at different process corners.

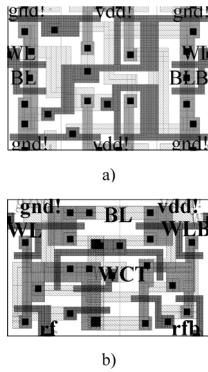


Fig. 6. Layout of (a) DICE cell and (b) proposed 11T cell.

TABLE I
GEOMETRIC PARAMETER OF MEMORY CELLS

Memory Cell Type	Number of transistors	Total transistor width	Cell area
Unhardened 6T memory cell	6	720 nm	0.2134 μm^2
Proposed hardened memory cell	11	1440 nm	0.3764 μm^2
DICE memory cell	12	1440 nm	0.3864 μm^2
Hardened memory in [8]	10	1160 nm	0.3520 μm^2

are ample of routing resources in parallel with the bitline, the two additional rf and rfb signals will not significantly increase the area of the overall memory array.

HSPICE simulation has been performed at a 0.9 V power supply and room temperature using the Berkeley Predictive Technology Model at 32 nm [12]. Fig. 7 shows the simulation results for the standby power and the write delay product of the two hardened memory cells and the conventional 6T memory cell at different process corners. For the proposed 11T hardened memory cell, the worst case standby power is measured, i.e., when BL is high and the memory cell stores a “0”. For the write delay, the average delay of the write “1” and “0” operations is used for the power delay product (PDP). The power delay product of

the proposed 11T hardened memory cell is 38% higher than the power delay product of the 6T (unhardened) memory cell due to the additional transistors. The DICE cell has 218% increases in the power delay product with respect to the 6T memory cell due to the large leakage current from the four access transistors. Therefore, by combining the delay improvement and power overhead, the proposed 11T hardened memory cell has a 55% reduction in power delay product compared with the DICE cell. The HSPICE simulation results (plotted in Fig. 7) confirm the reduction in power delay product at different process corners.

C. Process Variation

As CMOS technology scales down into the nano ranges, process variations are a serious concern due to uncertainty in device and interconnect characteristics. Fabrication process variations negatively impact the speed, stability, and power consumption of traditional SRAM designs. Using Monte Carlo and HSPICE, the soft-error tolerance of the proposed hardened memory cell is evaluated in the presence of process variations in the channel length and the threshold voltage of the transistors.

In the Monte Carlo simulation, transient faults on internal nodes of the memory cell follow a uniform distribution in the Monte Carlo simulation. In the presence of random variation, the data stored in the memory cell will not change unless the memory cell is ready to write (this is a problem common to all memory cells). Monte Carlo simulation results have nevertheless confirmed the excellent soft error hardening capabilities of the proposed memory cell in the presence of process variations in its design.

V. CONCLUSION

Previous hardened designs like DICE cell incur in an increase of power consumption and delay; yet another hardened design [8] suffers from two problems that result in failure of its operation. In this paper a novel cell configuration is derived from the hardened latch in [8]. In order to solve those problems in [8], the new configuration has been proposed, analyzed, and simulated using the predictive technology model [12] for soft error hardening at 32 nm technology node. A write control transistor [11] is then added to the proposed memory cell for fast writing “1” state into the cell. The proposed radiation hardened memory cell relies on a novel access mechanism along with two refresh transistors; the proposed cell requires 11 transistors, i.e., one

less than the DICE configuration (hence incurring in a smaller overhead in layout and area). Moreover, the proposed cell has been simulated, and assessed for critical charge, power consumption, and delay to overcome the problems encountered in [8]. Using HSPICE, simulation results have confirmed that the proposed memory cell accomplishes the highest soft error tolerance through hardening (it has more than twice the critical charge than the 6T unhardened configuration) and an impressive power-delay product compared with the other hardened design commonly referred to as DICE. Therefore, the proposed hardened cell demonstrates superior resistance to soft errors and excellent performance metric as required for high performance memory design. Monte Carlo simulation has confirmed that the soft error hardening of the proposed memory cell is accomplished also in the presence of process variations.

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Efficient Package Pin-Out Planning With System Interconnects Optimization for Package-Board Codesign

Ren-Jie Lee and Hung-Ming Chen

Abstract—In conventional package design, engineers designate the ball grid array (BGA) pin-out manually, this always postpones the time-to-market (TTM) of products due to the turn-around between package and design houses. Recent papers propose a method of automatically generating the pin-out and taking signal integrity (SI), power delivery integrity (PI), and routability (RA) into account simultaneously by pin-block design and floorplanning, thus dramatically speeding up the developing time. However, this approach ignores the considerations of shorter path length and equilength/length matching in routing printed circuit board (PCB) trace and pin-out assignment for high-speed interface IP designs, such as USB and PCI Express. Since these features are the most important performance metrics during chip-package-board codesign, in this paper we propose the ideas to optimize the system interconnects during package pin-out design. These ideas keep the same minimized package size as aforementioned recent work and ensure that SI, PI, and RA can still be considered with significant reduction in design cost. It is achieved by relaxing the restriction of pin-block side and order on the package, usually specified by package designers. The experimental results on industrial chipset design cases show that the average improvement of our pin-block planner is over 40% when comparing the design cost with the previous work, among which we have one case accommodated over a thousand pins. Our ideas also work for any kind of pin-block or pin-group configurations.

Index Terms—Pin-out planning, package-board codesign, system interconnects optimization.

I. INTRODUCTION

As silicon technology scales, more and more circuits could be integrated into a single chip. The amounts of input/output (I/O) signals increase dramatically per unit area. This trend significantly arises the complication in package designs and signal interaction between package and board [1], [2]. The complete package-board codesign methodology should preserve the signal integrity (SI), power delivery integrity (PI), and routability (RA) of high-speed signals routing from package to printed circuit board (PCB) while optimizing the package size. One codesign approach regarding the automation of pin-out designation was published very recently in [3]. In this method, an experienced engineer has to determine the pin configuration chart based on the location of PCB components. Next, the proposed signal-pin patterns are selected for pin-blocks construction in package design where SI, PI, and RA have been accounted for after placing pin-blocks. It also proposes a near optimal approach to minimizing package size by mathematical (linear) programming. Finally, this methodology obtains the final pin assignment by applying a rather intuitive floorplanner which bends the pin-blocks located in the excess areas and fills them into the adjacent empty areas.

However, the cost function in [3] only considers the package size, this work exposes some weaknesses, shown as follows.

- The method in [3] ignores the connections between the ball grid array (BGA) pins and high-speed interface IP designs, which are

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