THREE DIMENSIONAL DIELECTROPHORETIC ASSEMBLY OF SINGLE-WALLED CARBON NANOTUBES FOR INTEGRATED CIRCUIT INTERCONNECTS

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Abstract— **In this paper, we report a novel technological approach for three dimensional (3D) assembly of single-walled carbon nanotubes (SWNTs) using dielectrophoresis (DEP). The two terminal resistance of the assembled SWNTs is ~ 545 Ohms. Encapsulation of the 3D structure with a thin layer of parylene-C protects it from the environment and keeps it intact. This directed assembly procedure is versatile, inexpensive, and achieved at room temperature. By utilizing a self-aligned three mask process, we demonstrate a 3D assembly/encapsulation method utilizing conductive SWNTs as the metallization material, parylene-C as the inter-level dielectric and the encapsulation layer. This technology is also applicable for vertical assembly of other conductive nanostructures and will enable 3D research in nanotechnology.**

1. INTRODUCTION

The historical Moore's law continues to be outpaced by the progress in silicon technology. With the limits to device scaling being anticipated in the near future, there is an increasing need to develop molecular scale devices that compete or even replace the existing technology. Nanostructures such as carbon nanotubes (CNT) may serve as potential building blocks for next generation of electronic devices. Since their discovery in 1991 [1], a lot of effort has focused on them due to their excellent electrical, mechanical and thermal properties.

Carbon nanotubes (CNTs) are formed from crystalline sheets of atoms that have been rolled up and bonded to form a closed cylinder. The earliest nanotubes were made from pure carbon by folding graphite layers; however nanotubes need not be made only from pure carbon. Any compound with the property for forming graphite like sheets is a potential nanotube material. Nanotubes can be metallic or semiconducting depending on the helicity of the arrangement of the graphite rings in their walls and their diameter [2]. In the case of semiconducting nanotubes, the details of rolling and the diameter also determine the band gap energy (E_g varies inversely with diameter [2] [3]) and hence the electronic properties of the nanotube. The high current carrying capacity of the metallic carbon nanotubes make them an ideal candidate for future interconnects [4-7] while the high aspect ratio and partially conducting behavior of semiconducting carbon nanotubes have proved to be useful for making field-effect transistors [8], logic devices [3,9,10] sensors [11], and field emitters [12].

Copper, the current interconnect material would likely face difficulties in meeting the future needs of microelectronics industry in terms of resistivity and maximum current density. Carbon nanotubes with their extremely low resistivities and high achievable current densities may be a suitable material to replace copper. Successful integration of carbon nanotubes into CMOS electronics requires the following: 1) controlled placement of CNTs, 2) control over their electrical properties, and 3) low contact resistance. The only approach that has been explored until now for the integration of nanotubes into microelectronic interconnects is to grow them vertically using chemical vapor deposition (CVD). Investigators have utilized CVD based MWNTs grown using a catalyst deposited either on a buried electrode [13,14] or directly on metal electrodes [15]. Moreover, SWNTs are the nanotubes of choice for interconnect purposes since they are smaller in diameter than MWNTs and hence more SWNTs can be packed in a given cross-sectional area than MWNTs. The CVD based approach for making SWNT interconnects have various limitations: 1) the requirement of a catalyst metal which increases the contact resistance, 2) the requirement of high processing temperatures (~800°C) which is not CMOS compatible. One can also utilize Plasma-Enhanced CVD (PECVD) to grow SWNTs [16] at a lower temperature (~600°C), yet the process still requires a metallic catalyst. MWNT growth is demonstrated at low temperatures without a catalyst, but yields low quality MWNTs.

The ability to incorporate carbon nanotubes into microdevices in a three-dimensional manner using a low temperature process without a catalyst is very desirable for microelectronics as well as nanotechnology. In this paper, we present a novel approach for 3D assembly of single-walled carbon nanotubes (SWNTs) on a micromachined platform (Fig.1) using alternating current (ac) electric fields.

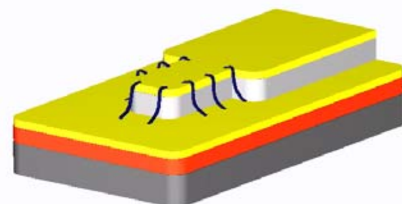

Figure 1: A schematic of SWNTs assembled in a three dimensional fashion on a micromachined platform.

We demonstrate this approach for SWNTs, yet it is also applicable for assembling multi-walled carbon nanotubes (MWNTs) and nanoparticles with direct applications in 3D interconnects, 3D nano-electromechanical systems, and for in-line characterization of manufactured nanomaterials.

2. BACKGROUND AND DEVICE PRINCIPLES

A. Dielectrophoretic Assembly

Dielectrophoresis has become a powerful method for manipulation, trapping and separating micro- and nanoparticles. An electric field set up between electrodes produces a dielectrophoretic force which attracts the nanomaterials in gaps where the gradient of the electric field is maximum or minimum. The biasing scheme for 3D assembly is illustrated in Fig.2. When a polarizable object is placed in a non-uniform electric field, due to its interaction with the field, exhibits a translation motion which forms the basis of dielectrophoretic assembly [17]. Dielectrophoresis occurs in both ac and dc electric fields, however ac fields are preferred since they allow manipulation and assembly of the nanostructures while minimizing and/or suppressing the electrochemical and particle migration effects present while using dc fields [18]. The dielectrophoretic force can be expressed as [19] :

$$F_{DEP} \propto \varepsilon_m \left((\varepsilon_p - \varepsilon_m) / (\varepsilon_p + 2\varepsilon_m) \right) \nabla E^2_{rms} \qquad (1)$$

where ε_p and ε_m are the dielectric constants of the nanoparticles and the solvent medium and E_{rms} is the average field strength. Li and co-workers [20] have demonstrated the use of DEP for manipulation of carbon nanotubes for nanosensing applications while Washizu [21] and Burke [22] have shown that DNA and proteins can also be manipulated using ac electric fields. Furthermore, Amlani [23] and Fritzsche [24] have demonstrated DEP assembly of gold nanoparticles on a planar surface. We extend the planar dielectrophoretic assembly method into three dimensional assembly of single-walled carbon nanotubes utilizing a novel micromachined platform (illustrated in Fig.1). From a nanoassembly perspective, this method overcomes most of the limitations of other methods and is a fairly simple and a versatile method which allows fabrication of vertical interconnects for microelectronics and higher density microdevices.

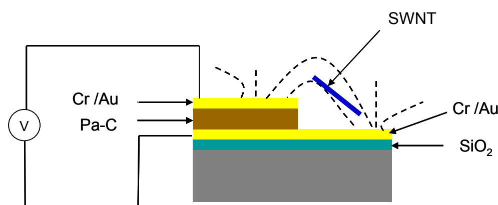

Figure 2: The DEP assembly for making 3D SWNT nanoassembly process.

B. Parylene-C as a dielectric and encapsulant

Parylene, poly-para-xylylene, is the generic name for members of a unique polymer series with more than 20 variations, yet only 3 of them are widely used, Parylene N, C and D. All of these parylenes are produced from the same monomer modified, and a chlorine atom is substituted to one of the aromatic hydrogens for Parylene-C and two of the aromatic hydrogens for Parylene-D. Parylene-C, known to provide a very low permeability to moisture and corrosive gases, is the coating of choice for encapsulation and hence is utilized in our assembly method. Along with its ability to create a true pinhole free insulation, the high resistivity, $6\times 10^{16}\Omega$-cm, and high breakdown voltage (300Volts/μm), indicate that Parylene-C has excellent dielectric properties.

The conventional methods for forming the polymer such as extrusion or molding cannot be applied to Parylene due to its high molecular weight and the high melting temperatures. Similar to vacuum metallization, Parylene polymers are deposited from the vapor phase. In contrast to the high vacuum deposition processes, the Parylene is formed at around 0.1Torr with mean free path on the order of ~100μm. Thus, a substrate in the Parylene deposition chamber will be uniformly impinged by the gaseous monomer, which in turn obtains a truly conformal coating. Furthermore, the deposition rates of Parylene-C are fast, compared with vacuum metallization. Finally, parylene is deposited at room temperature allowing this process to be compatible with back-end CMOS processes.

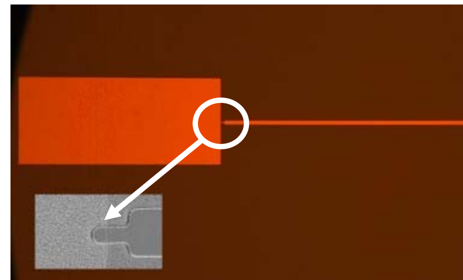

Figure 3: An optical picture of the assembly electrode. Inset shows the SEM micrograph.

C. Electrodes for Nanoassembly

For the assembly of SWNTs, we designed a micromachined platform consisting of a single finger (an optical image is illustrated in Fig.3 with the magnified SEM micrograph shown in the inset). The width of the finger (metal2) is selected as 2μm (limited by photolithography) and has an overlap of 3μm with the first metal layer. The assembly gap was selected as 0.7μm (thickness of the parylene-C layer). The length of the single-walled carbon nanotube used in our experiments is between 3-5 μm, hence the parylene-C layer thickness of 0.7μm was sufficient for this assembly. For assembling SWNTs with shorter and longer dimensions or for assembling other conductive nanostructures, this gap (distance) can be easily adjusted by modifying the thickness of the parylene-C layer. Controlling the thickness in the vertical dimension is relatively easier and allows one to fabricate submicron gaps without the need for

expensive electron-beam lithography. Hence, one of the advantages of our approach is to be able to fabricate submicron gaps utilizing standard tools used in optical lithography.

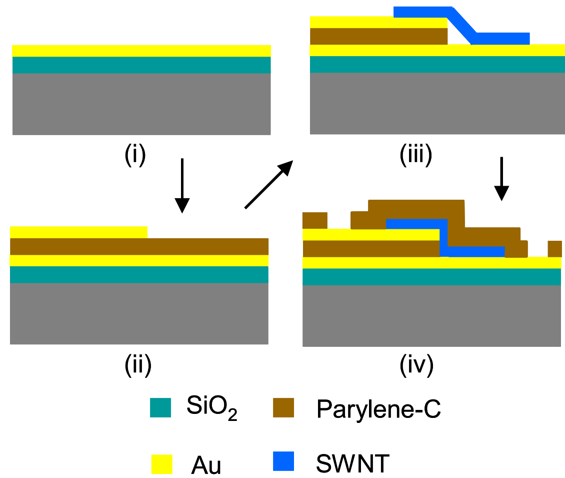

Figure 4: A schematic of the fabrication process.

3. Fabrication

A schematic of the fabrication process is illustrated in Fig.4. The process begins by growing a 1μm thick isolation oxide layer on a silicon wafer followed by the deposition and patterning of the first metal layer (Cr/Au - 175A/1500A) using lift-off process as shown in Fig.4(i). Then, a thin (0.7μm), conformal parylene-C dielectric layer is deposited on the wafers at room temperature. The second metal layer (Cr/Au - 175A/1500A) is then deposited and patterned using lift-off process (Fig.4(ii)). The two metal layers serve as the electrodes to assemble the metallic SWNTs. Next, by using the second metal layer as a mask (in a self-aligned manner), we etch the parylene-C layer in a reactive ion etcher. In this study, commercially available SWNTs (high quality, manufactured using CVD) in an aqueous solution is used. The average diameter of the SWNTs is between 2-5nm and the average length varied from 3-5 μm. An AC voltage of 10V peak-to-peak with a frequency of 10MHz is utilized for this assembly process [19]. After the voltage is turned on, a droplet (2-3μl) of the SWNT solution is dispensed on to the chip containing the microelectrodes. After 30 seconds of assembly, the sample is blow dried with nitrogen and the power is turned off resulting in assembled nanotubes in 3D (Fig.4(iii)). Fig.5 shows an SEM micrograph of the 3D assembled SWNT bundles connecting the top microelectrode to the bottom electrode. Fig.6 displays a close-up side view of this 3D structure and Fig.7 illustrates the top view of the assembled structures with the SWNT bundles appearing as dark lines.

4. Results and Discussion

After assembly, the current-voltage (I-V) curves are first measured from the SWNT bridge verifying that the assembly was successful. The measured current-voltage behavior is linear, as expected since dielectrophoresis is effective on conductive elements. Low contact resistance and good mechanical adhesion of the SWNTs to the substrate are key factors for building 3D interconnects. To enhance the adhesion of the SWNTs to the metal electrodes and to protect the SWNTs from the environment, assembled SWNTs were encapsulated using a thin (1μm) parylene-C

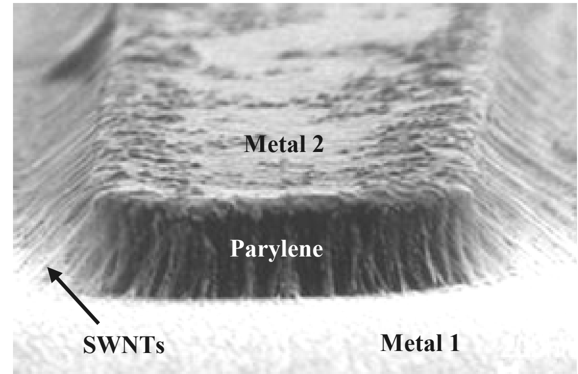

Figure 5: SEM micrograph of the 3D assembled SWNT bundles.

layer. Contacts were next opened on the top parylene layer using a reactive ion etcher (Fig.4(iv)). Current-voltage measurements from the encapsulated 3D SWNT bridge demonstrate a lower metal-SWNT-metal resistance (~380Ω) possibly attributed to the top parylene layer compressing the SWNTs and leading to an improved nanotube-metal contact as displayed in Fig.8.

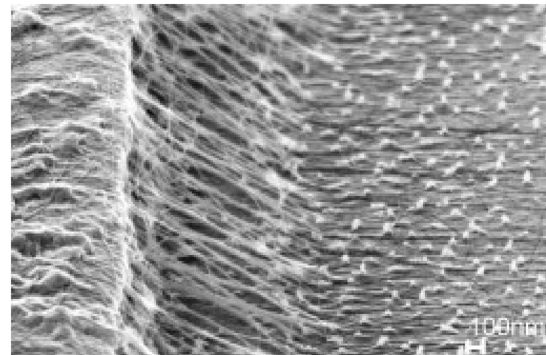

Figure 6: A magnified SEM micrograph of the 3D SWNT bundles connecting the top electrode (metal 2) to the bottom electrode (metal 1).

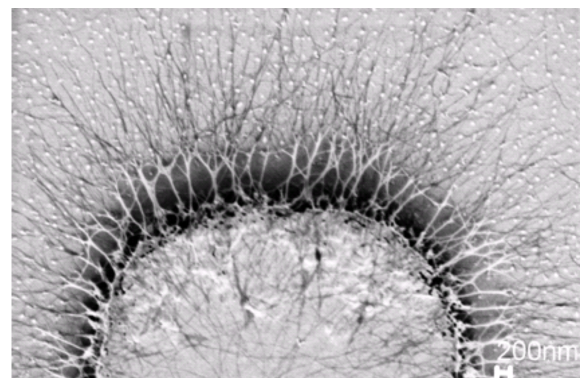

Figure 7: Top view of the assembled SWNT bundles.

5. CONCLUSION

In summary, utilizing dielectrophoresis we have developed a technology for the fabrication of three dimensional interconnects based on Single-walled carbon nanotubes. The two-terminal resistance of this three dimensional SWNT bridge structure resulted in a relatively low value (~545 Ω) demonstrating the feasibility of using this approach for vertical interconnects. Encapsulating the SWNT bridge with a thin (1μm) layer of parylene-C improved the SWNT-metal contact resistance (~380 Ω) while serving as a protective layer from the environment. This approach is quite versatile and can be extended for three dimensional manufacturing of other conductive nanostructures including nanowires, nanobelts and nanoparticles into devices and systems.

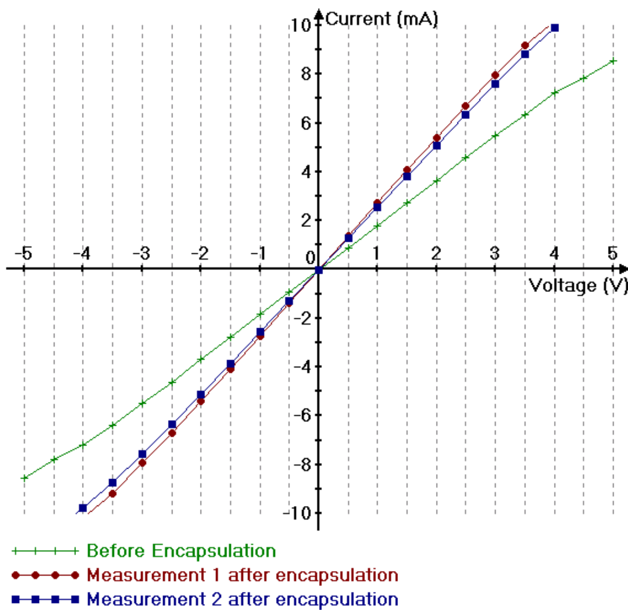

Figure8: The measured I-V curves before and after assembly.

ACKNOWLEDGMENTS

The authors acknowledge financial support from the Air Force Research Laboratory, Hanscom, MA contract # FA8718-06-C-0045, the Nanoscale Science and Engineering Research Centers program of the National Science Foundation (Award NSF-0425826) and the National Science Foundation (Award NER-0608892). The microfabrication was carried out in the Kostas Nanomanufacturing Center.

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