

# Integration of Single-Walled Carbon Nanotubes on to CMOS Circuitry with Parylene-C Encapsulation

Chia-Ling Chen<sup>1</sup>, Vinay Agarwal<sup>2</sup>, Sameer Sonkusale<sup>2</sup> and Mehmet R. Dokmeci<sup>1</sup>

<sup>1</sup>Department of Electrical and Computer Engineering, Northeastern University, Boston, MA, USA

<sup>2</sup>Department of Electrical and Computer Engineering, Tufts University, Medford, MA, USA

E-mail: [mehmetd@ece.neu.edu](mailto:mehmetd@ece.neu.edu)

**Abstract-** This paper presents heterogeneous integration of Single-Walled Carbon Nanotubes (SWNTs) with CMOS integrated circuits using die-level post processing. The chip was fabricated using the AMI 0.5 $\mu$ m CMOS Technology. An electroless zincation process was performed over the Aluminum assembly electrodes (Metal 3 of CMOS technology) to clean and to coat the electrodes with a thin Zinc layer. Low temperature dielectrophoretic assembly was utilized for the placement of the SWNTs on to these electrodes. Encapsulating the CMOS chip with a thin (1 $\mu$ m) parylene-C layer stabilized the SWNT-electrode contact resistance and also provided environmental protection. Electrical measurements from the assembled SWNTs yield ohmic behavior with a two-terminal resistance of  $\sim 44\text{K}\Omega$ . The SWNTs were incorporated on to the CMOS chip as a feedback element of a two-stage Miller compensated high gain operational amplifier. The measured small signal ac gain ( $\sim 1.95$ ) from the inverting amplifier confirmed the successful integration of carbon nanotubes with the CMOS circuitry. This paper lays the foundation for the realization of next generation integrated nanosystems with active nanostructures on CMOS integrated circuits.

**Keywords-** CMOS circuitry; Dielectrophoretic assembly; Nano scale integration; Parylene-C encapsulation; Single-Walled-Carbon-Nanotubes (SWNTs).

## I. INTRODUCTION

Single-Walled Carbon Nanotubes (SWNTs) have been attracting substantial interest as potential building blocks of chemical and biological sensors and future integrated circuits. [1, 2]. SWNTs are graphene cylinders with a wall thickness of one atomic layer and a diameter of about one nanometer. They have very exciting properties such as high aspect ratio, large surface area and hollow geometry [3], high current carrying capacity, superior thermal properties, fast response and good reversibility [4, 5]. These properties present nanotubes as viable candidates for sensing applications, such as gas sensors [6], pressure sensors [7], transistors [8, 9], and thermal sensors [10, 11].

Despite the initial success in implementing nanotube based sensors, the integration of nanotubes onto CMOS electronics is nascent. Recently, catalyst based CVD growth and AFM-assisted alignment are utilized for realizing SWNT based devices. However, the high CNT growth temperatures ( $\sim 700^\circ\text{C}$ ) are not compatible with CMOS technology [12, 13]. The technique of AFM-assisted CNT placement is fairly difficult to control and is impossible to scale up to volume manufacturing [14, 15]. The heterogeneous integration of

nanostructures with CMOS circuitry has numerous advantages: reduced parasitics due to the absence of wire bonding, higher sensor sensitivity through on chip signal processing, and low-cost miniaturized system-on-chip solutions. Historically, utilizing the materials provided by CMOS technology allowed the realization of various integrated micro systems. Moreover, depending solely on CMOS technology has limitations specifically in the availability of materials. [16].

There have been numerous approaches developed to incorporate nanoscale materials on to microdevices. One such technique, Dielectrophoretic (DEP) assembly, classified as a bottom-up approach, is a versatile and low temperature technique to manipulate nanoscale materials [17-19]. In DEP assembly, a nonuniform electric field is generated by the application of an AC voltage, and the nanomaterials suspended in a solution are attracted to regions where the intensity of the field is either maximum (positive DEP) or minimum (negative DEP). Furthermore, DEP assembly is a simple, low cost, and wafer scale process which is compatible with CMOS technology. Previously, Close and coworkers have utilized DEP assembly and have demonstrated MWNT interconnect lines using a relatively complicated post-CMOS approach [20]. In order to isolate the circuitry from the assembly voltage, they first conducted the DEP assembly and then etched the assembly electrodes and connected their CNTs to the circuitry. Furthermore, Chow and coworkers have designed and fabricated a CNT-CMOS low-power sensor chip [21].

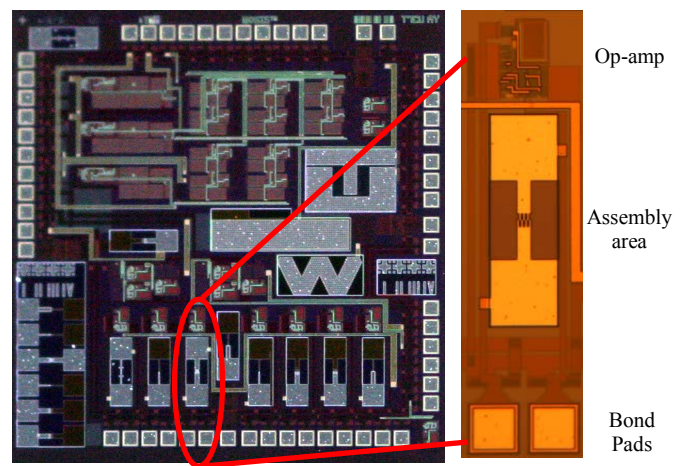


Fig. 1 Optical photograph of the CMOS chip.

However, a relatively high AC voltage ( $20 V_{pp}$ ) was utilized during the DEP assembly which was not compatible with CMOS circuitry. To address this problem, proper design of the electrodes and the circuitry is needed.

In this paper, we present heterogeneous integration of Single-Walled Carbon Nanotubes on to a CMOS chip (Fig.1) utilizing low voltage DEP assembly. The integration of the nanotubes is achieved using a DEP process which is low temperature and is suitable for wafer scale manufacturing. The presented technique is versatile and can be utilized for the realization of numerous nanomaterial based systems fabricated on CMOS circuitry.

## II. EXPERIMENTAL DETAILS

The CMOS chip comprising of the electrodes for the assembly of SWNTs and the interface circuitry was designed and fabricated using the AMI  $0.5\mu m$  CMOS process, provided by MOSIS. SWNTs were assembled on to the electrodes realized by the top metal layer (M3) using Dielectrophoresis. Dielectrophoresis is an inexpensive and high yield method for manipulation, trapping, and separation of micro- and nanomaterials and is utilized in these work. The integration of SWNTs on to CMOS circuitry was realized utilizing a post-CMOS fabrication approach which is illustrated in Fig.2 and is described below.

### A. Electroless Zincation Process

The unpackaged chips,  $2mm \times 2mm$  in size were received from the foundry with an opening in the top passivation layer,

and were mounted on a PDMS/silicon base to facilitate handling. Since the top metal layer of the CMOS chip is made of Aluminum, it readily forms an insulating oxide upon exposure to atmosphere. In order to provide a good contact between the Aluminum electrodes and the SWNTs, an electroless zincation process was performed (Fig.2(b)). It is a selective autocatalytic metal deposition process and a low-cost alternative to vacuum deposition processes and does not require any additional lithography steps. The electroless plating process is fairly straightforward and only requires contact between the aqueous plating solution and the metal lines on the CMOS die [22].

The zincation process started by immersing the CMOS chip in a 1M Sodium hydroxide (NaOH) solution for 2 min to clean the surface of the chip which was followed by a deionized water rinse. Next, the CMOS chip was placed into the zinc plating solution for 2 min which remetalized (with Zinc) the Aluminum electrodes on the CMOS chip. Then, the chip was immersed in 30% Nitric acid ( $HNO_3$ ) for 15 sec which stripped the granulated initial Zinc deposits and which resulted in smoother Zinc layer during the second zincation process. A deionized water rinse followed the second zincation process and completed the electroless zincation process. As shown in Fig.2(b), this was a “displacement reaction” in which the Aluminum ions were replaced by the zinc ions, thus forming a thin zinc layer. This process prevented the underlying Aluminum from getting reoxidized [23] and improved the contact resistance between the assembled SWNTs and the Aluminum assembly electrodes.

### B. Dielectrophoretic Assembly Process

After the electroless zincation process, SWNTs were next assembled in between the two Zinc coated metal electrodes. In these experiments, commercially available aqueous suspension of highly purified HiPCo-grown SWNTs were used with a concentration of  $0.004g/ml$ , which was diluted using deionized water. The average diameter of the SWNTs used was about  $2nm$  with an average length of  $3\mu m$ . A  $1\mu L$  SWNT solution was first dispensed onto the electrodes of the CMOS chip and then an AC sinusoidal signal of  $5V_{pp}$  at a frequency of  $10 MHz$  (Fig.2(c)) was applied between the electrodes to perform the DEP assembly. After 30 sec of DEP assembly, the solution was blown-dried with a nitrogen gun. We next encapsulated the SWNTs with a thin ( $1\mu m$ ) parylene-C layer (Fig.2(d)) with the purpose to provide environmental protection and to stabilize the contact resistance between the nanotubes and the metal electrodes.

## III. RESULTS AND DISCUSSION

### A. SEM Imaging and I-V Characterization

DEP assembly of SWNTs on to CMOS electrodes was achieved with a high yield and a typical assembly area is shown in Fig.3. The insert image shows an enlarged view of the assembled SWNTs connecting two electrodes. Two-

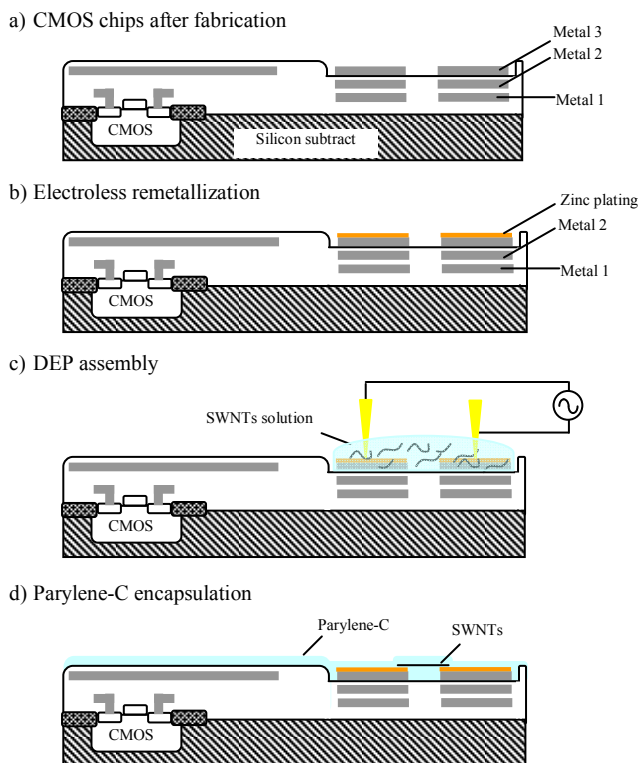


Fig.2 Post-CMOS integration process.

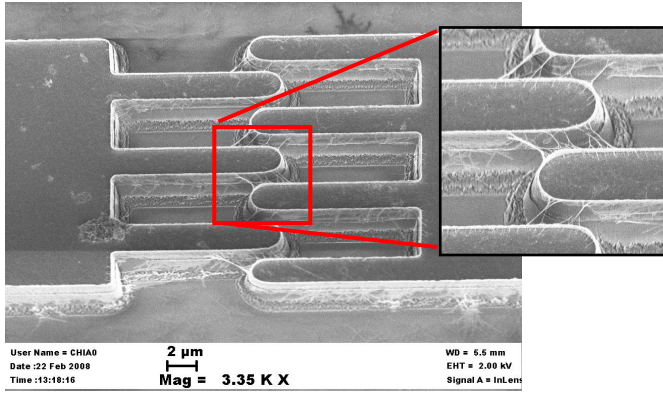


Fig. 3 SEM micrograph of the assembled SWNTs on to microelectrodes connected to CMOS circuitry.

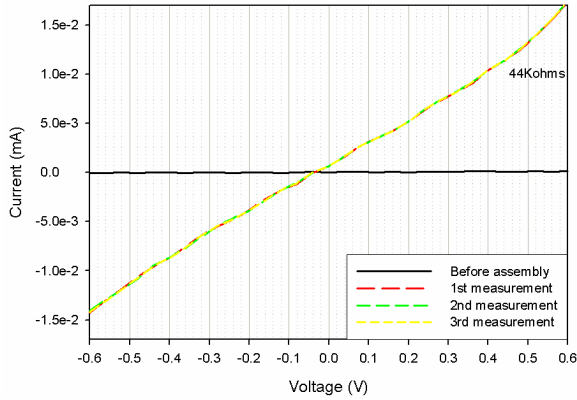


Fig. 4 Two terminal I-V measurements from assembled SWNTs.

terminal I-V measurements confirmed the connectivity between the two electrodes. Fig.4 shows two terminal I-V measurements taken after the DEP assembly process.

After DEP assembly, the SWNTs were attached to the metal electrodes with weak van der Waals forces, and also this attachment was made between two dissimilar materials. In order to address the contact problem, one approach is to utilize a focused ion beam (FIB) tool to selectively deposit metal patches on to areas where the the SWNTs are attached to the metal electrodes. In this work, we deposited a thin parylene-C layer (1 $\mu$ m) after the DEP assembly. The parylene coating as demonstrated previously, helped to stabilize the contact resistance between the SWNTs and the metal electrodes [24]. The black line in Fig.4 shows the I-V measurement before the DEP assembly and as expected, depicts zero net current flow. Red, green and yellow lines in Fig.4 show a sequence of stable I-V measurements after the parylene-C deposition corresponding to a measured resistance of  $\sim 44$ K Ohms.

### B. CMOS Readout Circuitry

The assembly electrodes were realized using the metal 3 layer of the CMOS technology and were connected to a high gain Miller-compensated single-ended operational amplifier [25]. The SWNTs were assembled onto the feedback path of an inverting amplifier configuration ( $R_{ref}$ ) as shown in Fig.5.

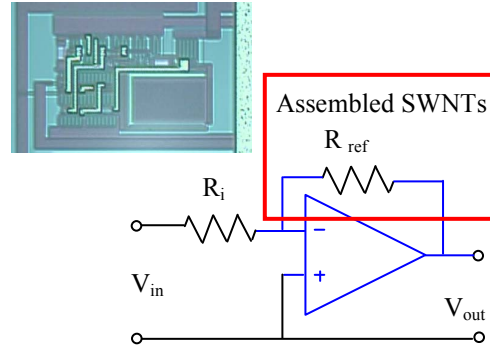


Fig.5 Schematic drawing showing an op-amp in the inverting configuration with assembled SWNTs acting as the reference resistor. Inset shows optical photograph of the fabricated op-amp.

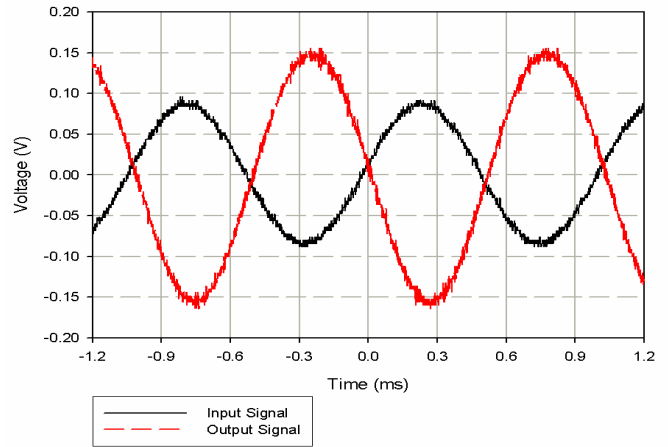


Fig. 6 Measured input and output signals from the inverting op-amp with SWNTs as the reference resistor. Using an input resistance ( $R_i$ ) of 22K Ohm, the measured output gain was  $\sim 1.95$ .

The resistance of the assembled SWNTs was measured as  $\sim 44$ K Ohms and an external resistor ( $R_i$ ) of 22K Ohms was used in the circuit. Measured input and output signals from the inverting op-amp with SWNTs as the reference resistor is displayed in Fig.6 and the gain of the inverting amplifier was measured as  $\sim -1.95$ . This value agreed well with the calculated gain ( $\text{Gain} = -R_{ref}/R_i = -2$ ).

The output waveform corresponding to a unit step function was fed in to the operational amplifier with the bundled SWNTs placed as the feedback resistor is shown in Fig.7. Using the approximate relationship between the time constant and cutoff frequency [26, 27]:

$$f_c = 1/1.5t_c \quad (1)$$

where  $f_c$  is the cutoff frequency and  $t_c$  is the time constant of the response and the cutoff frequency of the system was estimated to be  $\sim 9.5$  kHz.

### IV. CONCLUSIONS

Low temperature heterogeneous integration of SWNTs on to standard CMOS circuitry utilizing DEP assembly has been demonstrated. A high gain Miller-compensated single-ended

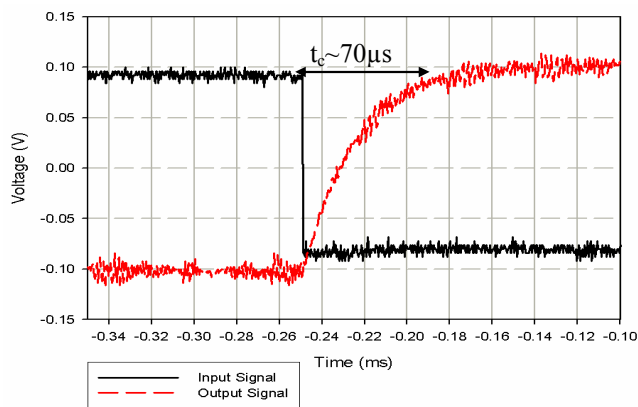


Fig. 7 Frequency response from the inverting op-amp with SWNTs as the reference resistor. The cutoff frequency was estimated to be 9.5 KHz.

operational amplifier was designed and fabricated using the AMI 0.5 $\mu$ m CMOS process. Electroless zincation was utilized to clean and remetalize a Zinc layer on to the Aluminum assembly electrodes. The DEP assembly was optimized (an AC signal of 5V<sub>pp</sub> and 10MHz) to be compatible with CMOS technology. A conformal, 1 $\mu$ m thick parylene-C layer was deposited as an encapsulation layer to provide environmental protection and to stabilize the SWNT to metal electrode contacts. The measured two-terminal resistance of the SWNTs were around 44K Ohms. The cutoff frequency of the SWNT assembled op-amp circuit was estimated to be 9.5 KHz. This versatile approach can be extended to the integration of other nanostructures on to CMOS electronics paving way for the realization of next generation of biological and chemical nanosensors and high performance integrated circuits.

#### ACKNOWLEDGMENTS

This research was conducted at the George J. Kostas Nanoscale Technology and Manufacturing Research Center at Northeastern University. The authors kindly acknowledge funding from the National Science Foundation Nanoscale Science and Engineering Center for High-rate Nanomanufacturing (NSF grant-0425826).

#### REFERENCES

- [1] E. S. Snow, J. P. Novak, M. D. Lay, E. H. Houser, F. K. Perkins, and P. M. Campbell, "Carbon nanotube networks: Nanomaterial for macroelectronic applications," *J. Vac. Sci. Technol. B*, vol. 22, pp. 1990-1994, 2004.
- [2] S. Iijima, "Helical microtubules of graphitic carbon," *Nature*, vol. 354, pp. 56-58, 1991.
- [3] C. K. M. Fung and W. J. Li, "Ultra-low-power and high-frequency-response carbon nanotube based MEMS thermal sensors," in *Proc., Int. Conf. on Intelligent Robots and Systems (IEEE/RSJ)*, Las Vegas, Nevada, 2003, pp. 2371-2376.
- [4] J. Abraham, B. Philip, A. Witchurch, V. K. Varadan, and C. C. Reddy, "A compact wireless gas sensor using a carbon nanotube/PMMA thin film chemiresistor," *Smart Mater. Struct.*, vol. 13, pp. 1045-1049, 2004.
- [5] B. Philip, J. K. Abraham, A. Chandrasekhar, and V. K. Varadan, "Carbon nanotube/PMMA composite thin films for gas-sensing applications," *Smart Mater. Struct.*, vol. 12, pp. 935-939, 2003.
- [6] J. Kong, N. R. Franklin, C. Zhou, M. G. Chapline, S. Peng, K. Cho, and H. Dai, "Nanotube molecular wires as chemical sensors," *Science*, vol. 287, pp. 622-5, 2000.

- [7] C. K. M. Fung, "Fabrication of CNT-based MEMS piezoresistive pressure sensors," in *Proc., 5<sup>th</sup> Int. Conf. on Nanotechnology (IEEE-NANO)* Nagoya, Japan, 2005, pp. 199-202.
- [8] E. Artukovic, M. Kaempgen, D. S. Hecht, S. Roth, and G. Gruner, "Transparent and flexible carbon nanotube transistors," *Nano Lett.*, vol. 5, pp. 757-60, Apr 2005.
- [9] D. R. Hines, S. Mezheny, M. Breban, E. D. Williams, V. W. Ballarotto, G. Esen, A. Southard, and M. S. Fuhrer, "Nanotransfer printing of organic and carbon nanotube thin-film transistors on plastic substrates," *Appl. Phys. Lett.*, vol. 86, p. 163101, 2005.
- [10] S. Selvarasah, C.-L. Chen, S.-H. Chao, P. Makaram, A. Busnaina, and M. R. Dokmeci, "A three dimensional thermal sensor based on single-walled carbon nanotubes," in *Proc., 14<sup>th</sup> Int. Conf. on Solid-State Sensors, Actuators and Microsystems (Transducers '07)* Lyon, France, 2007, pp. 1023-1026.
- [11] C. K. M. Fung, V. T. S. Wong, R. H. M. Chan, and W. J. Li, "Dielectrophoretic batch fabrication of bundled carbon nanotube thermal sensors," *IEEE Trans. on Nanotechnology*, vol. 3, pp. 395-403, 2004.
- [12] H. T. Soh, C. F. Quate, A. F. Morpurgo, C. M. Marcus, J. Kong, and H. Dai, "Integrated nanotube circuits: Controlled growth and ohmic contacting of single-walled carbon nanotubes," *Appl. Phys. Lett.*, vol. 75, pp. 627-629, 1999.
- [13] T. Hertel, R. Martel, and P. Avouris, "Manipulation of individual carbon nanotubes and their interaction with surfaces," *J. Phys. Chem. B*, vol. 102, pp. 910-915, 1998.
- [14] M. Nihei, M. Horibe, A. Kawabata, and Y. Awano, "Carbon nanotube vias for future LSI interconnects," in *Proc., IEEE Int. Conf. on Interconnect Technology*, Burlingame, CA, USA, 2004, pp. 251-253.
- [15] T. Junno, K. D. L. Montelius, and L. Samuelson, "Controlled manipulation of nanoparticles with an atomic force microscope," *Appl. Phys. Lett.*, vol. 66, pp. 3627-3629, 1995.
- [16] G. K. Fedder, "CMOS-Based Sensors," in *Proc., 5<sup>th</sup> Int. Conf. on Sensors (IEEE-Sensors)*, Irvine, CA, 2005.
- [17] N. G. Green, H. Morgan, and J. J. Milner, "Manipulation and trapping of sub-micron bioparticles using dielectrophoresis," *J. Biochem. Biophys. Methods*, vol. 35, pp. 89-102, 1997.
- [18] K. D. Hermanson, S. O. Lumsdon, J. P. Williams, E. W. Kaler, and O. D. Velev, "Dielectrophoretic assembly of electrically functional microwires from nanoparticle suspensions," *Science*, vol. 294, pp. 1082-6, 2001.
- [19] H. A. Pohl, *Dielectrophoresis: the behavior of neutral matter in nonuniform electric fields*. Cambridge; New York: Cambridge University Press, 1978.
- [20] G. F. Close, S. Yasuda, B. Paul, S. Fujita, and H.-S. P. Wong, "A 1 GHz integrated circuit with carbon nanotube interconnects and silicon transistors," *Nano Lett.*, vol. 8, pp. 706-709, 2008.
- [21] C. T. Chow, M. L. Y. Sin, P. H. W. Leong, W. J. Li, and K. P. Pun, "Design and modeling of a CNT-CMOS low-power sensor chip," in *Proc., 2nd Int. Conf. on Nano/Micro Engineered and Molecular Systems (IEEE-NEMS '07)*, Bangkok, Thailand, 2007, pp. 1209-1214.
- [22] J. H. Lau, *Flip Chip Technologies*. New York: McGraw-Hill, 1995.
- [23] M. Datta and S. A. Merritt, "Electroless Remetalization of Aluminum Bond Pads on CMOS Driver Chip for Flip-Chip Attachment to Vertical Cavity Surface Emitting Lasers (VSCEL's)," *IEEE Trans Components and Packaging Technology*, vol. 22, pp. 229-236, 1999.
- [24] P. Makaram, S. Selvarasah, X. Xiong, C.-L. Chen, A. Busnaina, N. Khanduja, and M. R. Dokmeci, "Three-Dimensional Assembly of Single-Walled Carbon Nanotube Interconnects Using Dielectrophoresis," *Nanotechnology*, vol. 18, p. 395204, 2007.
- [25] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.
- [26] C. Liu, J. B. Huang, Z. Zhu, F. Jiang, S. Tung, Y. C. Tai, and C. M. Ho, "A micromachined flow shear-stress sensor based on thermal transfer principle," *J. Microelectromechanical systems*, vol. 8, pp. 90-99, 1999.
- [27] K. W. C. Lai, C. K. M. Fung, V. T. S. Wong, M. L. Y. Sin, W. J. Li, and C.-P. Kwong, "Development of an automated microspotting system for rapid dielectrophoretic fabrication of bundled carbon nanotube sensors," *IEEE Trans. on Automation Science and Engineering*, vol. 3, pp. 218-227, 2006.