**RESUME OF FABRIZIO LOMBARDI: December 2, 2000.**

Chair and International Test Conference Endowed Professor,
Department of Electrical and Computer Engineering,
Northeastern University
309 Dana Research Building
Boston, Massachusetts 02115

**Date and Place of birth:** August 6, 1955 in Formia, Italy
**Marital Status:** Married, two children (a girl and a boy)
**Citizenship:** US

**Education:**

- Ph.D., University College London, University of London, 1982. (Ph.D. Thesis Title: *Modelling and Analysis of Fault Tolerant Microcomputer Systems* ).
- M.Sc. in Microwaves and Modern Optics, University College London, University of London, 1978.
- Dipl. in Microwave Engineering, University College London, University of London, 1978.
- B.Sc. in Electronic Engineering (Hons), University of Essex, 1977.

**Specializations and Research Interests:**

- Fault-Tolerant Computing, VLSI CAD, Testing, Configurable Computing, Distributed Systems.

**Record of Employment:**

- 1998-present: Chairperson and Holder of the International Test Conference (ITC) Endowed Professorship, Department of Electrical and Computer Engineering, Northeastern University, Boston.
- 1993-1998, Full Professor and Holder of Halliburton Professorship (1995), Department of Computer Science, Texas A&M University, College Station.
- 1991-1998, Courtesy Appointment in the Department of Electrical Engineering, Texas A&M University, College Station.
- 1989-1994, Graduate Program Advisor, Department of Computer Science, Texas A&M University, College Station.

- 1988-1993, Associate Professor of Computer Science, Texas A&M University, College Station.
- 1984-1988, Assistant Professor of Electrical and Computer Engineering and Assistant Professor in the Telecommunication Graduate Program, University of Colorado at Boulder.
- 1982-1984, Assistant Professor of Computer Science/Electrical Engineering, Texas Tech University, Lubbock.
- 1978-1982, Research Assistant, Microwave Research Unit, University College London.
- 1978-1980, Research Associate, Cardiothoracic Institute, Department of Clinical Pharmacology, University of London Medical Postgraduate School, Brompton Hospital, London.

**Awards:**

- Cardiothoracic Institute Research Support Award, United Kingdom (1978-1979).
- National Research and Development Corporation Research Support Award, United Kingdom (1979-1980).
- IEEE/Engineering Foundation's Research Award, USA (1985).
- British Columbia Advanced Systems Institute/University of Victoria Visiting Fellow, Canada (1988-89).
- Texas Engineering Experimental Station Research Fellow (1991-92 and 1997-1998).
- Selected as *Key Faculty Researcher* "because of the nature and industry relevance of pursued research" from the Industrial/Federal Government Steering Committee on National Technology Policy to provide guidance on Transfer and Commercialization of University-Originated Technologies for major research Laboratories such as Sematech, Nasa and SRC (only 100 faculty researchers from US Universities have been selected) (1992).
- Faculty Recognition Award, College of Engineering Texas A&M University and The Texas Engineering Experimental Station, (1993,1995).
- Distinguished Visitor of the IEEE Computer Society, (1990-93).
- International Research Program Award, Japan Advanced Institute of Science and Technology (JAIST), Japan (1993-1999).
- Halliburton Professorship, Texas A&M University (1995).
- Silver Quill Award, Motorola, Austin (1996).
- Certificate of Appreciation, TC on Test Technology, IEEE Computer Society (1998).

- Certificate of Appreciation, TC on Test Technology, IEEE Computer Society (1999).

**Courses Taught:**

- Graduate Level (600 level): Fault Tolerant Computing (TTU,CU,TAMU), Microwave Techniques (UCL), Digital Computer Design (TTU), Digital Communication Systems (CU), Digital Network Systems (CU), Integrated System Design Automation (TAMU), Advanced Computer Systems Design (TAMU), Defect Tolerance (TAMU), Array Systems (TAMU), Testing and Diagnosis of Digital Systems (TAMU), Advanced Logic Design (TAMU), Computer Architecture (TAMU).
- Upper Undergraduate Level (Senior only)(400 and 500 level): Analog and Digital Computation (TTU), Microprocessors (TTU), Electromagnetic Theory (TTU), Computer Organization (CU,TAMU), Switching and Finite Automata (CU).
- Other Undergraduate Courses (300 level and lower): Logic Laboratory (TTU), Introduction to Programming (TTU), Microprocessors (TTU), Microcomputer Architecture and Programming (CU), Engineering Problem Solving and Computing (TAMU).

**Graduate Students Supervision:**
Major advisor only;
*Master Degree with thesis:*

1. S. Ratheal, "Reconfiguration Strategies in Multiprocessing Systems," TTU, April 1984.
2. A.M. Azmi, "A Floating Point System with Variable Length Exponent" CU, June 1987.
3. C.M. Kao, "Design of Testable Homogeneous VLSI Structures," TAMU, December 1989.
4. P.Y.M. Koo, "Yield Enhancement of VLSI/WSI Array Systems" TAMU, December 1989.
5. J. Salinas, "The F-Path Approach for Pattern Generation in Microprocessor Testing" TAMU, August 1991.
6. D. Ray, "A Novel Approach for Generating Multiple Unique Input/Output Sequences for Conformance Testing of Protocols" TAMU, December 1991.
7. C. Feng, "Detectability and Fault Detection Techniques for Finite State Machines," TAMU, May 1992.
8. U. Arunkumar, "Verification and Validation of Timed Protocols," TAMU, May 1992.
9. G. Menta, "A Hierarchical Approach to Conformance Testing of Protocols," TAMU, August 1992.

10. M. V. Bommena, "C-Testability of a Ripple-Carry Adder under Multiple Faults, TAMU, August, 1992, (with Dr. K. Watson, EE Department).

11. M. Sathyanarayana, "Generation of Test Sequences for Programmable Logic Array-Based Finite State Machines," TAMU, May 1994.

12. R. T. Wilkinson, "Performance Evaluation of Scalable Fault-Tolerant Parallel Computing Systems, TAMU, May 1996. (with Dr. D. Avresky, CS Department).

13. D. G. Ashen, "A Comprehensive Test Method for Reprogrammable FPGAs," TAMU, August 1996 (with Dr. D. Ross, EE Department).

14. L. Zhao, "Iddq Testing of FPGAs", TAMU, August 1997, (with Dr. D.H. Walker, CS Dept),

15. D. Krishnamoorthy, "Performance Evaluation of Configurable Arrays with Mesh Interconnections and Wormhole Routing," TAMU, December 1997.

16. B. Liu, "A New Approach to Test Programmable Wiring Networks for VLSI," TAMU, May 1998.

17. S.J. Ruiwale, "Testing Dynamically Reconfigurable FPGAs," TAMU, December 1998 (with Dr. G. Choi, EE Department).

18. E. Mizan, Northeastern University, in progress.

19. X. Liu, Northeastern University, in progress.

*Master Degree with project:*

1. Chanda, "Fault Detection in Fine-Grain Hierarchically-Connected FPGAs by Gate-Level Simulation," TAMU, August 1998.

2. External examiner for David Wessels (M. S. University of Victoria, Canada, 1990).

*Ph.D. Degree*

1. D. Sciuto (currently a Full Professor with the Politecnico di Milano, Italy), "Testing and Reconfiguration Techniques for VLSI Processor Arrays", CU, November 1988.

2. X. Sun (currently with Motorola, Semiconductor Products Sector, Austin), "Automatic Conformance Testing of Protocols Implemented in Software or Hardware," TAMU, August 1993.

3. Y.-N. Shen (currently with AMD-Vantis, San Jose), "Verification and Validation of Finite State Machines," TAMU, December 1993.

4. J. Salinas (currently with the Applied Research Laboratory, TAMU, College Station). "Reconfigurable and Testable Computer Systems for WSI," TAMU, August 1994.

5. S. S. Kim (currently an Assistant Professor with Ajou University, Seoul), "Modeling Fault Tolerance and Testing in Complex Digital Systems," TAMU, August 1995.

6. T. Liu (currently with Actel, San Jose), "Design and Test of Programmable Interconnects for Digital Systems," TAMU, August 1995.

7. C. Feng (currently with Ameritch, Chicago), "Adaptive Fault Diagnosis for Multicomputer Systems," TAMU, August 1995, (with L. Bhuyan).

8. H.H. Kari (currently with Nokia Telecomm., Helsinki), "Latent Sector Faults and Reliability of Disk Arrays," Helsinki Institute of Technology (Finland), June 1997.

9. N. Park (currently an Assistant Professor with Oklahoma State University), "Modeling and Evaluating the Quality Assurance of Multi-Chip Module Systems," TAMU, June 1997.

10. X.T. Chen (currently with Lucent Bell Labs, Allentown), "A Computer-Aided Testing Framework for Field Programmable Gate Arrays: from Verification to Configuration," TAMU, August 1997.

11. D. Schin (currently with Sprint Communication, Kansas City), "Algorithms and Techniques for Unique Input/Output Sequence Generation," TAMU, August 1998.

12. W. Feng (currently with Lucent Bell Labs, Allentown), "Computer-Aided Testing of Switching and Interconnect Resources of FPGAs," TAMU, December 1998.

13. J. Zhao (currently with Lucent Bell Labs, Allentown), "Interconnect Testing of Embedded Memories at Chip and System Level," TAMU, May 1999.

14. M. Al-Hashimi (currently an associate Professor with King Abdulaziz University, Jeddah, Saudi Arabia), "Fault Tolerance in Multiprocessor Systems by N-Modular Redundancy on Demand," TAMU, May 2000.

15. Y. An, (currently with Lucent Technologies, Naperville) "Reliable Strategies for Wireless Mobile Environments," TAMU, August 2000.

16. F. Karimi, Northeastern University, in progress.

17. X. Wang, Northeastern University, in progress.

18. A. Khalili, Northeastern University, in progress.

19. N. Natchev, Northeastern University, in progress.

**Research Associates:**

1. W.-K. Huang (Fudan University, PRC), 1986-1987, University of Colorado,

2. Y.-N. Shen (Fudan University, PRC), 1988-1991, University of Colorado and Texas A&M University.

3. T. Liu (Academy of Sciences, PRC), 1990-1991, Texas A&M University.
4. M.S. Kim (Korean Army Academy), 1992-1993, Texas A&M University.
5. P. Liu (Academia Sinica, PRC), 1992-1993, Texas A&M University.
6. Q. Chi (Xi'an Jiaotong University, PRC), 1993, Texas A&M University.
7. J. Tong (Fudan University, PRC), 1995-1996, Texas A&M University.
8. W.K. Huang (Fudan University, PRC), 1994-1996, Texas A&M University.
9. F.J. Meyer, 1996-1998, Texas A&M University.

**Professional Societies:**

- Institute of Electrical and Electronics Engineers (IEEE), Computer Society (Member).
- European Association of Microprocessing and Microprogramming (EAMM) (Member).
- Association for Computing Machinery (ACM), SIGARCH, SIGMETRICS (Member).
- Society for Industrial and Applied Mathematics (SIAM) (Member).
- Eta Kappa Nu, Honorary Society of Electrical Engineers.
- Who's Who in Frontiers of Science and Technology, 2nd Edition, November 1985.
- Member of IEEE Computer Society Technical Committees on Distributed Processing, Fault-Tolerant Computing, Real-Time Systems, VLSI, Test Technology, Computer Architecture.
- Member of IEEE Test Technology Technical Committee on Defect and Fault Tolerance.

**Professional Service (Conferences and Symposia):**

- Participant to NASA/AIAA Workshop on Applied Fault Tolerant Computing for Aerospace Systems, Fort Worth, 1982.
- President Undergraduate Research Award (with H.E. Harvey), Texas Tech University, 1982.
- Session Chairman at *1983 IEEE Region 5 Conf. on Technology for an Efficient Tomorrow,* "Special Problems," Houston, April 1983.
- Session Chairman at *1983 Conference on Information Sciences and Systems,* "Fault Analysis" The Johns Hopkins University, Baltimore, March 1983.
- Invited Participant to NASA/IEEE Workshop on *Laboratories for Reliable System Research,* Langley, April 1983.

- Organizer and Chairman of 2 Special Sessions on "Test Technology for Large Scale Systems: I, Theory; II, Practice," *IEEE Int. Symp. on Circuits-and-Systems* , Montreal, May 1984.

- Organizer and Chairman of a Session on "Fault Tolerant Computing" *IEEE Phoenix Conference on Computers and Communications,* March 1985.

- Co-Organizer and Chairman of a Panel Session on "Diagnostics and Fault Tolerance" *1st IEEE International Conference on Supercomputing Systems,* St. Petersburg, December 1985 (with A.T. Dahbura).

- Program Committee Member to *IEEE Real-Time Systems Symposium,* New Orleans, December 1986.

- Session Chairman on "Design for Testability and Fault Tolerance" *12th Symposium on Microprocessing and Microprogramming,* Venice, September 1986.

- Session Chairman on "Multiprocessors: Short Notes," *12th Symposium on Microprocessing and Microprogramming,* Venice, September 1986.

- Co-Director, *NATO Advanced Study Institute on Testing and Diagnosis of VLSI and ULSI,* Como, July 1987.

- Invited Participant to *IFIP Workshop on Wafer Scale Integration,* London, September 1987

- Session Chairman on "Real-Time System Design," *IEEE Real-Time Systems Symposium,* San Jose, December 1987.

- Program Committee Member, *IEEE Real-Time Systems Symposium,* Huntsville, December 1988.

- Program Committee Member, *IFIP Workshop on WSI,* Como (Italy), June 1989; session chairman on "Architectures II".

- Program Committee Member, *Euromicro Workshop on Real-Time,* Como (Italy), June 1989; session chairman on "Testing and Fault Tolerance".

- Invited Keynote Speaker, *4th Technical Workshop: New Directions for IC Testing,* Victoria (Canada), October 1989.

- Program Committee Member, *IEEE Int. Workshop on Defect and Fault Tolerance in VLSI Systems,* Hidden Valley, November 1991.

- Session Chairman on "Fault Tolerance", *IEEE Int. Workshop on Defect and Fault Tolerance in VLSI Systems,* Hidden Valley, November 1991.

- Session Chairman on "Reconfigurable Array Concepts," *IEEE Int. Conf. on WSI,* San Francisco, January 1992.

- Member of the panel on "Conformance Testing," *1992 Int. Phoenix Conf. on Computers and Comm.,* Phoenix, April 1992.
- Program Committee Member, *IEEE Fault Tolerant Computing Symposium,* Boston, June 1992.
- Session Chairman on "Synthesis for Testability and Fault Protection," *IEEE Fault Tolerant Computing Symposium,* Boston, June 1992.
- Program Chairman, *IEEE Int. Workshop on Defect and Fault Tolerance in VLSI Systems,* Dallas, November 1992.
- Topic Coordinator "Recent Advances," *IEEE VLSI Test Symposium,* Atlantic City, April 1992.
- Program Committee Member, *Int. Workshop on Algorithms and Data Structures (WADS),* Montreal, August 1993.
- Session Chairman on "Numerical Algorithms," *ICPP,* St. Charles, August 1993.
- Session Chairman on "Reconfiguration," *IEEE Int. Workshop on Defect and Fault Tolerance in VLSI Systems,* Venice October 1993.
- General Chairman, *IEEE Int. Workshop on Defect and Fault Tolerance in VLSI Systems,* Venice, October 1993.
- Session Chairman on "Testability," *IEEE International Conference on WSI,* San Francisco, January 1994.
- Vice General Chairman, *IEEE Int. Workshop on Fault Tolerance in Parallel and Distributed Systems,* College Station, June 1994.
- Program Committee Member, *IEEE Int. Workshop on Defect and Fault Tolerance in VLSI Systems,* Montreal, October 1994; session chair on "Testable Architectures".
- Program Committee Member, *International Symposium on Parallel Architectures, Algorithms and Networks,* Kanazawa, December 1994; session chair on "Fault Tolerance".
- Program Committee Member, *1st IEEE Int. On-Line Testing Workshop,* Nice, July 4-5, 1995.
- Invited Guest Speaker, *6th Symposium on Fault Tolerant Computers (Simposio de Computadores Tolerantes a Falhas), Brazilan Computer Society (Sociedade Brasileira de Computacao),* Canela, August 1995.
- Program Committee Member, *IEEE Int. Workshop on Defect and Fault Tolerance in VLSI Systems,* Lafayette, November 1995.
- Publicity and Publication Chair, *2nd IEEE Int. Symp. on High Performance Comp. Arch.,* San Jose, January 1996.

- Member of panel on "Can defect-tolerant chips better meet the quality challenge?" *IEEE VLSI Test Symposium,* Princeton, May, 1996.
- Program Committee Member, *Int. Symp. on Parallel Architectures, Algorithms and Networks,* Beijing, June 1996.
- General Chairman, *IEEE Int. Workshop on Embedded Fault-Tolerant Systems,* Dallas, September, 1996.
- Program Committee Member, *IEEE Int. Conference on Innovative Systems on Silicon,* Austin, October 1996.
- Session Chairman on "Testing and Yield," *IEEE Int. Conference on Innovative Systems on Silicon,* Austin, October 1996.
- Program Committee Member, *4th Annual Workshop on Real-Time Applications,* Montreal, October 1996.
- Steering Committee Member, *IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems,* Boston, November, 1996.
- Program Committee Member, *IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems,* Boston, November, 1996.
- Member of panel on "On-Chip Testing," *IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems,* Boston, November 1996.
- Session Chairman on "Defect Avoidance," *IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems,* Boston, November 1996.
- General Chair, *IEEE Int. Workshop on Memory Technology, Design and Testing,* San Jose, August 1997.
- Program Committee Member and Topic Chair "Reconfiguration, Defect and Fault Tolerance," *IEEE Int. Conf. On Innovative Systems on Silicon,* Austin, October 1997.
- Session Chairman on "Innovations in Testing," *IEEE Int. Conf. On Innovative Systems on silicon,* Austin, October 1997.
- Program Committee Member, *IEEE Int. Conf. on Defect and Fault Tolerance in VLSI Systems,* Paris, November 1997.
- Session Chairman on "Self-Checking and Coding," *IEEE Int. Conf. on Defect and Fault Tolerance in VLSI Systems,* Paris, November, 1997.
- Program Committee Member, *IEEE/ACM Int. Conf. on FPGAs,* Monterey, February 1998.
- Session Chairman on "Technology Mapping for FPGAs," *ACM Int. Symp. on FPGAs,* Monterey, February 1998.

- Program Committee Member, *IEEE Workshop on Fault-Tolerant Parallel and Distributed Systems,* Orlando, April 1998.
- Program Chair, *IEEE Int. Workshop on Embedded Fault-Tolerant Systems,* Boston, May 1998.
- Session Chairman on "Hardware/Software Co-Design of Embedded Computing Systems," *IEEE Int. Workshop on Embedded Fault-Tolerant Systems,* Boston, May 1998.
- Program Committee Member, *IEEE Int. Conference on Parallel Processing,* August 1998.
- General Chair, *IEEE Int. Workshop on Memory Technology, Design and Testing,* San Jose, August 1998.
- Program Committee Member, *7th IEEE Int. Conf. on Computer Communications amd Networks,* Lafayette, October 1998.
- Program Committee Member, *PACT'98 Workshop on Reconfigurable Computing,* Paris, October 1998.
- Program Committee Member, *IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems,* Austin, October, 1998.
- Program Committee Member, *IEEE/ACM Int. Conf. on FPGAs,* Monterey, February 1999.
- Program Committee Member, *RAW'99: the 6th Reconfigurable Architectures Workshop,* San Juan de Puerto Rico, April 1999.
- Program Committee Member, *8th IEEE North Atlantic Test Workshop,* West Greenwich, May 1999.
- Session Chiarman on "Verification and Functional Test," *8th IEEE North Atlantic Test Workshop,* West Greenwich, May 1999.
- Program Committee Member, *IEEE International Symposium on Memory Technology, Design and Testing,* San Jose, August 1999.
- Session Chairman on "Architecture and Applications," *IEEE Symposium on Memory Technology, Design and Testing,* San Jose, August 1999.
- Program Committee Member, *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,* Alberqueque, October 1999.
- Program Committee Member, *IEEE/ACM International Conference on FPGAs,* Monterey, February 2000.
- Program Committee Member, *RAW'2000: the 7th Reconfigurable Architectures Workshop,* Cancun, May 2000.

- Program Committee Member, *9th IEEE North Atlantic Test Workshop,* Gloucester, May 2000.
- Program Committee Member, *IEEE International Workshop on Solving the Memory Wall,* Vancouver, June 2000.
- Session Chairman on "Memory Technology", *IEEE International Workshop on Solving the Memory Wall,* Vancouver, June 2000.
- Program Committee Member, *IEEE International Symposium on Memory Technology, Design and Testing,* San Jose, August 2000.
- Session Chairman on "New Ideas," *IEEE International Symposium on Memory Technology, Design and Testing,* San Jose, August 2000.
- General Co-Chair, *IEEE International Workshop on Embedded Fault-Tolerant Systems,* Washington, September 2000.
- Program Committee Member, *IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems,* Mt. Fuji-Yamanashi, October 2000.
- Session Chairman on "BIST," *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,* Mt. Fuji-Yamanashi, October 2000.
- Program Committee Member, *10th IEEE North Atlantic Test Workshop,* Gloucester, May 2001.

**Professional Service (Editorial and Refereeing):**

- Associate Editor, *IEEE Transactions on Computers,* 1996-present.
- Associate Editor, *IEEE Design and Test,* 1999-present.
- Member Advisory Editorial Board, *Journal of Microelectronic System Integration,* Plenum Press, 1993- present.
- Editorial Correspondent in the USA for *Euromicro,* 1986 - 88.
- Invited Guest Editor of a Special Issue on Fault Tolerant Computing, *Microprocessing and Microprogramming,* North Holland Publ. Co., vol. 20, no. 4-5, June 1987.
- Invited Guest Editor of a Special Issue on Defect and Fault Tolerance in VLSI Systems, *Journal of Microelectronic System Integration,* vol. 3, No. 2, Plenum Press, June 1995.
- Invited Guest Editor of a Special Issue on "Field Programmable Gate Arrays," *IEEE Design & Test Magazine,* vol. 15, No. 1, 1998.
- Invited Guest Editor (with D. R. Avresky, K.E. Grosspiesch, and B. W. Johnson) of a Special Issue on "Embedded Fault-Tolerant Systems," *IEEE Micro Magazine* , vol. 18, no. 5, 1998.

- Invited Guest Editor (with B. Cockburn and F.J. Meyer) of a Special Issue on "DRAM Architecture and Testing," *IEEE Design and Test Magazine,* vol. 16, no. 1, 1999.
- Invited Guest Editor (with J.L. Gaudiot) of a Special Issue on "Configurable Computing," *IEEE Transactions on Computers,* vol. 48, no. 6, pp. 553-555, 1999.
- Invited Guest Editor (with D. Avresky and B.J. Johnson), of a Special Issue on "Embedded Fault-Tolerant Systems," *Journal of Supercomputing: High Performance Computer Design. Analysis and Use,* Vol. 16, No. 1/2, Kluwer Academic Press, May 2000.
- Invited Guest Editor (with M.G. Sami) of a Special Issue on "Defect Tolerance in Digital Systems," *IEEE Transaction on Computers,* Vol. 49, No. 6, June 2000.
- Invited Guest Editor (with C. Metra), of a Special Issue on "Defect-Oriented Diagnosis for Very Deep Submicron Systems," *IEEE Design and Test Magazine,* Spring 2001.
- Invited Guest Editor (with D. Avresky and B.W. Johnson) of a Special Issue on "Fault Tolerant Embedded Computer Systems," *IEEE Transactions on Computers.* June 2001.
- Invited Guest Editor (with D. Kaeli and H. Hadimioglu) of a Special Issue on "Advances in High Performance Memory Systems," *IEEE Transactions on Computers,* November 2001.
- Member Editorial Board, *IEEE Press Book Series: Microelectronic Systems Principles and Practice,* 1997-current.
- Referee of IEEE Computer Magazine, 1990-1996.
- Referee of IEEE International Test Conference, 1982-present.
- Referee of IEEE Transactions on Communications, 1991-1996.
- Referee of IEE Transactions on Software and Microsystems, 1982-1986.
- Referee of ISA (Instrumentation Society of America), 1983.
- Referee of IEEE Fault Tolerant Computing Symposium, 1983-present.
- Referee of IEEE VLSI Test Symposium, 1992-present.
- Referee of IEEE Transactions on Computers, 1984-present.
- Referee of IEEE Transactions on CAD, 1988-present.
- Referee of Int. Conference on Parallel Processing, 1984-1987, 1993-1997.
- Referee of IEE Proc. on Computers and Digital Techniques, 1984-1993.
- Referee of IEEE Transactions on Parallel and Distributed Computing, 1990-1998.

- Referee of IEEE Transactions on VLSI Systems, 1992-present.
- Referee of JETTA, 1991-1998.
- Referee of IEEE Transactions on CPMT, 1994-1998.
- Referee IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 1996-present.
- Panelist, NSF Proposal Review Panel for the Design Automation Program (Testing), February 1999.
- Panelist, NSF Proposal Review Panel for the Computer Systems Architecture Program (Embedded/reconfigurable Architecture), February 1999.
- Referee of NSERC, Canada, 1990-present.
- Referee of NSF, 1989-present.

**Funded Research:**

1. Availability Analysis and Modelling of Parallel Processing Architectures, ONR Contract No. 76-C-1136, $19,250 (Unit 6, Joint Services Electronics Program), 1983-1984 ( Co-PI, Principal Investigator: R. Saeks).
2. Analysis and Design of Large Scale Computing Systems, ONR Contract No. 14-84-C-0104, $19,630, 1984-1985 (Co-PI, Principal Investigator: R. Hunt).
3. PI, Diagnosable Systems for Fault Tolerant Computing, IEEE/Engineering Foundation, $17,000, 1985-1986.
4. PI, A Laboratory for VLSI Testing and Diagnosis, AT&T IS Division, $25,000, 1985.
5. PI, Analysis and Evaluation of Class of Synchronous Architecture for Parallel Processing and Fault Tolerant Computing, AT&T Foundation, $69,200, 1985-1987.
6. PI, Fault Tolerance and Diagnosis in VLSI Systems, NATO Collaborative Research Grant, $10,166 , 1986-1988 (with M.G. Sami).
7. PI, Testing and Diagnosis of VLSI and ULSI, NATO-ASI, $35,000, 1986-1987 (with M.G. Sami).
8. PI, A Comprehensive Research Program on Large Scale Systems for Advanced Computing, AT&T Foundation, $40,000, 1986-87.
9. PI, Computer Aided Testing and Design for VLSI and WSI, AT&T Information Systems, $40,000, 1987-88.
10. PI, VLSI Testing, Texas A&M University Engineering Excellence Fund, $26,000, 1988-89.

11. PI, Wafer Scale Integration, IFIP Travel Grant, $750, 1989.

12. PI, Defect and Fault Tolerance in VLSI Systems, NSF Travel Grant, $1,200, 1990.

13. PI, Graduate Research Fellowship (for H.H. Kari), Foundation of Jenny and Antti Wihuri, Helsinki (Finland), $20,000, 1991.

14. PI, Graduate Research Fellowship (for H.H. Kari), Finnish Cultural Fund, Helsinki (Finland), $20,000, 1992.

15. PI, Testable Approaches and Design for Array Systems, NSF, MIPS Division, $80,000, 1991-93.

16. Studies on Self-Reconfigurable Massively Parallel Computers, Japan Ministry of Education, Science and Culture, $282,600, (Grant Number 05044090), 1993-96 (Co-PI, Principal Investigator: S. Horiguchi).

17. Fault Tolerance in Multiprocessor Arrays, Texas Advanced Technology Program - Research (Computer and Information Engineering), $260,000 (inclusive of $80,000 matching funds from Texas A&M University) 1994-96 (Co-PI, Principal Investigator: L. Bhuyan).

18. PI, "Testable and Fault Tolerant Design of Programmable Chips by Technology Mapping," Texas Advanced Research Program (Engineering), $232,551 (inclusive of $68,910 matching funds from Texas A&M University), 1996-1998.

19. "New Interconnection Schemes for Massively Parallel and Distributed Systems," Japan Ministry of Education, Science and Culture, $65,000, 1997-1999, (Co-PI, PI: Susumu Horiguchi).

20. PI, "Computer Engineering Capstone Design," Lockheed-Sanders, $10,000, 1999-2000.

21. PI, "Research in System-on-Chip Testing," LTX Corporation, $145,000, 1999-2000 (with F.J. Meyer).

22. PI, "Research in IC Manufacturing," Lucent Technologies Allentown, $75,000, 1999-2000.

23. PI, "Research in DSP and Computer Networks," Lucent Technologies Andover, $716,000, 2000-2001.

**Invited Seminars:**

- 1981: Northwestern University, University of London.
- 1983: University of Massachusetts - Amherst, Rice University, Arizona State University, Polytechnic Institute of New York, University of Colorado-Boulder, Virginia Polytechnic Institute and State University.

- 1984: University College London, University of Roma.
- 1985: University of Maryland-College Park, AT&T Information Systems - Broomfield.
- 1986: Politecnico di Milano, AT&T ISL-Denver.
- 1987: University of New Mexico, AT&T Bell Laboratories-Murray Hill, University of Victoria, Arizona State University, AT&T Information Systems-Denver.
- 1988: Fudan University, Academia Sinica-Beijing, University of Victoria.
- 1989: University of Victoria, University of British Columbia, Simon Frazier University.
- 1990: IBM-SID Houston, University of Victoria.
- 1991: University of Manchester Institute of Science and Technology, E-Systems-Greenville.
- 1992: University of Texas-Arlington, IEEE Circuits and Systems Society (Dallas Section).
- 1993: Texas Tech University, Colorado State University, IEEE Computer Society (Denver Section).
- 1994: Toyo University, Japan Advanced Institute of Science and Technology, University of Essex, ITRI-Austin.
- 1995: University of Sao Paulo at Sao Carlos.
- 1996: University of Houston, NTT Musashino Research and Development Center, Japan Advanced Institute of Science and Technology.
- 1997: Keio University, Japan Advanced Institute of Science and Technology.
- 1998: Northeastern University, University of Alberta, University of Connecticut, University of Oklahoma, University of Alabama-Huntsville, Yale University.
- 1999: Japan Advanced Institute of Science and Technology.
- 2000: Oklahoma State University.

**Academic Consultancy:**

1. IBM, University Program on "Reliability, Availability and Serviceability", Austin, 1983-1984.
2. International Communication Association, Professional Development Course on "Controlling Transmission Errors", Boulder, June 1986.
3. Politecnico di Milano, Technical Consultant for the ESPRIT Microelectronics Program of the European Economic Community, 1986-87.

4. SGS Microelectronics, Technical Consultant on Iterative Logic Array Testing, February 1988.

5. MIT Press, Times Mirror Books, 1989.

6. State of Louisiana, Board of Regents, 1989-1990.

7. University of Texas-Austin, Continuing Eng. Education Program, professional course on Object Oriented Programming for IBM-Austin, 1990.

8. Ministry of Education and Science of Japan, Technical Consultant on Reconfigurable Massively Parallel Computers, 1993-1996.

9. Government of Brazil (Brazilian Computer Society and State of Sao Paulo), 1995.

10. Mc Graw-Hill Publ. Co, 1996.

11. Advanced Micro Devices-Vantis, PLD Division, Sunnyvale, 1997.

12. Ministry of Education and Science of Japan, Technical Consultant on Interconnection Schemes, 1997-1999.

13. Franklin, Beedle and Associates Publ Inc, 1998.

14. McGraw-Hill Publ. Company, 1998.

15. Member of the External Advisory Board, Department of Electrical and Computer Engineering, Stevens Institute of Technology, Hoboken, 2000- current.

Extensive consultancy activities on technology assessment and evaluation with financial/banking institutions.

**BOOKS.**

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61. "A Functional Methodology for Array Testing," *Proc. 9th Annual IEEE Workshop on Design for Testability,* Vail, April 1986 (with D. Sciuto) (presentation only).

62. "On the Repair of Programmable Logic Arrays," *Proc. IEEE ISCAS 86,* pp. 649-652, San Jose, May 1986 (with C-L Wey) (invited).

63. "On a New Decision Process for the $t$-Diagnosis of an Analog System" *Proc. IEEE ISCAS 86,* pp. 1255-1256, San Jose, May 1986 (with C-L Wey).

64. "Two Algorithms for Delay-Constrained Reconfiguration of WSI Arrays," *Proc. IFIP Workshop on WSI,* Grenoble, March 1986 (with D. Sciuto) (invited)(presentation only).

65. "Diagnosis and Fault Identification Algorithms for Large Scale Computing Systems" *Proc. 1st IEEE Int. Conf. on Supercomputing Systems,* pp. 404-413, St. Petersburg, December 1985 (invited).

66. "Optimal Redundancy Management of Multi-Processor Systems for Supercomputing Applications," *Proc. 1st IEEE Int. Conf. on Supercomputing Systems,* pp. 414-422, St. Petersburg, December 1985.

67. "On Undirected Graph Diagnostic Models for VLSI Systems," *Proc. 8th Annual Workshop on Design for Testability,* pp. 4-5, Beaver Creek, April 1985.

68. "Fault Identification in t-Diagnosable Systems for Fault Tolerant Computation," *Proc. IEEE Int. Symposium on Circuits and Systems,* pp. 1539-1541, Kyoto, June 1985.

69. "On the Equivalence of Fault Identification in Undirected Graph Diagnostic Models and a Transitive Closure," *Proc. 19th Conf. on Information Sciences and Systems,* The Johns Hopkins University, Baltimore, pp. 74-75, March 1985 (abstract only).

70. "Fault Tolerance and t-Diagnosis: Affinities and Differences," *Proc. l9th Conf. on Information Sciences and Systems,* The Johns Hopkins University, Baltimore, pp. 77-79, March l985.

71. "A Testbed Environment for High Performance Computer System Design," *Proc. IEEE 4th Annual Phoenix Conf. on Computers and Communications,* pp. 523-527, Phoenix, March 1985. (with S. Ratheal).

72. "Models and Algorithms for t-Fault-Diagnosable Systems in Distributed Processing," *27th Midwest Symposium on Circuits and Systems,* pp. 647-649, Morgantown, June 1984 (invited).

73. "On the Application of t-Diagnosability to Fault Tolerant High Throughput Computation," *Proc. 18th Conf. on Information Sciences and Systems,* pp. 260-264, Princeton University, March 1984.

74. "t-Diagnosability and Fault Tolerance: System Organization for Parallel and Real Time Processing," *Computers in Comm. and Control,* D.A. Duce, Editor, Proc. Eurocon 84, 6th European Conf. on Electrotechnics, pp. 102-104, Brighton, September 1984.

75. "Performance/Efficiency Evaluation of Parallel Multiprocessor Restructurable Systems Using Analytic Modelling Techniques," *Proc. IEEE 3rd Annual Phoenix Conference on Computers and Communications,* pp. 72-79, Phoenix, March 1984.

76. "Performability Evaluation of Static and Dynamic Duplex Systems by Queueing Methods," *Computers in Comm. and Control,* D. A. Duce, Editor, Eurocon 84, 6th European Conf. on Electrotechnics, Brighton, September 1984.

77. "A Synchronous Parallel System with Interconnected Time Multiplexed Buses," *Proc. 18th Conf. on Information Sciences and Systems, pp.* 258-259, Princeton, March 1984 (with A.B. Kovaleski) (abstract only).

78. "Testable Large Scale Computer Networks: Analysis and Simulation of Reconfiguration Algorithms," *Proc. IEEE 3rd Annual Phoenix Conf. on Computers and Communications,* pp. 80-86, Phoenix, March 1984 (with S. Ratheal).

79. "Diagnosis and Performance of Large Scale Duplex Hybrid Systems," *Proc. 27th Midwest Symposium on Circuits and Systems,* pp. 650-653, Morgantown, June 1984.

80. "Intelligent Adaptability in Large Scale Systems: Distributed Networks for Triplet Testing," *Proc. IEEE Int. Symp. on Circuits and Systems,* pp. 714-717, Montreal, May 1984 (with S. Ratheal).

81. "Analysis and Design of Static and Dynamic Fault Tolerant Ring System," *Proc. 21st Annual Allerton Conf. on Communications, Control and Computing,* pp. 822-831, Urbana-Champaign, October 1983 (with V. Obac Roda and O.J. Davies).

82. "Fault Proof and Design of a Control Unit for a Fault Tolerant System in a Fly-By-Wire Aircraft," *Proc. Seventeenth Asilomar Conference on Circuits, Systems and Computers,* pp. 286-290, Pacific Grove, October 1983 (with S. Ratheal).

83. "Evaluation of a Bus Network Parallel Processing Architecture," *SIAM 1983 Conf. on Parallel Processing for Scientific Applications,* Fall Meeting, Norfolk, November 1983 (with A. B. Kovaleski and S. Ratheal)(abstract only).

84. "Soft Testbed: A First Step to Distributed Systems Design and Testing," *IEEE Computer Society Workshop on Laboratories for Reliable Systems Research* , Langley, April 1983 (with S. Ratheal)(abstract and presentation only).

85. "Efficient Testing for Analog and Digital Electronic Systems: A Highly Desirable Feature for Future Technology," *Proc. 1983 IEEE Conf. on Technology for an Efficient Tomorrow,* p. 180, Houston, April 1983 (with K. Nakajima and R. Saeks)(abstract only).

86. "Generalized Modelling of Centralized and Distributed Restructuring for Different Classes of Faults: Performance and Profits and Analysis," *Proc. 1983 IEEE Conf. on Technology for an Efficient Tomorrow,* pp. 181-186, Houston, April 1983 (with S. Ratheal).

87. "Analysis and Simulation of Triplet Configurations for Network Testability," *Proc. 17th Conf. on Information Sciences and Systems,* pp. 649-653, The Johns Hopkins University, Baltimore, March 1983 (with S. Ratheal).

88. "Control and Verification of Fault Tolerant Procedures for Duplex Hybrid System Operation," *Proc. 17th Conf. on Information Sciences and Systems* , pp. 664-668, The Johns Hopkins University, Baltimore, March 1983 (with H.E. Harvey).

89. "Generalized Modelling of Testing and Reconfigurability: System Activities for Improved Performance," *Proc. 5th Int. Conf. on Comp. Capacity Management* , pp. 169-178, New Orleans, April 1983 (with S. Ratheal).

90. "Analysis and Implementation of System Procedures for Software Implemented Fault Tolerant Microcomputer Schemes," *Proc. IEEE 2nd Annual Phoenix Conference,* pp. 123-127, Phoenix, March 1983 (with O.J. Davies, V. Obac Roda, and H.E. Harvey).

91. "Characterization of a High Available Duplex Large Scale System by Cell Partition," *Proc. 20th Annual Allerton Conf. on Communications, Control and Computing,* pp. 987-995, Urbana-Champaign, October 1982 (with O.J. Davies).

92. "On System Diagnosability Using Triplet Assertion," *Proc. IEEE Large Scale Systems Symposium,* pp. 264-268, Virginia Beach, October 1982 (with O.J. Davies).

93. "An Automated Multi-Unit Animal Activity Monitoring System," *Proc. 4th Annual Conf. of the IEEE Eng. in Medicine and Biology Soc.,* Frontiers of Computer in Medicine (COMPMED 82), Conf. Proc. vol. 4, September 1982, Philadelphia, (with O.J.Davies, V.M. B-D. Rumjanek and J. Morley).

94. "Availability Analysis of Fault Tolerant Microcomputer Systems with Periodic Preventive Replacement," *Proc. Euromicro 82, 8th Symposium on Microprocessing and .i Microprogramming,"* pp. 185-191, Haifa, September 1982 (with O.J. Davies).

95. Software Implementation of a Disagreement Detector for Duplex Hybrid Systems," *Proc. Eurocon 82, Electrotechnics Conference,* pp. 673-678, Editors E. Langer and J. Multoft, Copenhagen, North Holland Publ. Co., June 1982 (with V. Obac Roda).

96. "Microcomputer Schemes for Reliability and Faults Tolerance in Data Acquisition Applications," *Proc. of the 28th International Scientific Congress on Electronics,* pp. 484-489, Roma, March 1981.

97. "An Automated Activity Monitoring System for EAE Studies," *Proc. Multiple Sclerosis Society Annual Meeting,* vol. 2, London, February 1981, (with O.J. Davies, V.M. Rumjanek, and J. Morley).

98. "Toward More Reliable Microcomputer Systems," *Proc. IEE Colloquium on Reliable Systems for Microprocessor Control* , Digest 69, pp. 1-3, London, November 1980 (with O.J. Davies).

99. "Reliability in Microprocessor System," *Proc. 4th Annual Microprocessor Conference,* University of Liverpool, April 1980 (with O.J. Davies).

100. "Portable Pulmonary Function Data Logger," *Proc. 9th Annual Microprocessor Conference,* Biological Engineering Society, Sheffield, April 1979 (with O.J. Davies) (invited).

101. "A Portable Digital Recorder/Processor for Gamma Camera Images", *Proc. Physiological Society Annual General Meeting* , London, March 1979 (with O.J. Davies) (invited).