Meeting	Monday, Wednesday, Thursday 4:35 – 5:40 pm 153 Snell Engineering
Instructor	Prof. Jennifer Dy
Office	334 Dana Research Bldg.
Phone	617- 373-3062
E-mail	jdy@ece.neu.edu
Office Hours	Wed 2:30 – 3:30 pm Meleis (320 Dana)
	Wed 3:30 – 4:30 pm Dy (334 Dana)
	potential TA office hour TBA
Course Web Page	on Blackboard!

Course Objective

ECEU322 presents the fundamentals of digital logic analysis and synthesis. You will learn the basic concepts of logic design, including combinational and sequential logic. An important part of this course involves the design and simulation of digital circuits. In addition to handwritten homework, you will use the Xilinx Foundation Series schematic capture and simulation tools. The companion laboratory course, ECEU323 provides an opportunity to design, build and test digital circuits. The labs range in complexity from simple combinational design to a more complicated sequential design. All designs will be implemented with Xilinx field programmable gate arrays.

Co-Requisite	ECEU323 Digital Circuit Lab
Required text	Alan B. Marcovitz
	Introduction to Logic Design, McGraw-Hill. Second Edition. 2004.

Computer Laboratory

This course is tightly integrated with ECEU323. ECEU323 laboratory experiments use computer tools available on PCs throughout campus. Laboratory experiments involve analysis and simulation of digital circuits using Xilinx Foundation tools. See the ECEU323 web page on Blackboard for more details.

BE SURE TO USE THE XILINX 6.2i version of the tools.

Grading Policy

Written homework:	20%
Midterm Exams:	40%
Final Exam:	40%

Class Policies

There will be nine homework assignments, 2 midterm exams in class, and a final exam.

Homeworks will be collected during lectures on Thursday and will be collected in the beginning of the class. Late homeworks will NOT be accepted.

All work in this course, including homeworks, lab assignments and exams, are expected to represent *individual* effort. Any violations of the Northeastern University code of conduct (as described in the Student Handbook) will be referred to the Office of Student Conduct & Conflict Resolution.

There will be two midterm exams. No makeup exams will be given. A student that misses one of these exams for a legitimate reason (illness) will receive their final grade based on a combination of the other midterm exam and the final exam.

The issuance of incomplete grades will strictly follow the College of Engineering guidelines. An incomplete will only be given for missed work at the end of the term due to illness.

Topics Covered

Number systems, Boolean algebra, switching functions, combinational logic design and analysis, Karnaugh maps and minimization, design building blocks (decoders, encoders, arithmetic elements, etc.). Sequential circuit models, flip-flops and memory devices, analysis and synthesis of sequential circuits. Computer aided design, analysis and synthesis of digital circuits. Implementing digital circuits with field programmable logic. (See handout 2 for a complete list of topics).

Classroom Etiquette

As this is a large class, I would greatly appreciate it if you would treat the lectures and your fellow classmates with respect.

Please turn your cell phones off in class. If your phone rings during lecture you will be asked to leave immediately and not return for the rest of the lecture.

I will return graded homework and distribute handouts at the beginning of lecture. Please be on time to receive this material. If you arrive late DO NOT come up to the front of the class to pick up material. Wait until class is over. I will put all handouts on the course web page.

I am happy to receive and reply to email from you. (I usually do not reply to email between 8:30pm and 8:30am). If you need to speak to the instructor or have a question, feel free to send me an email and I will reply as soon as possible.