A Sub-1V Power Supply Sub-bandgap with an Extended Voltage and Temperature Range

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Abstract - This paper presents 1μW curvature-corrected bandgap reference that is capable of operating with an input power supply range of 0.88-5.5V. A 0.3V precision voltage reference is implemented with 3-stage RNMC (Reversed Nested Miller Compensation) operational amplifier and a novel PTAT current source to compensate the thermal nonlinearity of the base-emitter voltage. An experimental prototype generates a line regulation performance of 20ppm/℃ (a standard deviation of ±1.5mV before trimming) over an extended temperature range from -50 to 150 ℃.

Keywords: Tracking, filtering, estimation, information fusion, resource management.

1 Introduction

Precision voltage references with low sensitivity to temperature and voltage are in great demand for applications such as DRAM and flash memories. Conventional implementation of the bandgap voltage reference provides an output voltage almost equal to the silicon energy gap. Consequently, it cannot be used in deep-submicron technologies in the 1V range. Furthermore, a minimum supply voltage of about 2V is required and there is no headroom voltage margin above the bandgap potential. Therefore, bandgap references are not feasible in applications using 1V or lower supplies, eliminating the use of NiCad batteries. Many subbandgap reference voltage circuits have been proposed to cope with the low supply voltage requirement [1]. However, they need special process steps and characterization that increases production cost. Recently, a subbandgap reference circuit that operates with minimum power supply of 0.95V using standard CMOS process is reported [2]. They achieved reference voltage of 0.631V with 10μA quiescent current and temperature coefficient of 17ppm from -40 to 125 ℃.

The proposed subbandgap circuit improves the performance by employing 3-stage RNMC (Reversed Nested Miller Compensation) operational amplifier instead of the simple 2-stage subthreshold operational amplifier used in [2]. Second-order curvature correction of $V_{be}$ on temperature is accomplished by a current-mode technique, which employs a source follower with amplifier input stage. The reference voltage of 0.3V is obtained with 1μA quiescent current, and the temperature coefficient of 20ppm/℃ over an extended temperature range from -50 to 150 ℃ is achieved. In addition, to compensate the voltage errors at both low supply voltage (0.88V) and low temperature (-50 ℃), a substrate bias source is applied in order to increase the PTAT (Proportional To Absolute Temperature) dependence.

2 PROPOSED SUBBANDGAP REFERENCE VOLTAGE CIRCUIT

The proposed reference consists of 4 modules, which are the bandgap core, a current source, a 3-stage RNMC amplifier, and a substrate bias generator.

2.1 Subbandgap Core Circuit

The proposed bandgap core module shown in Figure 1 consists of 4 p-channel current mirrors driven by a high gain amplifier. The sub-bandgap concept uses an inner loop to develop both $V_{be}$ and $\Delta V_{be}$. The function of the third leg is to generate a multiple of the $\Delta V_{be}$ so that the sum of a diode drop and the $\Delta V_{be}$ equals the bandgap. This provides headroom as well as an absolute voltage equivalent to a diode. A current-mirroring technique in both the diode and PTAT from the inner closed loop is used to remove any loading effects. The voltages $V_a$ and $V_b$ in the inner loop are equal due to large loop gain of the amplifier and can be written as,

$$V_a = V_{be1} = V_T \ln \left( \frac{I_1}{I_s} \right)$$  \hspace{1cm} (1)

$$V_b = I_2 R_4 + V_T \ln \left( \frac{I_1}{N I_s} \right)$$  \hspace{1cm} (2)
where, \(V_T = kT/q\) is thermal voltage, \(I_s\) is saturation current, and \(N = 24\) is the base-emitter area ratio of PNP\(_1\) and PNP\(_2\) diodes as shown in Figure 1. Using (1) and (2), the reference voltage of the proposed circuit are derived as following.

\[
V_{ref} = \frac{R_5}{R_5 + R_4} \left[ V_{be} + \frac{KR_5}{R_4} \left( V_T \ln(KN) - V_m \right) \right]
\]

where, \(K\) is the current mirror ratio \(=I_{p1}/I_{p2}=I_{p4}/I_{p3}\) and \(V_{os}\) is the amplifier input offset.

The reference voltage of 300mV is achieved from the experimental prototype. This can be adjusted to higher reference voltages; just two resistors \((R_5, R_6)\) ideally adjust the output to any desired value between 0 and the sub-threshold voltage.

2.2 PTAT Current Source

A conventional PTAT current source [3] is sensitive to process variation. The proposed PTAT current source shown in Figure 2 improves process sensitivity by introducing large loop gain using operation amplifier. The drain current of MOS transistor that operates in the weak inversion region assuming \(V_D >> V_T\) is given by,

\[
I_D = \frac{V_D - V_T}{\eta T}
\]

where, \(I_{D0}\) is the characteristic current, \(S\) is the aspect ratio of the transistor, \(\eta\) is the slope factor. The reference current is computed as,

\[
I_{ref} = \frac{V_T}{R_3} \ln \left( \frac{S_{p5}S_{n7}}{S_{p6}S_{n6}} \right)
\]

2.3 RNMC Operational Amplifier

The proposed bandgap reference is based on a 3-stage reversed nested miller compensation (RNMC) amplifier [4]. A RNMC operational amplifier shown in Figure 3 with a sub-threshold current reference in a closed loop ensures the potentials track over all conditions. The dc gain of the 3-stage amplifier is \(A_{dc} = A_1A_2A_3\) and \(A_i = g_{mi}R_{oi}\) where \(A_i, g_{mi}\), and \(r_{oi}\) are the \(i\)th stage gain, transconductance and output resistance respectively. \(g_{mi}\) in weak inversion region is \(I_D/\eta V_T\) and the temperature term in \(g_{mi}\) cancels out with PTAT current. Therefore, the gain of the amplifier divides the error with PTAT temperature tracking characteristics for constant \(g_{mi}\) and gain flatness and the gain is affected only by the temperature slope of the channel length modulation. Selecting the reference voltage below half the supply voltage results in reducing the channel length variation dependency. The third stage input is connected to the output of the differential stage; implementing push-pull output stage configuration. The high gain stage amplifier design provides higher initial accuracy of power supply rejection ratio (PSRR) and
recovery time. Since the diode inputs are typically below the threshold voltage and the input stage is also in the subthreshold region of operation, the applied input voltage can be below the threshold.

Figure 3. RNMC Operational Amplifier

2.4 Substrate Bias

The proposed subbandgap reference circuit employs substrate bias technique for PMOS transistors in N-well process. Substrate bias generator shown in Figure 1 keeps the substrate potential lower than the source. Some mismatch due to the voltage coefficient of the N-well resistor is minimized by low back bias potentials. To compensate the voltage errors at both low supply voltage (0.88V) and low temperature (-50°C), a substrate bias source is applied, which increases the PTAT dependence.

3 Experimental Results

A 20-PPM/°C sub-bandgap reference with a supply voltage of about 0.3 volts is demonstrated. Figure 4 shows measured data results of the dc regulation of output versus input voltage with temperature. To the first order, the diode temperature coefficient can be accurately predicted based on the junction thickness and current density, or r (curvature coefficient) minus n (ideality factor) described in [5]. For junction depths of 0.5μm and greater, the ‘r – n’ factor is approximately 2 which implies a near theoretical optimum bandgap voltage of 1.23V for optimum temperature compensation. The temperature coefficient is about 50 PPM/°C based on uncorrected curvature. In this paper, it is shown that the extended temperature range design reduces the effect of temperature curvature to less than 20 PPM over an extended temperature range of 200°C. Some mismatch due to the voltage coefficient of the N-well resistor is minimized by low back bias potentials. The RNMC amplifier design provides higher initial accuracy, a PSRR greater than 56dB at 10KHz, and 10μs recovery time with small sample distribution.

Figure 5 shows that the quiescent current changes with changing temperature and supply voltage. A comparison with recent reported low-voltage bandgap references [6], [7] is tabulated in Figure 6. Wideband noise is measured as 7μV RMS at 1kHz as shown in Figure 7.

Figure 4. Waveforms of Supply and Temperature Regulation

Figure 5. Waveforms of Total Quiescent Current

Figure 6 Comparison with the Performance of Bandgap Voltage References

<table>
<thead>
<tr>
<th>Technology</th>
<th>Proposed</th>
<th>Previous [6]</th>
<th>Previous [7]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold voltage (V)</td>
<td>Vtn = 0.6</td>
<td>Vtn = 0.9</td>
<td>Vtn = 0.9</td>
</tr>
<tr>
<td></td>
<td>Vtp = -0.3</td>
<td>Vtp = -0.9</td>
<td>Vtp = -0.9</td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>0.88 ~ 5.5</td>
<td>0.98 ~ 1.5</td>
<td>2 ~ 4</td>
</tr>
<tr>
<td>Supply current (μA)</td>
<td>1</td>
<td>18</td>
<td>23</td>
</tr>
<tr>
<td>Reference voltage (mV)</td>
<td>298 ± 1.5</td>
<td>603 ± 2.2</td>
<td>1142 ± 1.43</td>
</tr>
<tr>
<td>Temperature range (°C)</td>
<td>-50 ~ 150</td>
<td>0 ~ 100</td>
<td>0 ~ 100</td>
</tr>
<tr>
<td>Temperature coefficient (ppm/°C)</td>
<td>20</td>
<td>15</td>
<td>6.1</td>
</tr>
<tr>
<td>FSR @ 10kHz (dB)</td>
<td>56</td>
<td>44</td>
<td>47</td>
</tr>
<tr>
<td>Die size (mm²)</td>
<td>0.12</td>
<td>0.24</td>
<td>0.057</td>
</tr>
</tbody>
</table>

Figure 6 Comparison with the Performance of Bandgap Voltage References

A standard CMOS N-well process with a high value resistor (poly silicon: 2KΩ) is used to minimize die area. The use of a simple circuit technology results in a small silicon area of 0.12mm² as shown in Figure 8, power consumption of less 1μW at a 1V supply and a PSRR greater than 56dB over a wide frequency band. The design is used in a low drop-out (LDO) power supply of National Semiconductor (LP3998).
4 Conclusions

A sub-bandgap reference with power dissipation as low as 1μW is realized in a 0.5μm 5V process. Since the sub-bandgap is realized by averaging both the $V_{be}$ and PTAT instead of summing them, process sensitivity is reduced. The bandgap reference achieves significant temperature stability (a before trim temperature coefficient of less than 20PPM/℃) over an extended temperature range (-50℃ to 150℃), and provides a higher precision than previously reported.

References


