ECE 3626
Integrated Circuit Fabrication Processes
Winter 2002
Final Exam
Open Book, Open Notes

Name:__________________

Student ID:______________

Assigned: **03/07/2002**
Due: **03/14/2002 at 2:00 pm in Rm. 329 Dana**

The following exam is open book and open notes. You may use any source of information that you find useful *except* consulting with other students, faculty, staff, or other experts.

At times, you may find that it is necessary to make approximations or assumptions. When you do, please indicate that an assumption was made and justify its use in writing.

If you need assistance, I will have Office Hours during the scheduled exam period:

8:30-11:30 am, Tuesday, March 12, 2002

You may also email questions to me at *hopwood@ece.neu.edu*

Problem 1 (30 pts): Ion implantation

Rather than the usual Gaussian profiles obtained by ion implantation, a certain process requires that a more uniform density of boron dopant be implanted throughout the p-type well region. The well region begins at the wafer surface and extends 0.5 μm into the surface.

One method of obtaining a more uniform implant profile is by performing multiple ion implantations with varying dose and energy.

a) Design a 3-step implant (and activation anneal) to achieve a nearly uniform doping level of 10^{17} cm^{-3} throughout the first 0.5 μm of the surface. (E_i and ϕ_i, for i=1, 2, 3)

b) Describe the activation anneal needed for this implant process (time and temperature)

c) Specify the mask material and thickness needed to protect underlying silicon from implantation ($N_D=10^{14}$ cm^{-3})

d) When completed, use tsuprem to confirm that your process is correct (Note: DO NOT use tsuprem to design the process by trial and error. You should develop the process analytically first, then simulate it.)

Problem 2 (30 pts): Plasma deposition

Polysilicon is to be deposited at low temperature using plasma enhanced CVD. To prevent gas-phase nucleation of silicon particles due to heterogeneous reaction paths, the feed gas (SiH_4) is greatly diluted with argon.

Flow of SiH_4 = 1 cm^3/minute at STP
Flow of Ar = 100 cm^3/minute at STP

Use a simplified set of reactions for this problem consisting of dissociation of SiH_4 and ionization of argon (note: T_e has units of eV).

$Ar + e \rightarrow Ar^+ + 2e$	$k_1 = 1.23E\text{-}7\exp(-18.68/T_e)\ cm^3s^{-1}$
$SiH_4 + e \rightarrow SiH_3 + H + e$	$k_2 = 1.5E\text{-}8\exp(-10/T_e)\ cm^3s^{-1}$
$SiH_4 + e \rightarrow SiH_2 + 2H + e$	$k_3 = 1.5E\text{-}9\exp(-10/T_e)\ cm^3s^{-1}$

The sticking coefficients for the silane-related molecules to both the chamber walls and the wafer surface are:

$\gamma_{SiH4} = 0.054 \exp(-0.86\ eV/ kT)$

$\gamma_{SiH3} = \gamma_{SiH2} = 1$

The plasma chamber consists of two parallel plates that are both energized by radio frequency power at 50 W each. Each plate has an area of 250 cm^2 and the separation between plates is 8 cm. You may estimate that the sheath voltage is 100 volts. The chamber is constantly evacuated by a turbomolecular pump which maintains a pressure of 7×10^{-3} torr.

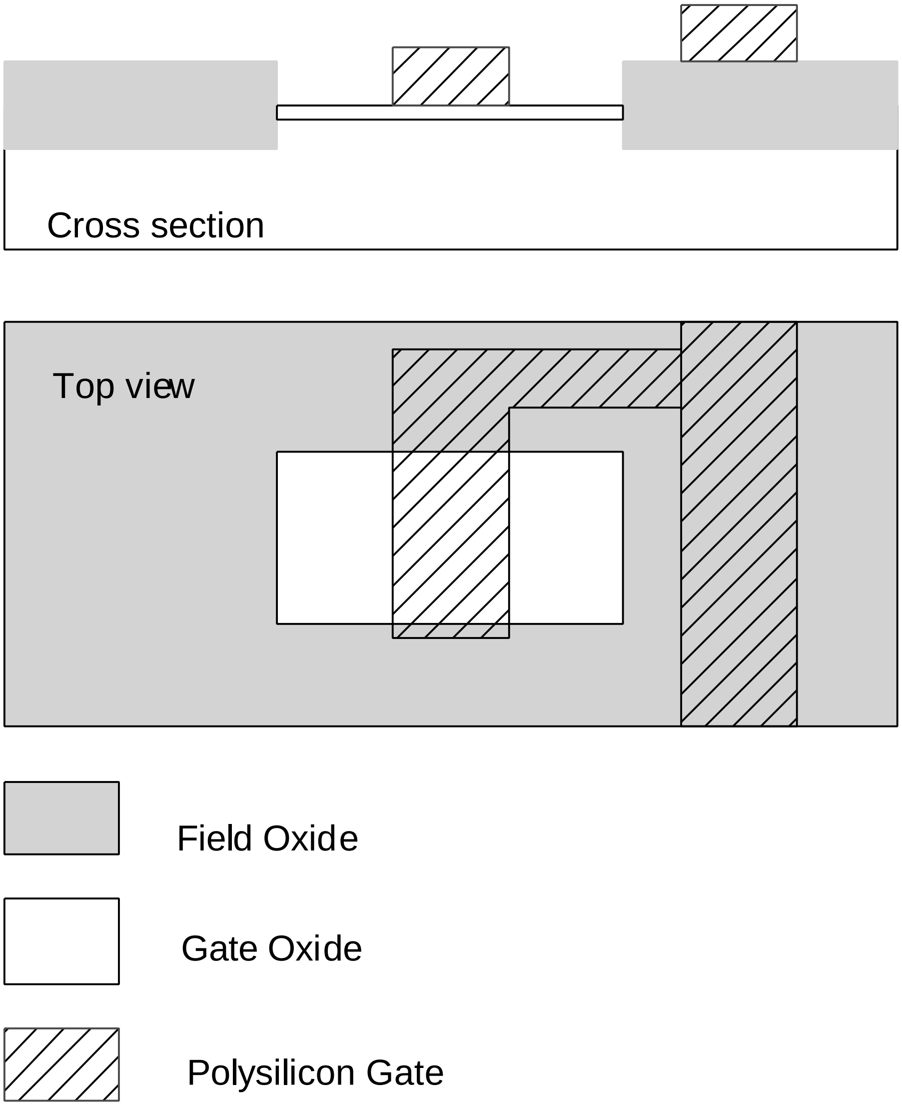
a) Find the electron density and electron temperature within the plasma assuming that the presence of SiH_x (x=2-4) is a negligible perturbation.

b) Determine the time required to deposit a 0.2 μm thick film of polysilicon to be used as a MOSFET gate material (ignore any hydrogen that may be incorporated in the film). Recall $n_{Si} = 5 \times 10^{22}\ cm^{-3}$.

c) Explain the advantages and disadvantages of using plasma-enhanced CVD of polysilicon rather than conventional (thermal) low pressure CVD of polysilicon.

Problem 3 (30 pts): Lithography

After polysilicon is deposited over the entire wafer as in problem 2, the gate electrodes must be patterned using photoresist. We would like 0.3 μm gates. The polysilicon resides atop both a 10 nm gate oxide and a 1 μm field oxide as shown below. Design a photolithography process that will pattern the polysilicon. You should specify the type of photoresist, an exposure wavelength for the light source, a numerical aperture for the projection printer, and a spatial coherence for the light source. (You may use the text *and/or* search the web for PR specifications.)



Problem 4 (10 pts)

Answer the following questions with a brief written paragraph:

a) Assuming that the photoresist in Problem 3 is 0.5 μm thick, describe an etch process for removing the unwanted polysilicon from the wafer. You should include specifications such as the type of etch, the selectivities, the anisotropy, λ_i/s, etc.

b) Conventional interconnects consist of aluminum(Si/Cu) alloy wires and SiO_2 insulation (i.e.,interlayer dielectrics, ILDs). Read the articles on "Dual Damascene Copper" and "Low-k Dielectrics" that are posted on the course's webpage at

http://www.ece.neu.edu/edsnu/hopwood/ece3626.html

In one paragraph, describe the importance of the recent trend toward high-conductivity metals and low-permittivity dielectric interconnect materials.