

the aspect ratio of the lines increases, it becomes more difficult to obtain very good etching results and very good gap fill results," noted Sam Broydo, managing director of core technical capabilities at Applied Materials (Santa Clara, Calif.). "Damascene doesn't have those two challenges. But it replaces them with other challenges. Some people consider those other challenges, such as filling trenches with metal and then doing CMP of metal, simpler than the first two. But there is some disagreement about that."

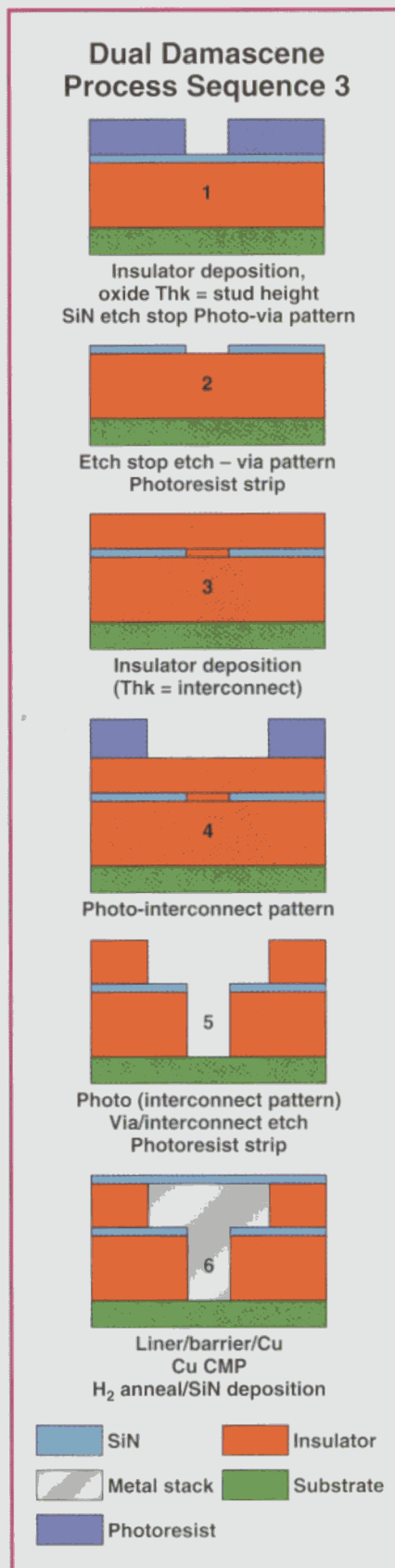
Although the industry's experience with dual damascene processing has been relatively limited, several different strategies have been investigated. Following is a look at three different dual damascene process sequences and an examination of the advantages and disadvantages of each.

Dual damascene processes

Certainly the oldest and perhaps the most intuitively obvious approach to dual damascene processing is shown in Figure 1. After deposition of the insulator, a trench is etched. This is followed by the application of a fairly thick layer of photoresist. The pattern for the via is then exposed and developed and finally etched through the oxide to the substrate. In reality, this is not a very manufacturable process because it is difficult to develop a deep hole in the thick layer of photoresist, and to etch an even deeper hole through the underlying oxide. Also, noted Broydo, because of alignment issues, the trench needs to be much wider than the via.

Figure 2 illustrates an alternative process sequence for dual damascene where the via is etched first and the trench second. This avoids the problems of deep vias found in the first sequence, and some companies are reportedly working to turn this into a manufacturable process. There are two concerns with this process, however. One is that since no etch stop is used, the trench etch must be stopped somewhere in the middle of the oxide. This requires very well-controlled etch rate and uniformity across the wafer and from wafer to wafer. The second con-

3. Trench and via etching is done in one step in this dual damascene process, with a very thin silicon nitride layer acting as a hard mask. (Source: Applied Materials)



cern is that it will be difficult to completely remove all the photoresist and photoresist residue from the vias.

Figure 3 illustrates a third, slightly more complex process sequence, yet one that is perhaps more manufacturable. What makes this approach different is the use of a very thin silicon nitride layer that acts as a hard mask. Here, the silicon nitride layer, which could be as thin as 250 Å, is deposited on top of the dielectric and then patterned to create a hole for the via. A second layer of dielectric is then deposited on top of the silicon nitride. The trench is then patterned and etched into this top layer of dielectric stopping on the silicon nitride layer. The etch continues, however, through the hole in the nitride to form the via. Finally, the trench and via are filled. Note that the illustration shows the trench much wider than the via, but in practice they will be close to the same size.

The main advantage of this sequence, according to Broydo, is that there is only one etch step and one metal fill step.

Conclusion

Dual damascene will likely be the patterning choice for copper interconnects, although it is not yet clear how soon copper will be put into production. In the meantime, the industry will experiment with dual damascene aluminum, where aluminum CMP and aluminum gap fill present the biggest challenges. At some point, the industry will also have to decide how and when to integrate low-k dielectrics into its strategies for interconnects. □

References

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