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Making the Move to Dual Damascene Processing

A look at several different dual damascene processing strategies.

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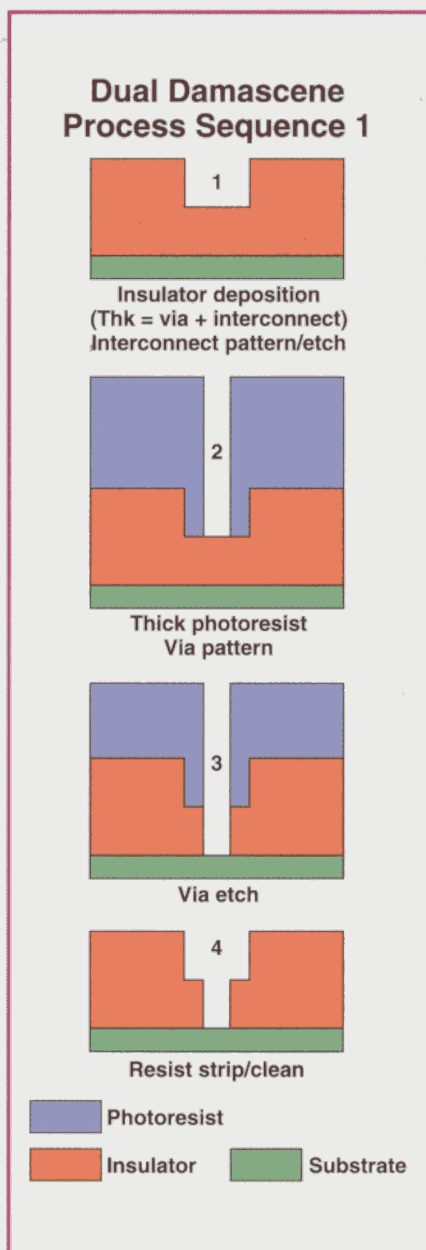
Key Technologies:

- Dual damascene
- Multilevel metal
- Interconnects

At A Glance:

Dual damascene processing is likely to be the way interconnects are formed in the future. It eliminates not only the need for metal etch — which is increasingly challenging in aluminum interconnects and nearly impossible with copper — but also the need for dielectric gap fill, another challenging process. Three different fabrication sequences for dual damascene processing are described.



1. This process sequence for dual damascene was the first one tried by most companies to investigate the dual damascene concept, but developing and etching deep via holes through a thick layer of photoresist is difficult. (Source: Applied Materials)

The practice of creating patterns by metal inlays was first developed by the ancient artisans of Damascus. Today, thousands of years later, a similar process is being adopted by the semiconductor industry. Called "damascene" processing in honor of its origins, the technique involves the creation of interconnect lines by first etching a trench or canal in a planar dielectric layer, and then filling that trench with metal, such as aluminum or copper. In *dual* damascene processing, a second level is involved where a series of holes (i.e., contacts or vias) are etched and filled in addition to the trench. After filling, the metal and dielectric are planarized by chemical-mechanical polishing (CMP).

The main advantage of damascene processing is that it eliminates the need for metal etch. This is an important concern as the industry moves from aluminum to copper, since copper is extremely difficult to etch. A second advantage of damascene processing is that it eliminates the need for dielectric gap fill. Metal etch and dielectric gap fill are seen as two of the industry's greatest challenges in the drive to smaller dimensions. A third advantage is that a damascene approach gets around some problems associated with lithographic overlay tolerance, making it possible to achieve higher interconnect packing density.

Too many changes?

Copper, which has a lower resistance than aluminum, is not the only material that the semiconductor industry is looking to change. To further reduce time delays and increase on-chip speed, there is also interest is moving to materials with a low dielectric constant (k).[1]

The challenge is that it would be difficult and risky to make all three large-